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Ferroelectric Polarization Switching of Hafnium Zirconium Oxide in a Ferroelectric/Dielectric Stack

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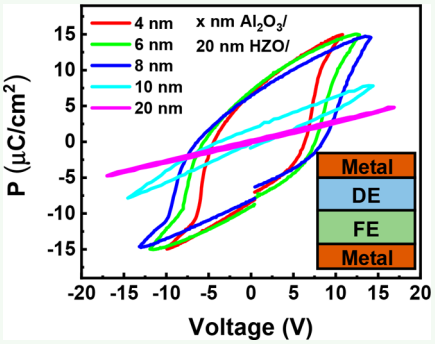
Supporting Information

ABSTRACT: The ferroelectric polarization switching in ferroelectric hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO) in the HZO/Al_2O_3 ferroelectric/dielectric stack is investigated systematically by capacitance−voltage and polarization−voltage measurements. The thickness of dielectric layer is found to have a determinant impact on the ferroelectric polarization switching of ferroelectric HZO. A suppression of ferroelectricity is observed with a thick dielectric layer. In the gate stacks with thin dielectric layers, a full polarization switching of the ferroelectric layer is found possible by the proposed leakage-current-assist mechanism through the ultrathin dielectric layer. Theoretical simulation results agree well with experimental data. This work clarifies some of the critical parts of the long-standing confusions and debate related to negative capacitance field-effect transistors (NC-FETs) concepts and experiments.



KEYWORDS: *ferroelectric, HZO, Fe-FET, negative capacitance, steep-slope*

INTRODUCTION

A ferroelectric material has two stable polarization states with different directions, which are switchable by the external electric field, and thus is extensively explored for nonvolatile memory applications. Using ferroelectric field-effect transistors (Fe-FETs) as FET-type ferroelectric memory is a promising ferroelectric memory architecture because of its high density and nondestructive readout.[1−4] Recently, using a ferroelectric-gated transistor as a negative capacitance field-effect transistor (NC-FET) has attracted tremendous attention as a novel steep-slope device.[5−9] In both Fe-FET and NC-FET, a ferroelectric (FE) insulator and linear dielectric (DE) insulator bilayer stack[10−17] is applied as the gate structure. The necessity of such a linear DE layer is because an interfacial oxide layer between the semiconductor channel and FE insulator is required to improve the ferroelectric/semiconductor interface and meanwhile provide sufficient capacitance matching if the quasi-static negative capacitance (QSNC) concept is applied for the development of NC-FETs.[5] The QSNC definition was introduced to distinguish between the stabilized NC effect and transient NC effect.[18] One important fact, which has been overlooked in the past several years, is that the FE/DE stack capacitor is fundamentally different from an FE capacitor and DE capacitor in series.[18,19] Therefore, the complete understanding of the impact of the DE layer on the ferroelectric properties of an FE/DE stack is crucial to study of the ferroelectric switching mechanism in Fe-FETs and NC-FETs.

Ferroelectric hafnium oxide, such as hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO), has been recently discovered as an ultrathin CMOS compatible high performance ferroelectric insulator.[20,21] Therefore, HZO is chosen as the FE insulator for this study, and Al_2O_3 is chosen as the linear DE insulator to study the ferroelectric polarization switching in the FE/DE stack. It is well-known that ferroelectric HZO has a thickness-dependent remnant polarization (P_r) at about 10−30 μC/cm.[2,22,23] However, a conventional dielectric insulator cannot support such a large charge density. For example, Al_2O_3 has a typical dielectric constant of 8 and a breakdown electric field less than 1 V/nm.[24] The calculated charge density at breakdown electric field is about 7 μC/cm^2, which is the maximum charge density (Q_{max}) for ideal Al_2O_3 to be able to support without breakdown. Note that in reality, this value for Q_{max} is much smaller. As can be seen, even in ideal case, there is a big gap between the remnant polarization in HZO and the maximum charge density in Al_2O_3. This fact can also be generally applied to other FE/DE stack systems. Thus, the puzzle and confusion in the field is how can ferroelectric polarization switching happen in an FE/DE stack without sufficient charge balance? Such charge difference can only be explained by introducing the leakage-current and interfacial charges. The impact of leakage current in FE/DE bilayer was previously reported, and the interfacial charging is believed to be important in the ferroelectric switching process by a thermodynamic free energy model.[10] In FE hafnium oxide systems, the discussions are mostly focused on the impact of leakage current on the negative capacitance effect.[15−17,25] The hysteresis-free NC effect in HZO/Al_2O_3 is reported by fast pulse measurement; the impacts of leakage current and charge trapping are minimized because of the fast pulses.[15−17,26]

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In this work, we provide a simple understanding of the ferroelectric polarization switching process in an FE/DE stack by introducing the leakage current through the thin DE layer and only considering the electrostatics. The ferroelectric polarization switching of HZO in the HZO/Al_2O_3 FE/DE stack is investigated systematically by capacitance−voltage ($C-V$) and polarization−voltage ($P-V$) measurements. The thickness of the dielectric layer is found to have determinant impact on the ferroelectric polarization switching of ferroelectric HZO. The suppression of ferroelectricity is observed with thick dielectric layer. In the gate stacks with thin dielectric layers, a full polarization switching of the ferroelectric layer is found possible by the proposed leakage-current-assist mechanism through the ultrathin dielectric layer. It is confirmed that the charge needed for ferroelectric polarization switching comes from the leakage current through the thin dielectric layer. Without such leakage current to realize the charge balance, the FE HZO cannot be fully polarized.

EXPERIMENTAL SECTION

Figure 1 shows the experimental device structures. Four types of capacitor structures are used in this work: (a) TiN/Al_2O_3/TiN (type A), (b) TiN/HZO/TiN (type B), (c) TiN/Al_2O_3/HZO/TiN (type C), and (d) TiN/Al_2O_3/TiN/HZO/TiN (type D). The device fabrication process started with the standard solvent cleaning of heavily p-doped Si substrates (resistivity < 0.005 Ω·cm). TiN was deposited by atomic layer deposition (ALD) at 250 °C, using $[(CH_3)_2N]_4Ti$ (TDMAT, heated up to 60 °C) and NH_3 as the Ti and N precursors, respectively. All TiN layers are metallic and 30 nm thick. $Hf_{1-x}Zr_xO_2$ film was deposited by ALD at 200 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf, heated up to 60 °C), $[(CH_3)_2N]_4Zr$ (TDMAZr, heated up to 75 °C), and H_2O as the Hf, Zr, and O precursors, respectively. The $Hf_{1-x}Zr_xO_2$ film with $x = 0.5$ was achieved by controlling the HfO_2/ZrO_2 cycle ratio of 1:1. The ALD deposition of TiN and HZO was in two separated ALD chambers to avoid cross-contamination. The two ALD chambers are connected externally by an Ar environment in a glovebox to avoid environmental contamination. After the deposition of type A−D structures, the samples were annealed at 500 °C in N_2 environment for 1 min by rapid thermal annealing. Then, Ti/Au top electrodes were fabricated by photolithography, e-beam evaporation, and a lift-off process (capacitor area = 5024 μm^2). CF_4/Ar dry etching was done to remove top TiN layer for device isolation for type A−C capacitors. For type D capacitors, BCl_3/Ar dry etching was used to remove the top Al_2O_3 layer, and CF_4/Ar dry etching was used to remove the top and middle TiN layers. All electrical measurements were done at room temperature in a cascade summit probe station. $C-V$ measurement was performed using an Agilent E4980A LCR meter, and $P-V$ measurement was carried out using a Radiant RT66C ferroelectric tester.

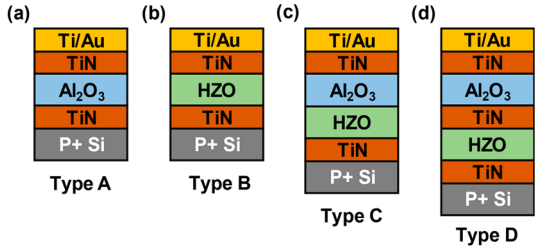

Figure 1. Capacitor structures used in this work. (a) Al_2O_3 only (type A), (b) HZO only (type B), (c) Al_2O_3 and HZO stack without internal metal (type C), and (d) Al_2O_3 and HZO stack with TiN layer as the internal metal (type D).

RESULTS AND DISCUSSION

Figure 2(a) shows the $C-V$ measurement of a type A capacitor with 20 nm Al_2O_3, from 1 kHz to 1 MHz. Figure 2(b) shows the $P-V$ measurement of the same type A capacitor, showing a linear dielectric characteristic. Both measurements (small signal $C-V$, dP/dV in $P-V$) give consistent capacitance values for the type A dielectric capacitor with a capacitance of ~0.33 $\mu F/cm^2$ and a corresponding dielectric constant of ~8. Figure 3(a) shows the $C-V$ measurement of a type B capacitor with 20 nm HZO, from 1 kHz to 1 MHz. The $C-V$ measurement of a type B capacitor shows two signature peaks in the $C-V$ hysteresis loop as the ferroelectric characteristics. The different capacitances at different voltages in $C-V$ are attributed to the different dielectric constant due to the difference in atomic structures in different ferroelectric polarization states. The corresponding dielectric constants are calculated, as also shown in the right axis. Figure 3(b) shows the $P-V$ measurement of the same type B capacitor, showing a ferroelectric hysteresis loop.

Figure 4(a) shows the $C-V$ measurements of type C capacitors with 20 nm HZO and Al_2O_3 from 0 to 20 nm, measured at 10 kHz. The capacitances of type C capacitors decrease with thicker Al_2O_3 as expected. The signature two capacitance peaks due to ferroelectricity in the $C-V$ hysteresis loop decrease and eventually disappear in the 20 nm HZO/20 nm Al_2O_3 stack, suggesting the reduction of ferroelectricity in the thick DE layer and FE layer stack. This feature is even more clearly presented in Figure 4(b), which shows the $P-V$ measurements of type C capacitors with 20 nm HZO and Al_2O_3 from 4 to 20 nm. The applied voltage ranges are maximized in $P-V$ measurement before the leakage current has essential impacts. The significant decrease of remnant polar-

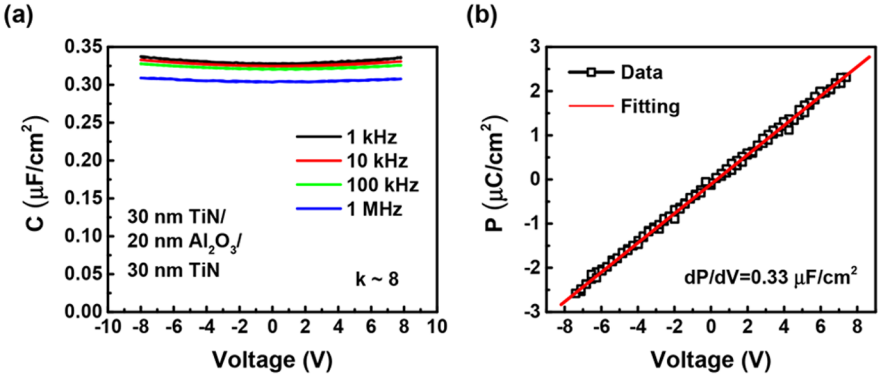

Figure 2. (a) $C-V$ measurement and (b) $P-V$ measurement on a type A capacitor with 20 nm Al_2O_3.

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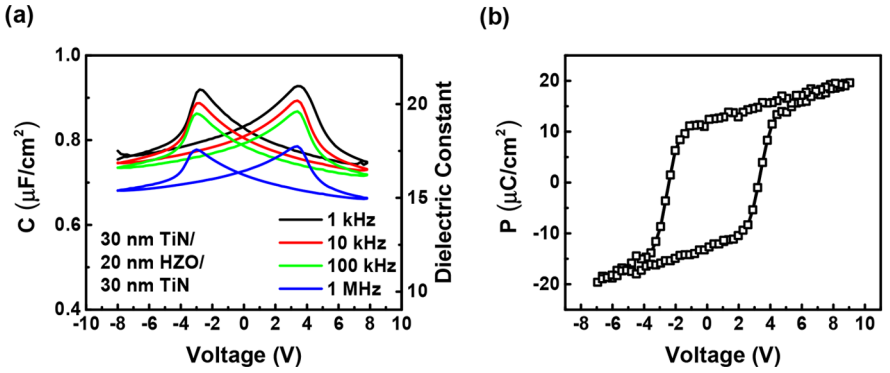

Figure 3. (a) $C-V$ measurement and (b) $P-V$ measurement of a type B capacitor with 20 nm HZO.

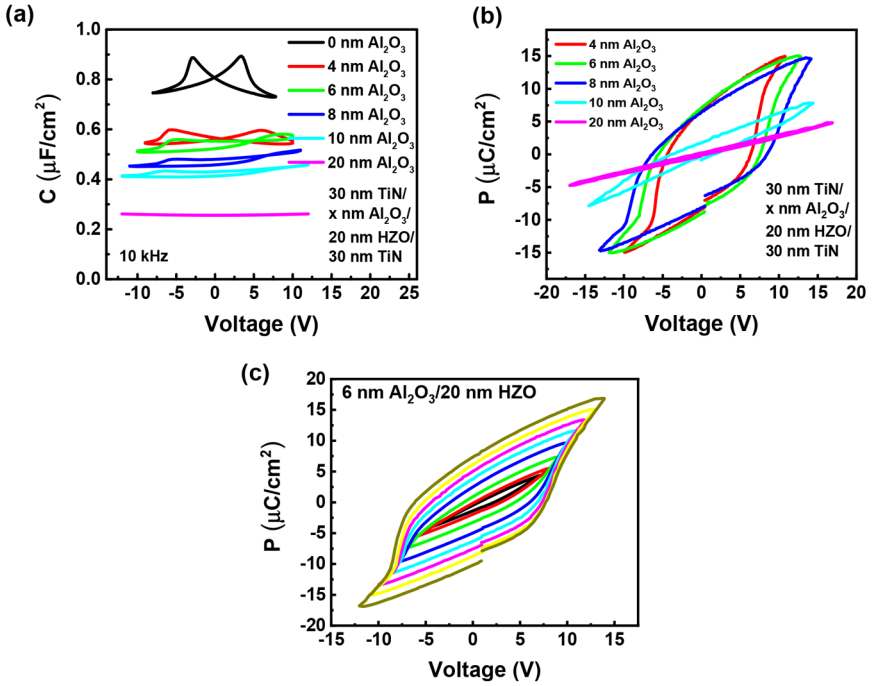

Figure 4. (a) $C-V$ measurements and (b) $P-V$ measurements on type C capacitors with different Al_2O_3 thicknesses and 20 nm HZO. (c) $P-V$ measurements on a type C capacitor with 6 nm Al_2O_3 and 20 nm HZO at different voltage sweep ranges.

ization in $P-V$ hysteresis loops is clearly observed with thicker DE layers. The $C-V$ measurements and $P-V$ measurements consistently confirm that a thick DE layer can suppress the ferroelectricity in the FE/DE stack. Figure 4(c) shows the $P-V$ characteristics of an FE/DE capacitor with 20 nm HZO and 6 nm Al_2O_3, measured at different voltage sweep ranges. The coercive voltage and remnant polarization are found to be dependent on the sweep voltage range.

To further understand the physics behind the DE layer thickness dependence on the ferroelectricity of the FE/DE stack, a theoretical analysis is provided, as shown in Figure 5. To understand the dynamic process of ferroelectric switching, this process is plotted by a two-step process: before ferroelectric polarization switching and after ferroelectric polarization switching. As is well-known, the ferroelectric polarization switching is atom reposition within the unit cell, so it is always slower than the electron redistribution. Thus, the two-step assumption is valid. For simplicity, it is assumed the FE layer has a dielectric constant of ϵ_{FE} (without considering ferroelectric polarization) and a thickness of t_{FE}; the DE layer has a dielectric constant of ϵ_{DE} and a thickness of t_{DE}. It also assumes that the FE layer has equal numbers of polarization up states and polarization down states in the virgin state before the measurement, so the net polarization is zero, as in Figure 5(a). This situation is similar to two high-k dielectric stacks. We define V_{TOT} to be the voltage applied to the FE/DE stack, V_{DE} to be the voltage across the DE layer, and V_{FE} to be the voltage across the FE layer. Therefore, before the ferroelectric polarization switching, the voltages across the DE layer and FE layer are

$$V_{DE,init} = \frac{V_{TOT}\epsilon_{FE}t_{DE}}{\epsilon_{DE}t_{FE} + \epsilon_{FE}t_{DE}} \quad (1)$$

$$V_{FE,init} = \frac{V_{TOT}\epsilon_{DE}t_{FE}}{\epsilon_{DE}t_{FE} + \epsilon_{FE}t_{DE}} \quad (2)$$

There are totally three different cases according to the different DE thicknesses. Here, we first assume the leakage current is zero and then discuss the impact of leakage current. First, if t_{DE} is very thick, then $V_{FE,init}$ can be sufficiently small so that it is smaller than the coercive voltage (V_c) of the FE layer, according to eq 2. Thus, no polarization switching can happen.

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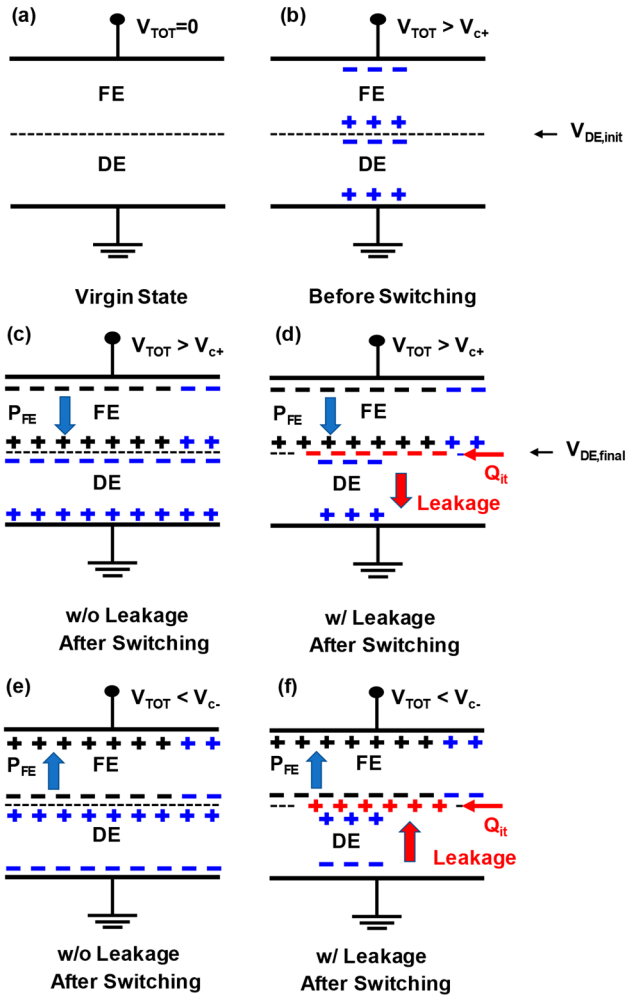

Figure 5. Illustration of charge distribution in FE/DE stack in the following conditions. (a) $V_{TOT} = 0$, and FE layer is not polarized. (b) V_{TOT} larger than positive coercive voltage V_{c+} before polarization switching. V_{TOT} larger than positive coercive voltage V_{c+} after polarization switching (c) assuming no leakage current through the DE layer and (d) assuming the existence of leakage current through the DE layer. V_{TOT} less than negative coercive voltage V_{c-} after polarization switching (e) assuming no leakage current through the DE layer and (f) assuming the existence of leakage current through the DE layer. Type of charges: black, ferroelectric polarization; blue, dielectric polarization; red, interfacial trapped charge.

So, the $C-V$ and $P-E$ characteristics behave like a linear dielectric insulator. Second, if $V_{FE,init} > V_c$ but t_{DE} is sufficiently thick, the FE layer cannot be fully polarized. As the polarization switching happens, V_{DE} increases until V_{FE} reaches V_c, and the polarization process cannot continue. In this case, the total charge in the FE layer (Q_{FE}) can be approximated as $\epsilon_{DE}(V_{TOT} - V_c)/t_{DE}$, where we have ferroelectric polarization charge (P_{FE}) < P_r and $V_{DE,final} = Q_{FE}/(\epsilon_{DE}/t_{DE})$. Note that $P_{FE} \cong Q_{FE} = Q_{DE}$ if the P_{FE} is significantly larger than the dielectric charge. Such an assumption is made for the simplicity of qualitative discussion and does not affect the conclusion. The numerical simulation including the difference of P_{FE} and Q_{FE} gives the same conclusion. Third, if the DE layer is thin enough so that the second criterion is not meet anymore, we can have the FE layer fully polarized. So V_{DE} can be estimated as $V_{DE,final} = P_r/(\epsilon_{DE}/t_{DE})$. It is clear that if Q_{FE} is larger than the maximum charge density in the DE layer, $V_{DE,final}$ will be larger than the breakdown voltage (V_{BD}) of the DE layer, which of course cannot happen. What is really happening in this process (if $V_{DE,final} > V_{BD}$) is when V_{DE} rises from $V_{DE,init}$ to $V_{DE,final}$, the DE layer first becomes leaky, and these leakage charges will balance the ferroelectric polarization charges so that V_{DE} cannot reach V_{BD}. Thus, all the ferroelectric polarization charges are balanced by the charges from leakage current instead of the charge in DE layer. Therefore, in the thin DE limit, the ferroelectric polarization switching process is a leakage-current-assist process. At the extremely leaky limit, it becomes almost like a metal−FE−metal structure. Here is a summary of all three cases

Case 1: Thick DE limit, no polarization switching

$$V_{FE,init} < V_c \tag{3}$$

Case 2: Moderate DE thickness, partial switching (by dielectric charge or leakage)

$$V_{FE,init} > V_c \text{ and } P_r > \epsilon_{DE}(V_{TOT} - V_c)/t_{DE} \tag{4}$$

$$P_{FE} = \epsilon_{DE}(V_{TOT} - V_c)/t_{DE} \tag{5}$$

$$V_{DE,final} = P_{FE}/\frac{\epsilon_{DE}}{t_{DE}} \tag{6}$$

Case 3: Ultrathin DE limit, leakage-current-assist switching

$$P_r < \epsilon_{DE}(V_{TOT} - V_c)/t_{DE} \tag{7}$$

$$P_{FE} = P_r \tag{8}$$

$$V_{DE,final} = P_r/\frac{\epsilon_{DE}}{t_{DE}} \tag{9}$$

To calculate the leakage-current-assistant switching process as in case 3, a theoretical model is developed. Figure 5 shows the model of the FE/DE stack and the charge distribution upon the application of a positive external voltage (V_{TOT}). If there is no leakage current, the charge in the DE layer (Q_{DE}) is always the same as the charge in the FE layer (Q_{FE}). But as discussed above, this no leakage-current assumption is not valid, since Q_{FE} can be much larger than the maximum Q_{DE} at DE breakdown. Therefore, the leakage current through the DE layer is unavoidable. Here, E_{effect} is defined as a critical electric field. For simplicity, E_{effect} is assumed to be a constant without thickness dependence. There is negligible leakage current below the E_{effect}, and above the E_{effect}, the leakage current exists. The charge carried by the leakage current will be trapped at the FE/DE interface as Q_{it}. In the equilibrium condition, there is no charge transfer process with zero current. As a result, the electric field in the DE layer will be pinned at the E_{effect}, so that

$$Q_{DE} = \epsilon_{DE}E_{effect} \tag{10}$$

The charge balance equation becomes

$$Q_{FE} = Q_{DE} + Q_{it} \tag{11}$$

As we can see, it is critical to have enough Q_{it} from leakage current to obtain a high Q_{FE}. So, the polarization switching process must be leakage-assist-switching. Eqs 10 and 11 are the key formulas in the simulation of the $P-V$ hysteresis loop of the FE/DE stack.

Figure 6(a) shows the simulation of the minor loops of the FE HZO capacitor based on numerical fitting to the experimental

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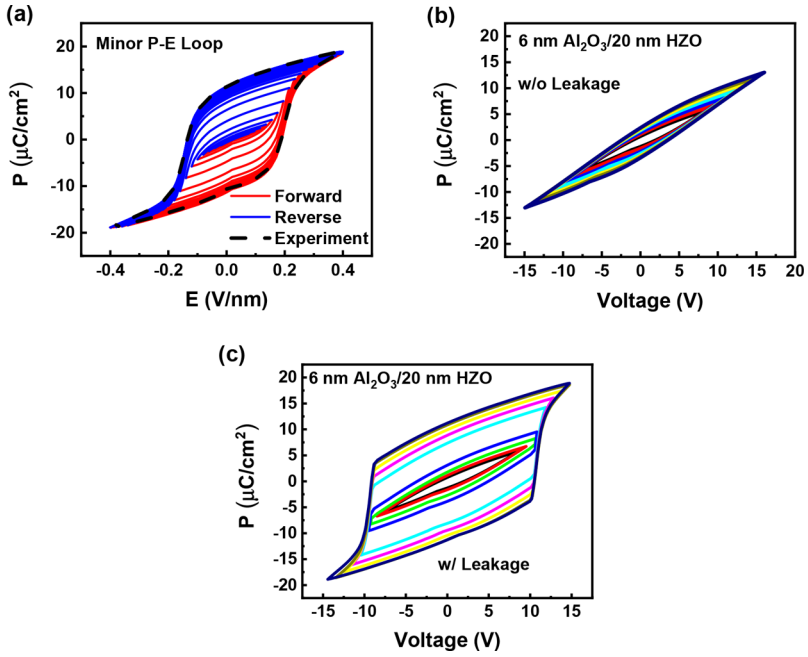

Figure 6. (a) Simulation of minor loops in an FE HZO capacitor. (b) Simulation without leakage current of $P-V$ hysteresis loops in a 6 nm Al_2O_3/20 nm HZO capacitor at different voltage sweep ranges. (c) Simulation with leakage current of $P-V$ hysteresis loops in a 6 nm Al_2O_3/20 nm HZO capacitor at different voltage sweep ranges.

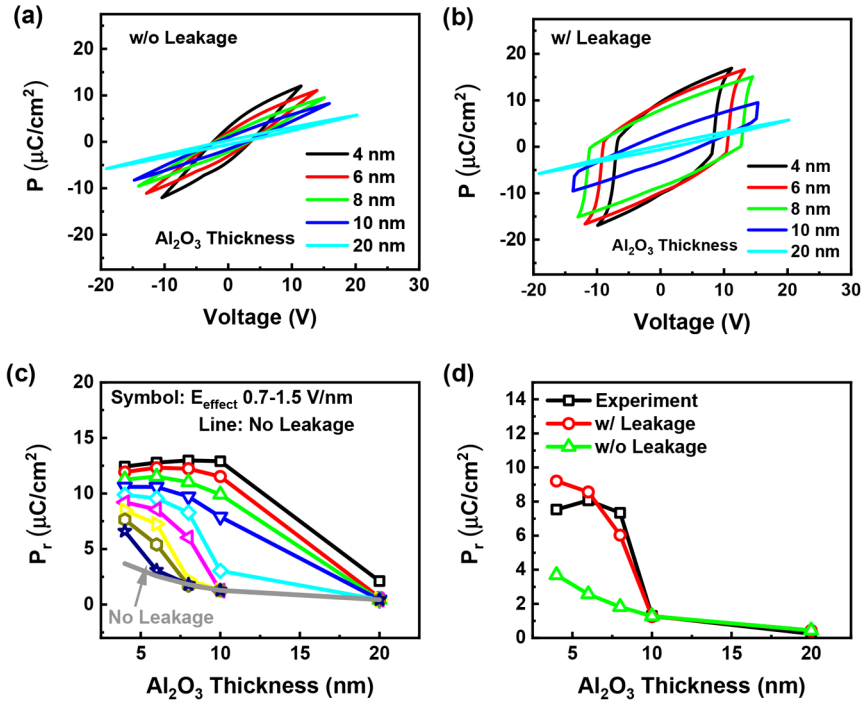

Figure 7. Simulation (a) without leakage current and (b) with leakage current of $P-V$ hysteresis loops of FE/DE capacitors with 20 nm HZO and different Al_2O_3 thicknesses. (c) Remnant polarization versus Al_2O_3 thickness on both without leakage-current and with leakage-current assumptions at different E_{effect}. (d) Comparison of experimental results on P_r vs Al_2O_3 thickness with simulation results, with and without leakage-assist switching.

$P-E$ curve. If there is not enough charge from Q_{it} and Q_{DE}, the FE layer always exhibits a minor loop with less P_r. Figure 6(b) shows the simulation of the $P-V$ hysteresis loops in a 6 nm Al_2O_3/20 nm HZO capacitor at different voltage sweep ranges, assuming no leakage current. Figure 6(c) shows the simulation of the same structure but using the leakage-assist-switching model with leakage current from the DE layer. It is obvious that a significantly larger P_r is obtained. The experimental $P-V$ hysteresis loops in a 6 nm Al_2O_3/20 nm HZO capacitor (Figure 4(c)) with certain level of unavoidable leakage current match well with the leakage-assist-switching model presented in Figure 6(c).

The thickness of the DE layer, thus the leakage current, has a significant impact on the ferroelectricity of the FE/DE stack as

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studied experimentally. The leakage-assist-switching model can also simulate the thickness-dependent behavior. Figure 7(a) shows the simulation of the $P-V$ hysteresis loop of the FE/DE stack with 20 nm HZO and different Al_2O_3 thicknesses, assuming no leakage current. Figure 7(b) shows the simulation of the same structure but using the leakage-assist-switching model. The specific voltage sweep ranges are selected according to the experimental results, as shown in Figure 4(b). Modeling and experiments are in great agreement. The model also successfully predicts the loss of P_r in the FE/DE stack with a thick DE layer because of the voltage division and no leakage current. Figure 7(c) shows the P_r versus thickness comparison in the without leakage model and with leakage model with different E_{effect}, suggesting the FE/DE stack with a leakier DE layer can have a larger P_r. Figure 7(d) compares the experimental results on P_r vs Al_2O_3 thickness with simulation results, showing the leakage-assist-switching model matches well with experimental results in terms of thickness dependence. The above results provide new insights to understand the large amount of reported experimental results in NC-FETs usually with FE/DE stacks. FE and FE/DE are fundamentally different in terms of coercive field, P_r, switch speed, and many others.

The impact of internal metal is studied by comparing type C and type D capacitors (see Supplementary Section 1). The FE/DE stacks with internal metal and without internal metal are physically very different. If the internal metal gate becomes the externally connected metal wires or the internal metal gate is physically connected to measurement equipment, the required balanced charges can be provided even externally. All these facts are extremely important to understand and interpret the experimental observation related to Fe-FETs and NC-FETs. The so-called interfacial coupling effect or capacitance enhancement was observed in previous reports.[19,27−30] This interfacial coupling effect can improve the equivalent oxide thickness of an FE/DE gate stack, which is also observed in the HZO/Al_2O_3 FE/DE stack as shown in Supplementary Section 2. The above understanding of ferroelectric switching process helps to just apply ferroelectric polarization switching (sometimes calls transient negative capacitance effect) to explain the DC enhancement of ferroelectric-gated transistors without invoking the QSNC concept (see Supplementary Section 3). The operation speed of such transistors could be eventually limited by the ferroelectric switching speed,[31] which needs to be thoroughly investigated still.

CONCLUSION

In summary, the ferroelectric polarization switching in FE HZO in the HZO/Al_2O_3 FE/DE stack is investigated systematically by $C-V$ and $P-V$ measurements. The thickness of the dielectric layer is found to have determinant impact on the ferroelectric polarization switching of HZO. The suppression of ferroelectricity is observed with a thick linear dielectric layer. In the gate stacks with thin dielectric layers, a full polarization switching of the ferroelectric layer is found possible by the proposed leakage-current-assist mechanism through the ultrathin dielectric layer. The numerical simulation using the leakage-assist-switching model matches very well with the experimental results.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsaelm.9b00092.

Additional details for the impact of internal metal, interfacial coupling, and the DC enhancement of Fe-FETs (PDF)

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Author Contributions

P.D.Y. conceived the idea of the FE/DE stack and supervised the experiments. M.S. and X.L. did the ALD deposition and device fabrication. M.S. and X.L. performed DC electrical measurements and analysis. M.S. did the numerical simulation. P.D.Y. and M.S. proposed the idea of DC enhancement on Fe-FETs. M.S. and P.D.Y. cowrote the manuscript, and all authors commented on it.

Notes

The authors declare no competing financial interest.

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