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ARTICLE

Nanometer-Thick Oxide Semiconductor Transistor with Ultra-High Drain Current

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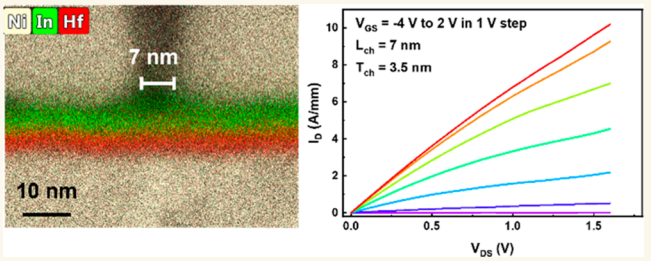
ABSTRACT: **High drive current is a critical performance parameter in semiconductor devices for high-speed, low-power logic applications or high-efficiency, high-power, high-speed radio frequency (RF) analogue applications. In this work, we demonstrate an In_2O_3 transistor grown by atomic layer deposition (ALD) at back-end-of-line (BEOL) compatible temperatures with a record high drain current in planar FET, exceeding 10 A/mm, the performance of which is 2−3 times better than all known transistors with semiconductor channels. A high transconductance reaches 4 S/mm, recorded among all transistors with a planar structure. Planar FETs working ballistically or quasi-ballistically are exploited as one of the simplest platforms to investigate the intrinsic transport properties. It is found experimentally and theoretically that a high carrier density and high electron velocity both contribute to this high on-state performance in ALD In_2O_3 transistors, which is made possible by the high-quality oxide/oxide interface, the metal-like charge-neutrality-level (CNL) alignment, and the high band velocities induced by the low density-of-state (DOS). Experimental Hall, *I*−*V*, and split *C*−*V* measurements at room temperature confirm a high carrier density of up to 6−7 × 10^{13} /cm^2 and a high velocity of about 10^7 cm/s, well-supported by density functional theory (DFT) calculations. The simultaneous demonstration of such high carrier concentration and average band velocity is enabled by the exploitation of the ultrafast pulse scheme and heat dissipation engineering.**



KEYWORDS: *atomic layer deposition, oxide semiconductor, ultrahigh current, back-end-of-line compatibility, charge neutrality level, nanometer-thick transistor*

Looking for a transistor with a higher drain current (I_D) at low voltages has been a key pursuit in the development of modern semiconductor devices. The high drain current is essential for high-speed, low-power logic applications for microelectronics and high-efficiency, high-power, high-speed applications for radio frequency (RF) power electronics. The criteria for achieving a transistor with high I_D is rather straightforward because I_D is determined by the product of carrier density (n_{2D}) and average velocity.[1] However, the demonstration of simultaneous high carrier density and high velocity has been difficult with the maximum I_D ($I_{D,max}$) of reported semiconductor devices reaching 1−2 A/mm with Si,[1] 3−4 A/mm with GaN,[2] and 5 A/mm with graphene[3] (although graphene does not have a bandgap and therefore cannot be regarded as a semiconductor). The control of mobile carriers in conventional semiconductor devices is achieved by carrier accumulation at the oxide/semiconductor interface for enhancement-mode devices or carriers doped in the channel for depletion-mode devices. In this case, the maximum supported n_{2D} is determined by $2E_{BD}\epsilon_{ox}\epsilon_0/q$, where E_{BD} is the breakdown electric field of the gate oxide, ϵ_{ox} is the dielectric constant, ϵ_0 is the vacuum permittivity, and q is the elementary charge. For example, ALD HfO_2 has a typical breakdown electric field of 0.5 V/nm and a dielectric constant of 15 (calculated from Figure S3d in the Supporting Information), leading to a maximum carrier density of about 8 × 10^{13} cm^{-2}. However, in practical devices, such high carrier densities are difficult to achieve due to the U-shape distribution of interface traps in the bandgap and consequently a reduced gate capacitance C_G.[4] As a result, the experimental n_{2D} for practical inversion-mode Si devices is about 2 × 10^{13} /cm^2, which is much lower than the ideal case. Moreover,

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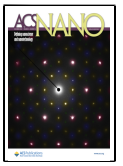

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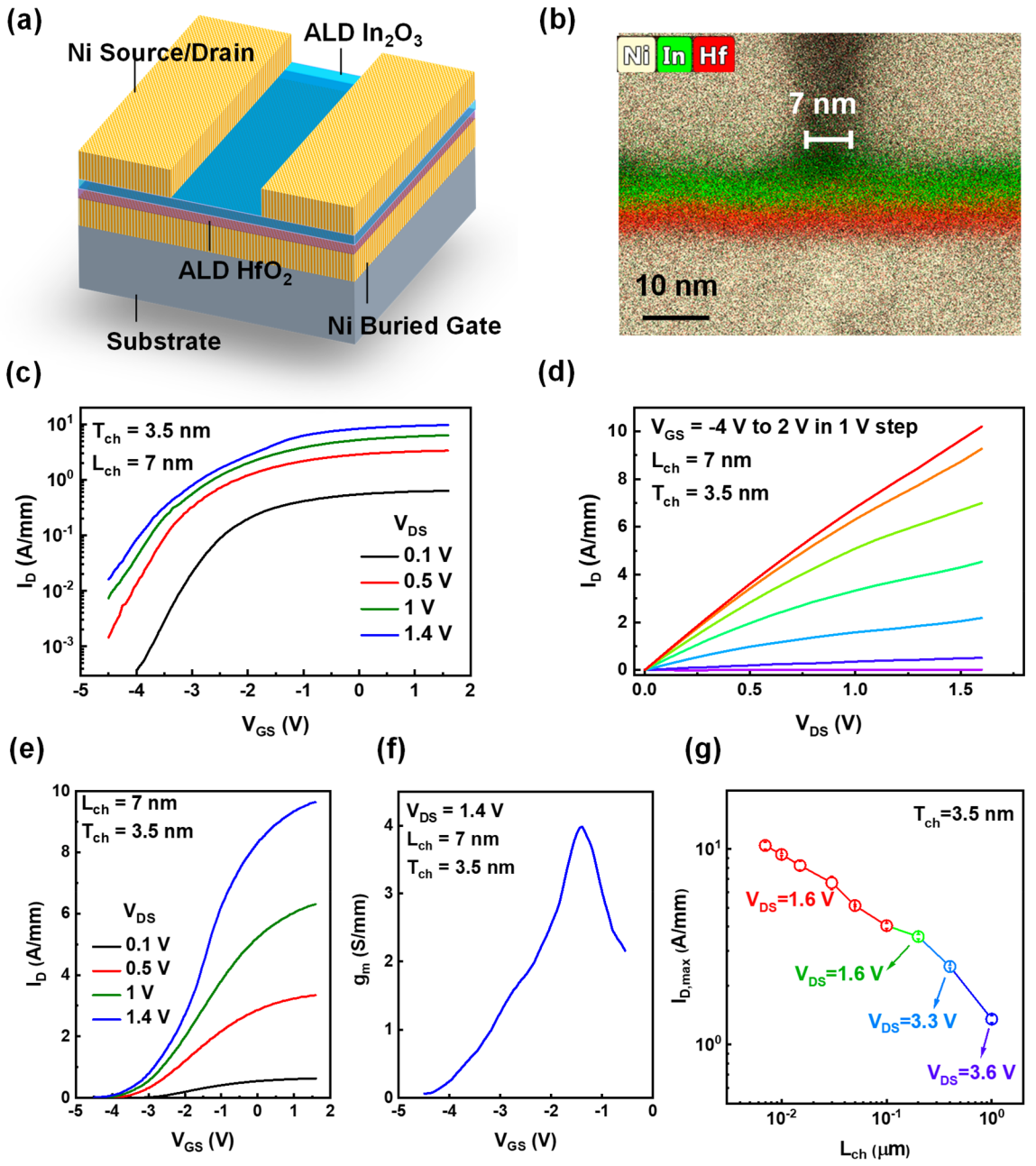

Figure 1. Characterization and performance of scaled ALD In_2O_3 transistors. (a) Schematic diagram of an ALD In_2O_3 transistor. (b) HAADF-STEM cross-sectional image with EDX element mapping of an In_2O_3 transistor with L_{ch} of 7 nm, T_{ch} of 3.5 nm, and 3 nm HfO_2 as the gate insulator. (c) I_D−V_{GS} in log scale and (d) I_D−V_{DS} characteristics of a representative ALD In_2O_3 transistor with L_{ch} of 7 nm and T_{ch} of 3.5 nm. The device exhibits high a I_D exceeding 10 A/mm. (e) I_D−V_{GS} characteristics in linear scale and (f) g_m−V_{GS} characteristics at V_{DS} of 1.4 V of the same device, showing a maximum g_m of 4 S/mm. From (d) and (e), n_{2D} is estimated to be ~7.6 × 10^{13}/cm^2 using $n_{2D} = C_G(V_{GS} - V_T)$. Details are seen in Figure S3 in the Supporting Information. (g) $I_{D,max}$ scaling metrics of ALD In_2O_3 transistors with statistics. Each point represents an average of at least five devices.

because the electrons at lower concentration averagely occupy lower energy states in the conduction band, a reduced n_{2D} decreases average carrier velocity, which will be discussed later in this work. Such an effect reversely boosts the performance of device with a high n_{2D}, which is amplified in semiconductor materials having a single conduction band with low density of states (DOS).

Oxide semiconductor thin-film transistors are a mature technology in flat-panel display applications[5−7] and are considered promising high-performance devices for back-end-of-line (BEOL) compatible monolithic 3D integration.[8−11] Recently, an atomic layer deposition (ALD) based indium oxide (In_2O_3) transistor has been reported, featuring an atomically thin channel down to 0.5 nm and a high field-effect mobility (μ_{FE}) over 100 cm^2/V·s, enabled by an atomically smooth surface and a charge neutrality level (CNL) located above the conduction band edge (E_C) for low resistance contacts.[12−18] The oxide/insulator and oxide/semiconductor interfaces were found to have a low D_{it}, resulting in a subthreshold slope (SS) down to 63.8 mV/dec at room temperature.[13] Note that, although the SS of III−V compound semiconductor transistors can also reach near 60 mV/dec, such

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a low D_{it} of these materials is located in their subthreshold regions. As a result, n_{2D} is still strongly affected by D_{it} in the on-state due to the U-shape distribution of interface traps. Therefore, considering the CNL alignment above E_C, ideal oxide−oxide interface, and U-shape distribution of interface traps, an ALD In_2O_3 transistor is expected to have low D_{it} in the on-state, leading to a high carrier density and high electron velocity in scaled transistors simultaneously. Although the authors reported an ON-state drain current over 3 A/mm in a scaled ALD In_2O_3 transistor with L_{ch} of 8 nm and V_{DS} of 0.5 V,[17] a higher drain bias quickly leads to instability of the device due to its self-heating effect. Meanwhile, a comprehensive understanding of the superior transport nature of ALD semiconducting In_2O_3 is urgently needed, since works toward the outstanding conducting properties of ALD In_2O_3, especially the recent ultrahigh current over 20 A/mm in gate-all-around (GAA) nanoribbon FETs achieved by authors,[18] are widely reported without the origin being elucidated yet.

In this work, we report an ALD In_2O_3 transistor with a scaled channel length (L_{ch}) down to 7 nm, achieving a high $I_{D,max}$ exceeding 10 A/mm in planar structure, which is 2−3 times higher than the best known semiconducting materials such as Si, GaN, InGaAs, graphene, etc., second only to GAA In_2O_3 FETs. A high transconductance (g_m) of 4 S/mm is also realized, higher than all known transistors with a planar structure. The utilization of a fast pulse measurement scheme and heat engineering enables measuring such a high drain current density. Such ultrascaled planar transistors serve as one of the simplest platforms to investigate the transport nature of such thin-film semiconductors. We conclude that this high on-state performance is attributed to the simultaneous high carrier density of up to 6−7 × 10^{13} /cm^2 and the high velocity of about 10^7 cm/s, confirmed experimentally by Hall, I−V, and split C−V measurements at room temperature, as well as supported by density functional theory (DFT) calculations. We also elucidate theoretically that a low effective mass, single conduction band composed of mostly s-orbital character results in a low DOS that gives rise to a high average electron energy and high average band velocity. The low contact resistance/resistivity induced by the unique CNL alignment of the metal/In_2O_3 interface in the conduction band and the high-quality oxide−oxide interface with low D_{it} are another two factors for a high drain current.

RESULTS AND DISCUSSION

Figure 1a illustrates this work's schematic diagram of the ALD In_2O_3 transistors in this work. The devices comprise a 3 nm-thick HfO_2 gate insulator, an ALD In_2O_3 channel with a thickness (T_{ch}) from 2.5 to 3.5 nm, and Ni used as the gate electrode and the source/drain contacts. The details about device fabrication are discussed in the Methods section. Figure 1b shows the high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) cross-sectional image with energy-dispersive X-ray spectroscopy (EDX) to highlight the Ni/In/Hf elements in a representative In_2O_3 transistor with L_{ch} of 7 nm and T_{ch} of 3.5 nm. The channel width (W_{ch}) is defined as 2 μm by ICP dry etching, except for devices with L_{ch} below 30 nm, which have a narrower W_{ch} of 600 nm to dissipate heat more efficiently. Figure S1 in the Supporting Information shows an SEM image from the top view of a transistor with a L_{ch} of 100 nm and a W_{ch} of 2 μm defined by dry etching, illustrating the device structure. Parts c and d of Figure 1 present the I_D−V_{GS} and I_D−V_{DS} characteristics obtained by pulsed I−V measurements. A pulse width of 90 ns is utilized (unless otherwise specified) to suppress self-heating effects from the ultrahigh drain current so that the intrinsic electron transport properties of the devices can be probed, as described in the Methods section. Here, a high $I_{D,max}$ of 10.2 A/mm is achieved at V_{GS} = 1.5 V (V_{GS}−V_T = 4.3 V, where V_T is extracted at low V_{DS} by linear extrapolation) and V_{DS} = 1.4 V, which, although with a planar structure, 2−3 times outperforms any best-reported $I_{D,max}$ from devices with other semiconducting materials of any FET structure, including graphene. This output performance is only second to a GAA FET with the same ALD In_2O_3 channel material. Parts e and f of Figure 1 show the I_D−V_{GS} on a linear scale and the g_m−V_{GS} characteristics with V_{DS} of 1.4 V, both for the same device. A high g_m of 4 S/mm for a V_{DS} of 1.4 V is achieved, which is also higher than all known planar semiconductor devices. The total resistance of 140 Ω·μm means an ultralow R_C less than 70 Ω·μm, originating from the CNL at the Ni/In_2O_3 interface aligning deep inside the conduction band.[14,16] The survival of 3 nm HfO_2 at such high voltages is attributed to the voltage drop in the depleted In_2O_3 and to the ultrashort stress time during pulse measurements. The I_D−V_{GS}, I_D−V_{DS}, and g_m−V_{GS} characteristics of a device with the same gate stack and L_{ch} of 100 nm are shown in Figure S2 in the Supporting Information, which shows a high $I_{D,max}$ of 4.1 A/mm and a high g_m of 1.3 S/mm even with this relatively long channel. The visually low ON/OFF ratio and large SS originate from the impact of gate leakage in the OFF state and background noise (∼ μA) from the ultrafast pulse characterization setup, as discussed in Figure S5 in the Supporting Information. Gate leakage also gives rise to a visually large DIBL. The actual DIBL of a transistor with L_{ch} of 100 nm, determined by V_T from linear extrapolation, is as small as 23.5 mV/V, as shown in Figure S2c in the Supporting Information. The same characteristics of a long channel device with L_{ch} of 1 μm are presented in Figure S3 in the Supporting Information, showing clear current saturation. The high on-state performance is attributed to the high electron density and high velocity of ALD In_2O_3, coupled with low contact resistance. Moreover, the wide bandgap of 3.0 eV in In_2O_3 makes it possible to sustain the high estimated lateral electric fields of ∼2 MV/cm (V_{DS} = 1.4 V and L_{ch} = 7 nm). Similar electrical characterization of devices with T_{ch} of 2.5 nm are also presented in Figure S4 in the Supporting Information. The $I_{D,max}$ scaling metrics with a L_{ch} from 1 μm down to 7 nm of In_2O_3 transistors are shown in Figure 1f with statistics, demonstrating the wafer-scale uniformity of ALD growth. The $I_{D,max}$ is the maximum drain current under stable conditions, obtained by pulse measurements.

Toward the importance of reliability for any electronic devices, ultrascaled ALD In_2O_3 transistors survive under such high current and power, primarily thanks to a short stress time and hence the much longer cooling period between two pulses, as illustrated in Figure S13 in the Supporting Information. Systematic works on thermal engineering to improve heat dissipation, including interface thermal conductivity engineering[19] and development of high thermally conductive and electrically isolating buffer layer between BEOL layer and front-end-of-line (FEOL) layer, are strongly needed to ensure the operation at such a high on-state level. Positive bias stress tests were also performed on ultrascaled devices with different V_D bias at a constant stress of V_G−V_T = 4.3 V and presented in

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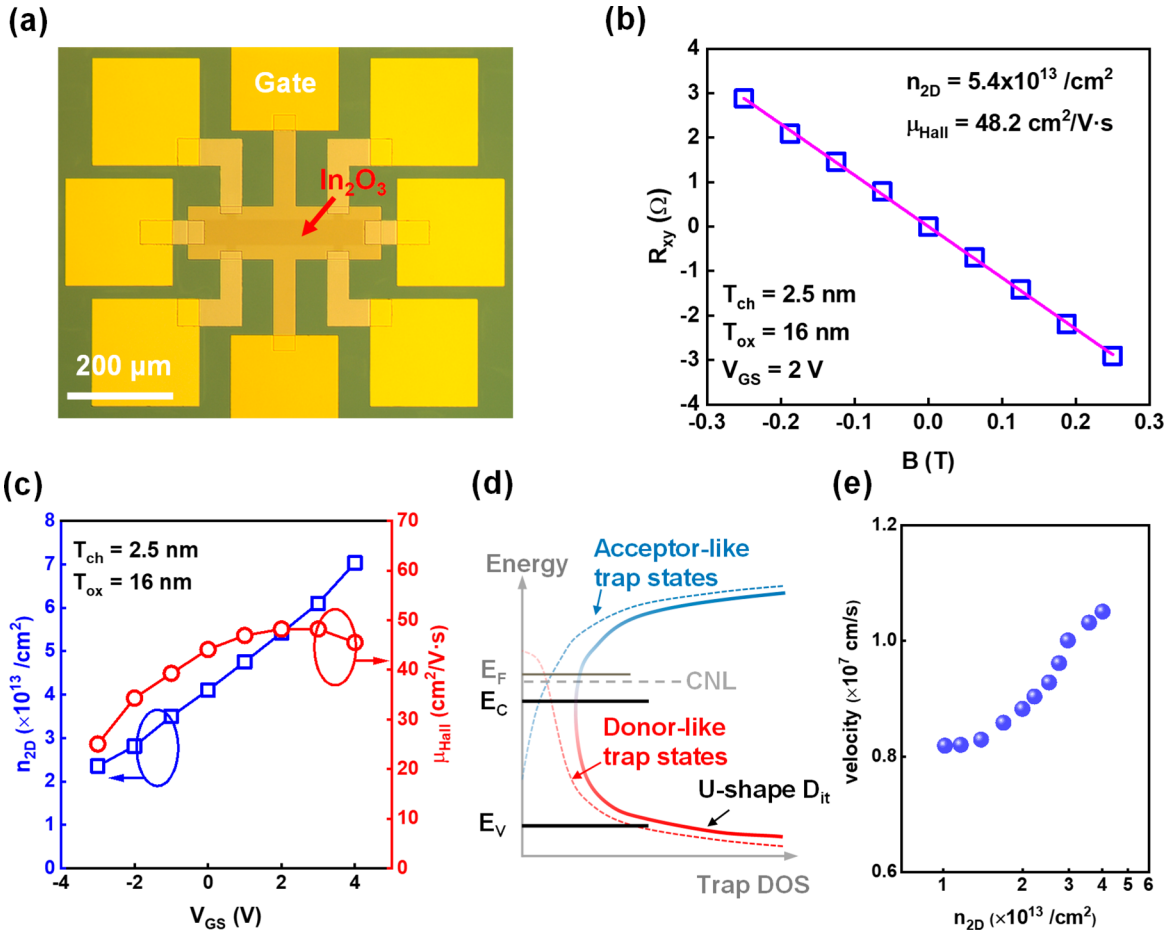

Figure 2. Carrier density and velocity in ultrathin ALD In_2O_3. (a) Photo image of a Hall bar device with a back-gate structure with 16 nm HfO_2 as the gate insulator and 2.5 nm In_2O_3 as the channel semiconductor. Hall devices underwent the same thermal treatment process. A thick oxide is used here to avoid the impact of the gate leakage current. (b) Hall measurement of R_{xy} versus B field with the gate electrode at 2 V. n_{2D} of 5.4 × 10^{13} /cm^2 and μ_{Hall} of 48.2 cm^2/V·s are achieved. (c) n_{2D} and μ_{Hall} versus V_{GS} characteristics for V_{GS} from −3 to +4 V. (d) CNL or TNL alignment in ALD In_2O_3 with U-shape D_{it} distribution. (e) Velocity versus n_{2D} extracted from the I_D−V_{GS} characteristics in Figure 1 and carrier density from Hall measurements.

Figure S6 in the Supporting Information, demonstrating the device's reasonable stability even under high bias.

To understand the origin of the observed high current in ALD In_2O_3 transistors, the carrier density and velocity are characterized by Hall, I−V, and split C−V measurements at room temperature. Figure 2a shows a photo image of the experimental Hall bar device, with a similar Ni/HfO_2/In_2O_3/Ni gate stack, having undergone the same thermal treatment process as the ALD In_2O_3 transistors. To minimize the impact of gate leakage current, a thickness of 16 nm HfO_2 is used in the Hall measurements. Figure 2b shows the R_{xy} versus B field characteristics with T_{ch} of 2.5 nm. A n_{2D} of 5.4 × 10^{13} /cm^2 and Hall mobility (μ_{Hall}) of 48.2 cm^2/V·s are achieved. Figure 2c shows the V_{GS}-dependent n_{2D} and μ_{Hall}. A maximum n_{2D} of 7 × 10^{13} /cm^2 is obtained, which can be depleted or modulated by gate voltage and is significantly higher than other semiconducting materials such as Si, GaN, etc. The high n_{2D} is very close to the maximum charge density supported by HfO_2 as calculated above, indicating a high-quality oxide/oxide semiconductor interface without significant trapped charges at the Fermi level. Figure S8 in the Supporting Information presents a typical I_D−V_{GS} curve of an ALD In_2O_3 transistor with T_{ch} of 1.2 nm, L_{ch} of 800 nm, and 5 nm HfO_2 thickness, showing a steep subthreshold slope (SS) of 63.5 mV/dec corresponding to a D_{it} of 6 × 10^{11} cm^{-1}·eV^{-1}, suggesting a high-quality HfO_2/In_2O_3 interface. The SS in Figure 1c of 612.5 mV/dec is much larger due to the relatively thick channel designed to achieve high drain current, but the D_{it} at the HfO_2/In_2O_3 interface is expected to be similar and independent of channel thickness because of the similar atomic configuration at the interface. More importantly, the maximum charge density is not limited by the high D_{it} in the tail of the U-shape distribution as with conventional metal-oxide-semiconductor (MOS) devices like InGaAs. This is because In_2O_3 has a CNL about 0.4 eV above the E_C, so the D_{it} in the on-state is expected to be even lower than in the subthreshold region, as shown in Figure 2d. Thus, with ALD In_2O_3 transistors containing an oxide/oxide interface, the capability of carrier density modulation by gate oxide is much higher than those with a conventional III−V oxide/semiconductor interface. The high carrier density is also further verified by split C−V measurements as shown in Figure S9 in the Supporting Information.

I_D can be calculated simply by the product of charge density and average velocity. Because of the ultrascaled channel length of 7 nm compared to the estimated mean free path for backscattering of roughly 8 nm in In_2O_3 (see Figure S7 in the Supporting Information), the average velocity is estimated to be the ballistic injection velocity. Using the transfer character-

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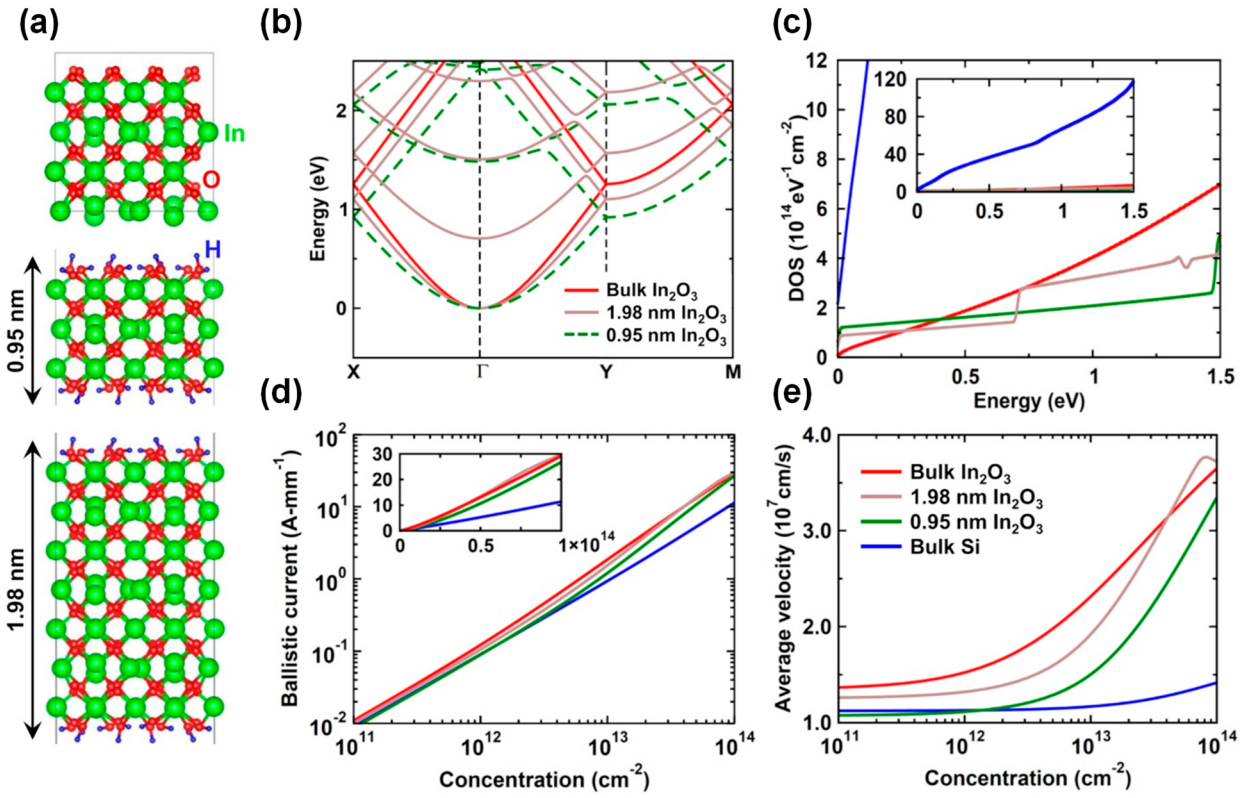

Figure 3. First-principles simulations of In_2O_3. (a) Atomic structure of bulk In_2O_3 (top), 0.95 nm-thick In_2O_3 (middle), and 1.98 nm-thick In_2O_3 (bottom). (b) Calculated band structure of bulk and nanoscale In_2O_3. (c) Comparison of DOS versus electron energy (relative to the band edge) between In_2O_3 and Si. In_2O_3 presents a much lower DOS such that, for a given carrier density, electrons in In_2O_3 have much higher energy than those in Si. (d) Ideal ballistic current versus electron concentration. At high concentrations, In_2O_3 can carry significantly more current than Si. (e) Average (ballistic injection) velocity versus electron concentration in In_2O_3 and Si. In_2O_3 presents higher average velocitiy because of its lower DOS and higher band velocities. For panels (c) and (d), the properties of bulk In_2O_3 and bulk Si are obtained assuming a thickness of 3.5 nm.

istics in Figure 1c for I_D and the Hall measurements in Figure 2c for n_{2D}, a high electron velocity in the range 0.85−1.05 × 10^7 cm/s is obtained at high n_{2D} and shown in Figure 2e. This electron velocity might still be underestimated because nonideal effects, such as contact resistance, short channel effects, etc., are not considered, suggesting that the electron injection velocity in ALD In_2O_3 transistors can be even higher. Such a high carrier density and velocity have contributed to a high $I_{D,max}$ over 10 A/mm, which is significantly higher than those of other state-of-the-art semiconductor devices.

To elucidate the nature of the simultaneous existence of the high n_{2D} and high velocity in In_2O_3, density functional theory (DFT) calculations of the electronic properties were conducted (see the Methods section for details). Figure 3b shows the band structure of bulk In_2O_3 and three In_2O_3 2D slabs with thicknesses of 3.52, 1.98, and 0.95 nm; the corresponding atomic structures are presented in Figure 3a. In all cases, there is a single nearly isotropic conduction band located at the zone center, composed of mostly In s-orbital character, with effective masses of 0.17 m_0 (bulk), 0.19 m_0 (3.52 nm slab), 0.23 m_0 (1.98 nm slab), and 0.30 m_0 (0.95 nm slab). A key feature of the band structure is the absence of higher-energy secondary bands until well above 0.5 eV relative to the conduction band edge. Figure 3c shows the DOS of bulk In_2O_3 with an assumed thickness of 3.5 nm, the three In_2O_3 slabs, and for comparison bulk Si with an assumed thickness of 3.5 nm. In_2O_3 displays a much smaller DOS than Si, due to its lower effective mass and single conduction band (the DOS effective mass of bulk In_2O_3 is 0.17 m_0 compared to 1.06 m_0 for bulk Si). Thus, for a given n_{2D}, the Fermi level is located deeper inside the conduction band of In_2O_3 compared to Si. For example, a carrier density of 5 × 10^{13} /cm^2 corresponds to a Fermi level of roughly 0.5 and 0.1 eV above the band edge for bulk In_2O_3 and Si, respectively, as seen in Figure S10 in the Supporting Information. Moreover, from Figure S10, one finds that the smaller effective mass of In_2O_3 results in a higher average band velocity at a given energy. From the DFT band structure, the ideal ballistic current is computed versus n_{2D} and shown in Figure 3d. This current represents an ideal upper limit for a short-channel device in which transport is ballistic, the current is controlled by injection from the source contact only ($V_{DS} \gg k_BT/q$), and there is no potential barrier. With In_2O_3, the minimum carrier concentration needed to achieve a current of 10 A/mm is 2 × 10^{13} /cm^2, while with Si, a carrier concentration near 5 × 10^{13} /cm^2 is required. To understand why In_2O_3 can carry a larger current than Si, the ballistic injection velocity is obtained from the ratio of the ideal ballistic current over the charge density, which is plotted in Figure 3e. The velocities of In_2O_3 are significantly higher than Si, particularly for large n_{2D}. For 5 × 10^{13} /cm^2, In_2O_3 shows velocities ranging from 3.4 × 10^7 cm/s (0.95 nm slab) to 3.7 × 10^7 cm/s (1.98 and 3.52 nm slabs) compared to 1.4 × 10^7 cm/s with Si. The origin of this 2−3 times velocity enhancement is traced back to In_2O_3 having a single conduction band with

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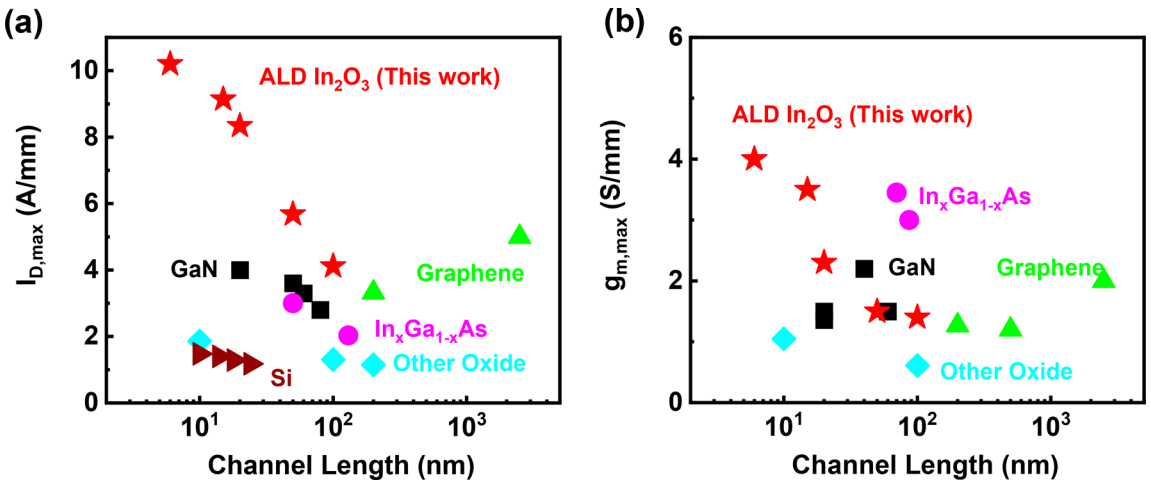

Figure 4. Benchmarking of ALD In_2O_3 with other semiconductor materials. Comparison of (a) $I_{D,max}$ and (b) g_m versus channel length characteristics with other high-performance semiconductor materials and graphene. Transistors with ALD In_2O_3 demonstrate the largest I_D and g_m compared to all known semiconductors with a planar structure due to the high carrier density and high velocity.

relatively low effective mass, leading to a combination of higher band velocities and a Fermi level located deep in the band where electrons sample higher energy states. In_2O_3 also benefits from its secondary bands being high enough in energy to not play a significant role in transport, which would otherwise lower the average electron velocity and energy. The difference in velocity between experiments and the DFT calculations primarily comes from the fact that the simulation is based on single-crystal In_2O_3 and perfect ballistic transport.

Therefore, the two major contributors to the high $I_{D,max}$ in ALD In_2O_3 transistors are high carrier density and high velocity, with the former originating from the high-quality oxide/oxide interface and a metal-like CNL alignment and the latter arising from the low DOS and high-carrier-induced velocity enhancement. Moreover, the ALD In_2O_3 transistors are aided by low contact resistances and the wide bandgap of In_2O_3 for laterally scaled channel lengths. The above first-principles calculations are based on a single crystal structure. The crystal structure of the experimental devices is confirmed to be polycrystalline. As shown in the TEM cross-sectional image and X-ray diffraction (XRD) data in Figure S11 in the Supporting Information, unannealed ALD In_2O_3 is amorphous, while annealed ALD In_2O_3 at 275 °C in O_2 for 60 s, the same process condition for device fabrication, is polycrystalline. It would be natural to assume that the charge transport has much more scatterings in the polycrystalline boundaries and that carrier mobility (velocity) might be reduced significantly. However, our DFT calculations on polycrystalline In_2O_3 reveals that there is a possible mobility enhancement effect such that polycrystalline and single crystalline In_2O_3 could have similar charge transport behavior and comparable electron mobility and velocity, as supported by Figure S12 in the Supporting Information.

Parts a and b of Figure 4 present the benchmark of $I_{D,max}$ and g_m versus channel length of selected high performance-semiconductor devices with different channel materials. ALD In_2O_3 displays an $I_{D,max}$ that is 2−3 times better than the best-reported transistors with different channel materials, including Si, InGaAs, GaN, graphene, etc., and also demonstrates the best g_m compared to all other semiconductor materials with a planar device structure, due to the simultaneous high carrier density and high velocity. Data used in this work are summarized in Table S1 in the Supporting Information.[2,3,8,11,20−30]

CONCLUSIONS

In summary, an ALD In_2O_3 transistor with a record high $I_{D,max}$ exceeding 10 A/mm is reported, which, even achieved in planar structure, is 2−3 times higher than that of other known semiconductor devices. It is found experimentally and theoretically that high carrier densities, resulted from the high-quality oxide/oxide interface and a metal-like CNL alignment, and high carrier velocities, originating from the low DOS and high-carrier-induced velocity enhancement from a low effective mass and a single conduction band, are the two major contributors to the high $I_{D,max}$ in ALD In_2O_3 transistors. Hall, $I-V$, and split $C-V$ measurements at room temperature confirm a simultaneous high carrier density of up to 6−8 × 10^{13} /cm^2 and a high velocity of about 10^7 cm/s, which is well-supported by density functional theory (DFT) calculations.

METHODS

Device Fabrication. The device fabrication process started with solvent cleaning of the p+ Si substrate with thermally grown 90 nm SiO_2. A bilayer lift-off process was then adopted for the sharp lift-off of 30 nm Ni buried metal gates formed by e-beam evaporation, utilizing photoresist PMGI SF9 + AZ1518 stack, patterned by Heidelberg MLA150 Maskless Aligner. This step is critical to avoid sidewall metal coverage and to enable a high-quality ultrascaled ALD gate dielectric and semiconducting channel. HfO_2 of 3.0 nm as a gate dielectric was grown by ALD at 200 °C using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as Hf and O precursors, respectively. Then, In_2O_3 thin films with various thicknesses were grown by ALD at 225 °C using $(CH_3)_3In$ (TMIn) and H_2O as In and O precursors, respectively. N_2 is used as the carrier gas at a flow rate of 40 sccm. The base pressures are 169 and 437 mTorr at a N_2 flow rate of 0 and 40 sccm, respectively. Concentrated hydrochloric acid was applied for channel isolation. S/D ohmic contacts were formed by e-beam evaporation of 30 nm Ni in two steps to avoid the difficulty of the sub 10 nm lift-off process, as employed before. A two-step e-beam lithography process was performed by the formation of first the source electrode and then the drain electrode, utilizing diluted e-beam resist AR-P 6200 (2.5%), patterned by a JEOL JBX-8100FS E-Beam Writer. Then, inductively coupled plasma (ICP) dry etching using BCl_3/Ar plasma was applied to define the channel width accurately. The

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devices were annealed in O_2 at 275 °C for 1 min to improve the performance.

Material Characterization. The cross-sectional TEM specimens were fabricated by focused ion beam (FIB) using a FEI Helios G4 UX dual beam scanning electron microscope (SEM). Before FIB milling, a platinum (Pt) layer was deposited to protect the surface from ion damage. To remove FIB induced damages, the TEM samples were ion polished using a low current (27 pA) at a low voltage (2 keV) multiple times during the final steps.

Transmission electron microscopy (TEM) analyses and energy-dispersive X-ray spectroscopy (EDX) element mapping were carried out on a Thermo-Fischer FEI Talos 200X TEM microscope operated at 200 kV equipped with a high-angle annular dark field (HAADF) detector and SuperX EDS with four silicon drift detectors. All the EDX maps were captured under the drift correction mode.

Device Characterization. The DC characterization is performed using a B1500A semiconductor device analyzer. The pulse characterization is performed using a B1530A waveform generator/fast measurement unit (WGFMU). The device is grounded at the source, while the drain and gate are connected to two channels of the WGFMU via remote sense/switch units (RSU). A waveform with a pulse delay time (PD) of 2 μs, a rise time (RT) of 60 ns, a pulse width (PW) of 90 ns, and a fall time (FT) of 60 ns is adopted to maximize device reliability while minimizing pulse-induced AC response during measurements. Two channels carry the waveform simultaneously with a chronological difference of less than 1 ns, confirmed with TDS5000 digital phosphor oscilloscopes. Data is collected during an averaging time (AT) of 50 ns after a measurement delay (MD) of 2.1 μs to wait for the signal to stabilize. No bias is applied at each channel during the pulse interval to dissipate generated heat. During output characterization, the amplitude of the V_{DS} pulse increases in 100 mV steps while the amplitude of the V_{GS} pulse remains constant. During transfer characterization, the amplitude of the V_{DS} pulse increases in 50 mV steps while the amplitude of the V_{GS} pulse remains constant. The transfer data is spliced with the on-state data from the pulse characterization while the off-state data comes from the DC characterization, due to the limited signal sensing range of the B1530A WGFMU in the high-current mode (100 μA−10 mA) and the relatively low resolution of the RSUs.

Pulse characterization is critical to alleviate severe self-heating-induced burning and minimize time-dependent dielectric breakdown of the ultrathin gate insulator. The pulse data is in line with the DC data in the low-power range. While DC characterization inevitably causes severe self-heating and consequential device failure, pulse characterization enables repeatable measurements. The details of pulsed $I-V$ measurements and the impact of self-heating effects are shown in Figure S13 in the Supporting Information. All the electrical tests are performed in a standard probe station with a N_2 flow unless stated otherwise.

Theoretical and Computational Details. The density functional theory (DFT) calculations were carried out using the Quantum Espresso (QE) code.[31,32] Optimized norm-conserving Vanderbilt pseudopotentials[31] and the Perdew−Burke−Ernzerhof (PBE)[33,34] exchange-correlation were adopted. A kinetic energy cutoff of 140 Ry and a Monkhorst−Pack[35] Brillouin zone sampling of 6 × 6 × 6 for bulk (primitive cell) In_2O_3 and 3 × 3 × 1 for the 2D slabs of In_2O_3 were used. Crystalline In_2O_3 is body-centered cubic with 40 atoms in the primitive cell.[36] The 80-atom conventional cubic cell was used to generate the 0.95 nm In_2O_3 slab. The indium layer at the boundary of the cell was removed, and the top and bottom oxygen layers were passivated with hydrogen atoms (one hydrogen per oxygen). The same process was used to generate the 1.98 nm slab but starting with a 1 × 1 × 2 supercell of the bulk cubic cell. A vacuum layer of 25 Å was added to both slabs. With bulk silicon, an energy cutoff of 120 Ry and a Brillouin zone sampling of 16 × 16 × 16 (primitive cell) were employed. All atoms and lattice vectors were fully relaxed, with energies and forces converged to 10^{-5} Ry and 10^{-4} Ry/Bohr, respectively. Spin−orbit coupling was not included.[37] The optimized lattice constant of bulk In_2O_3 is 10.30 Å, which is consistent with other studies.[36−39] The in-plane lattice constants for the 1.98 nm slab are 10.28 and 10.32 Å and those for the 0.95 nm slab are 10.26 and 10.36 Å. Bulk Si has an optimized lattice constant of 5.47 Å, which is close to the measured value of 5.43 Å.[38] The calculated band gaps for bulk In_2O_3, the 1.98 nm slab, the 0.95 nm slab, and bulk Si are 0.94, 1.27, 1.88, and 0.61 eV, respectively. The band gaps of bulk In_2O_3 and Si are below the experimental values of 2.7−3.25 eV[39,41−44] and 1.12 eV;[45] however, this study focuses only the conduction states. The effective mass of bulk In_2O_3, equal to 0.17 m_0, is consistent with some reported values.[38−40,46−48]

The Wannier code[49] was employed to generate maximally localized Wannier functions, which were used to calculate electron energies and velocities on the following $\boldsymbol{k}$-grids: 200 × 200 × 200 for bulk In_2O_3 and bulk Si and 200 × 200 × 1 for the In_2O_3 slabs. Calculated quantities include the density of states (DOS), $D(E) = 2\sum_{\boldsymbol{k},n}\delta(E - E_{\boldsymbol{k},n})/\Omega$, the distribution of modes (DOM), $M(E) = (h/2)\sum_{\boldsymbol{k},n}|v_x(k, n)|\delta(E - E_{\boldsymbol{k},n})/\Omega$, and the average velocity along the transport direction (the x-direction), $v_x^+(E) = \sum_{\boldsymbol{k},n}|v_x(k, n)|\delta(E - E_{\boldsymbol{k},n})/\sum_{\boldsymbol{k},n}\delta(E - E_{\boldsymbol{k},n})$,[50] where $E_{\boldsymbol{k},n}$ are the electron eigen-energies for a given wavevector $\boldsymbol{k}$ and band index n, and $v_x(\boldsymbol{k}) = (1/\hbar)\partial E_{\boldsymbol{k}}/\partial k_x$. The carrier concentration and ideal ballistic current are calculated using $n_{2D} = (1/2)\int_{E_c}^{\infty} D(E)f_0(E, E_F)\mathrm{d}E$ and $I_{ball} = (2q/h)\int_{E_c}^{\infty} M(E)f_0(E, E_F)\mathrm{d}E$,[51] where $f_0(E,E_F)$ is the Fermi−Dirac distribution and E_F is the Fermi energy (the factor of 2 in n_{2D} accounts for only half the states being occupied in an ideal ballistic device[52]). The ballistic injection velocity is obtained from $v_{inj} = I_{ball}/(qn_{2D})$. From the experimental Hall data, the average mean free path for backscattering is fitted by (1) finding the location of the Fermi level for which the calculated and measured n_{2D} are the same, (2) calculating the average distribution of modes at that Fermi level, $\langle M\rangle = \int_{E_c}^{\infty} M(E)[-\partial f_0/\partial E]\mathrm{d}E$, and (3) obtaining the average mean free path for backscattering using the relation $\langle\lambda\rangle = (h/2q)\, n_{2D}\, \mu_{Hall}/\langle M\rangle$.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.2c10383.

Figures of SEM and TEM images, performance of ALD In_2O_3 transistors, I_D-V_{GS} characteristics of an ALD In_2O_3 transistor, reliability characterization of short-channel In_2O_3 transistors, calculated mean free path and capacitance of In_2O_3, split $C-V$ measurements, electronic properties of In_2O_3 and Si from DFT, PXRD spectrum, crystal structures, charge transport modelling in ALD In_2O_3 polycrystalline films, schematic diagram of the pulsed $I-V$ measurement setup, and DC measurement and table of performance of representative devices with different semiconductor materials (PDF)

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Author Contributions

P.D.Y. conceived the idea and proposed research. M.S. and Z.L. developed the ALD In_2O_3 thin film deposition and device fabrication process. Z.L. did the device fabrication, electrical measurements, and analysis on thickness and EOT scaling of ALD In_2O_3 devices. A.C. did the split $C-V$ measurements and carried out XRD characterization. V.A. and J.M. performed the first-principles calculations and analysis. Y.H. and K.C. provided the mobility model on poly crystal. M.L. provided insights on ballistic transistors and understanding of device physics. Z.S, Y.Z., and Z.L performed the STEM and EDX measurements. M.S., Z.L, V.A., J.M., and P.D.Y. cowrote the manuscript, and all authors commented on it.

Notes

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