Performance Potential and Limit of MoS_2 Transistors

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MoS_2, a two dimensional layered transition metal dichalcogenide material of Mo atoms sandwiched between two layers of S atoms, has generated considerable interest in recent years for its unusual electronic and optical properties.[1,2] Unlike graphene, atomically thin MoS_2 is a semiconductor with a bandgap from 1.2 eV of bulk MoS_2 to 1.8 eV of monolayer MoS_2, with a mobility in the range of 1–500 $cm^2\ V^{-1}s^{-1}$.[3–5] Moreover, large area MoS_2 growth techniques by CVD have been developed,[6] making it a suitable candidate for practical electronic device applications, such as thin film logic circuits and amplifiers with high gain.[7–9] Fundamental studies on the low field transport properties,[3,10] the metal-semiconductor Schottky contact,[3,5,11–14] structural defect-induced scattering,[15] as well as low frequencies noise mechanisms,[16–20] have been carried out by various groups. However, the overall assessment of technological relevant parameters such as output capability and signal to noise ratio are still lacking, and their limiting factors are yet to be discussed. Previous studies on MoS_2 transistors typically yield output current much smaller than the standard silicon transistor.[1,3] In the process of evaluating the intrinsic electrical properties of MoS_2, large uncertainties exist in the presence of significant extrinsic factors, such as contacts and gating, and more importantly, the lack of systematic studies on a series of transistors with long-term stability through thermal cycles. These factors combined together lead to significant deviations from the intrinsic properties of MoS_2 and inaccurate projection of its performance potential. In order to address these problems, in this paper, we perform systematic studies on its performance limit in the high field transport region and its precision limit determined by the low frequency noise, both of which are the most important factors in future nanoelectronic applications. During the device fabrication, we developed an effective yet stable doping method on arrays of deeply scaled MoS_2 transistors down to 100 nm, and performed low temperature measurement of the above metrics, which exhibit improved electrical characteristics with consistent temperature dependence.

MoS_2 devices studied here are based on a 90-nm SiO_2 back-gated field-effect transistor (FET) configuration, as depicted by the schematic view in **Figure 1**a. The MoS_2 flake was identified and measured by atomic force microscopy (AFM) as shown in Figure 1b,c, the thickness of which is around 6 nm, corresponding to about 9 layers. Details about the doping method and its effect are given in Figure S1 (Supporting Information). Arrays of devices with four different channel lengths from 1 μm down to 100 nm were fabricated by electron beam lithography. All the measurements were conducted in vacuum (≤10^{-5} Torr) to prevent any impact from the environment.[21] **Figure 2**a–b shows the direct current (DC) output characteristics of a representative 100-nm channel MoS_2 FET at 300 and 20 K, with a drain voltage from 0 to 1.5 V and back-gate voltage from –45 to 40 V. Evidently, the current saturation becomes more significant as the temperature decreases, even starting to show the sign of negative differential resistance (NDR) effect which will be discussed in details later. At room temperature, the maximum drain current is 334 μA μm^{-1} for this device, and the highest current among all our seventeen 100-nm devices reaches 550 μA μm^{-1} at room temperature (Figure S2, Supporting Information), which is larger than previous MoS_2 devices reported, including top-gated device with optimized interface engineering.[22] For the device without doping, on-current is only 126 μA μm^{-1} as shown in Figure S1 (Supporting Information). Comparing to on-resistance R_{on} of 13.3 kΩ·μm for the device without doping, the doped device shows a much lower R_{on} of 3 kΩ·μm. When the temperature decreases to 20 K, the drain current of this device further increases by 240% to 800 μA μm^{-1}, which is the highest drive current reported so far on MoS_2 FETs. Although it is achieved at low temperature, this greatly improved metric extends the current carrying capability of thin film MoS_2 transistors much closer to that of the silicon standard. More importantly, it shows the vital roles that extrinsic factors such as doping effects and phonon scatterings play in the MoS_2 transistors, and further optimization from these aspects can have huge impact on device performance. The transfer characteristics at V_d = 1 V from the same device are plotted in Figure 2c. Similarly, a near 240% increase of drain current and transconductance is obtained when the temperature decreases from 300 to 20 K.

Figure 3a shows the R_{on} as a function of temperature at fixed gate voltage V_g = 40 V for two best 100-nm devices, where R_{on} decreases with decreasing temperature. An ultralow R_{on} of 0.83 kΩ·μm at 20 K is obtained for the 100-nm device, which is significantly lower than the previous results in the literatures.[1,3,5,11] The field-effect mobility μ_{FE} is extracted in the linear region of the transfer characteristics according to the following equation: $\mu_{FE} = g_m/(C_g EW)$, where W is the width of the channel, E is the transverse electric field in the channel, and g_m is the transconductance. The temperature dependence of μ_{FE} for four different channel length devices at various temperatures is plotted in Figure 3b, showing a sharp increase when the temperature decreases, which can be attributed

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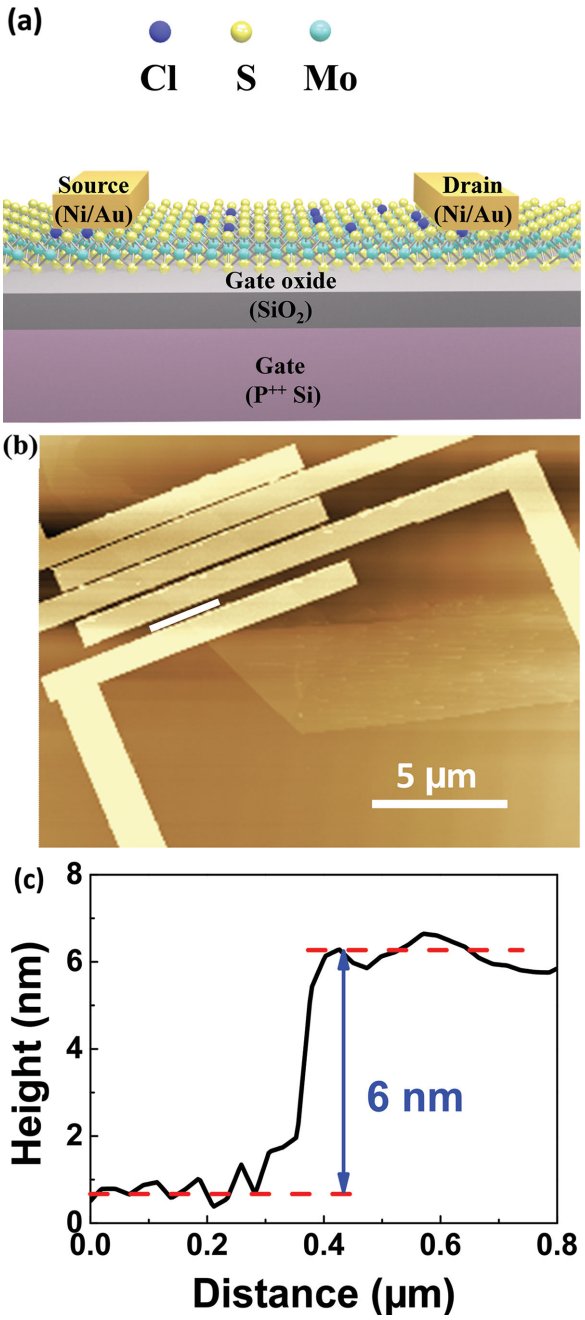

Figure 1. a) Schematic of the MoS_2 back-gate FET fabricated in this work. The gate dielectric is 90-nm SiO_2. The S/D contact metal is Ni (30 nm)/Au (60 nm). b) AFM image of the few-layer MoS_2 FETs on a flake. c) Measured height at the flake edge of a ≈6-nm thick MoS_2 flake by AFM.

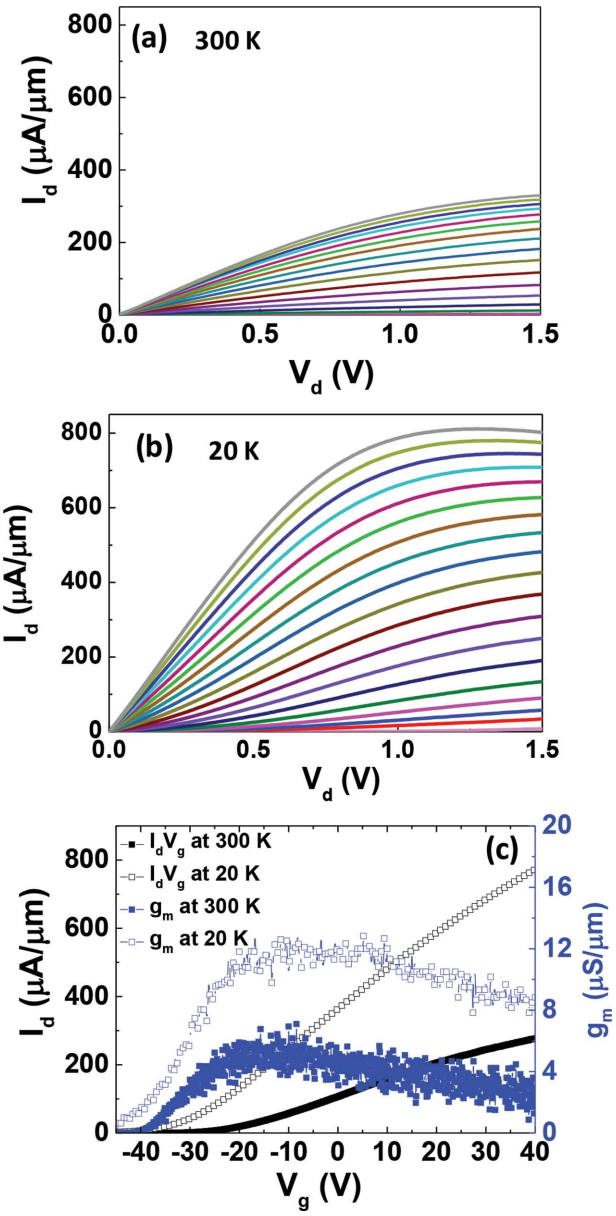

Figure 2. Output characteristics of the 100-nm device at 300 K a) and 20 K b). c) Transfer characteristics of the same device with V_d = 1 V at 300 and 20 K.

to the reduced phonon scattering from the underlying substrate. Moreover, the mobility gradually decreases with scaling channel lengths from 1 μm to 100 nm, which can be attributed to the transconductance degradation due to contact resistance and short channel effect.

In order to further probe the high field transport properties, temperature dependent output characteristics of the 100-nm MoS_2 device at higher drain bias up to 2 V at V_g = 40 V are shown in **Figure 4**a. Interestingly, instead of typical current saturation, the drain current reaches a maximum value at a moderate V_d and then decreases when V_d increases further, exhibiting a significant NDR behavior beyond saturation when current exceeds 400 μA μm^{-1} at high vertical field (V_g = 40 V at 280 K). Figure 4b shows the saturation current degradation $\Delta I/I_{sat}$ and saturation current I_{sat} as a function of temperature, both of which increase monotonically when the temperature decreases with a similar trend. The NDR effect is more pronounced in higher drain current, which occurs at lower temperatures, when electron temperature rising from self-heating effect is larger. As shown in previous studies, self-heating affects transport significantly in SOI devices and nanowire devices,[23,24] and recently, in typical graphene devices. Previous studies

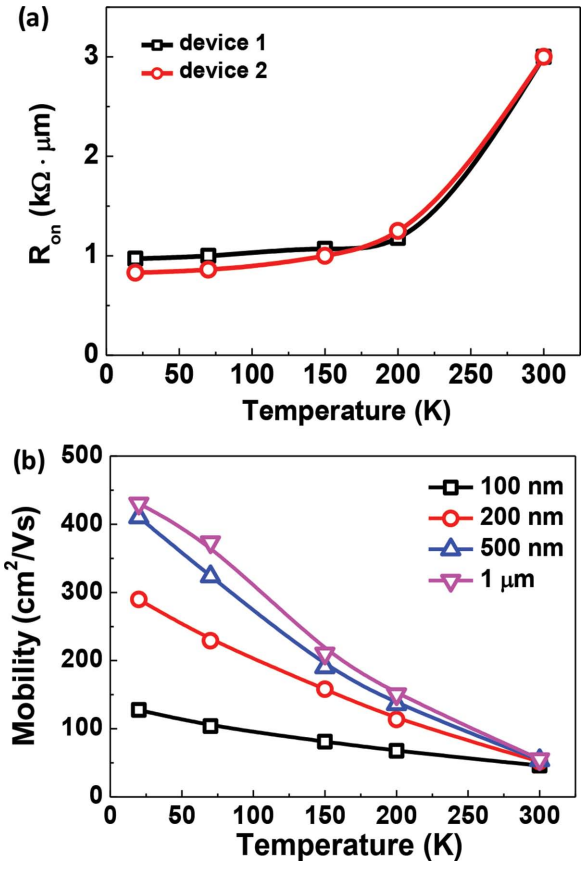

Figure 3. a) R_{on} as a function of temperature extracted from I_d–V_d curves of two 100-nm devices at V_g = 40 V. b) Mobility as a function of temperature for four different channel lengths.

point out that self-heating effect can be partially responsible for the current saturation in graphene transistors when current densities exceeds 500 μA μm^{-1} or transverse fields exceeds 1 V μm^{-1}.[25–27] This effect applies similarly or even more strongly on low dimensional MoS_2 devices on a thick SiO_2 substrate in this study, since both of these materials have low thermal conductivity. To further verify the origin of the NDR behavior, a pulsed-IV method with varying pulse width from 1 ms to 500 μs was used. It is well known that pulsed-IV measurement is a useful tool to reduce or even eliminate the self-heating effect. During pulsed-IV measurement, a pulse is applied to the drain of the transistor while its gate is biased at a fixed voltage (see Figure S4a, Supporting Information). As shown in Figure 4c, the magnitude of the NDR gradually decreases and approaches typical saturation when the pulse width is reduced. The NDR effect disappears once the pulse width is further reduced to 100 μs (see Figure S5, Supporting Information). This dependence of pulse width further confirms the dominant role that self-heating plays in NDR effect observed in our high performance MoS_2 transistors. It also indicates that another possible mechanism for NDR, valley transfer, is insignificant in our few-layer MoS_2 device, as the pulsed-IV measurement in the range of 100 μs does not change carrier velocity. Furthermore, longer channel devices of 200, 500 nm, and 1 μm also exhibit similar NDR behavior (shown as Figure S7, Supporting Information). The carrier velocity of these devices is much less than that of the 100-nm device, and cannot reach the critical velocity for valley transfer. As shown in Figure 4d, the current degradation $\Delta I/I_{sat}$ dependence of pulse width persists at different temperatures. Short pulse reduces self-heating during the on state, and thus less current degradation is observed accordingly. Similar to Figure 4a, Figure 4d shows the NDR effect is more pronounced at low temperatures owing to their higher current and low environmental temperature, which is consistent with the results in SOI FETs.[28] For transistors based on 2D materials other than graphene, choosing a substrate with high thermal conductivity is especially important due to the typically poor thermal conductivity of these 2D materials. To rule out the possible contribution from dielectric relaxation in the NDR behavior, we conducted double-sweep measurement at different temperatures. Figure S4b, S4c (Supporting Information) shows hysteresis behavior in the DC output characteristics of the same 100-nm device at 300–20 K with V_g = 40 V and at 20 K with 5 V steps in V_g from 0 to 40 V, respectively. It is clear that the hysteresis is negligible when NDR takes place, which shows that dielectric relaxation is not responsible for the NDR effect in our MoS_2 devices.

Other than high field transport, another limiting factor in modern electronics is the low frequency noise generated in the electronic devices, which determines how small signals can be detected and resolved without error in circuits.[29] Maintaining a high signal to noise ratio becomes challenging for deeply scaled devices which have stringent operation voltage window requirement and severe short channel effect. In modern communications, the low frequency noise could up-convert to phase noise at radio frequencies and hampers the use.[29] In view of the scientific significance and practical applications, a thorough understanding of the low frequency noise mechanisms in MoS_2 FET is of great importance. However, previous results always yield scattered, rather poor noise level partially because of the nonoptimized contact and device process. Furthermore, the mechanisms of the dominant factors in different output current and temperature regions remain unclear. Here, we carry out low frequency noise measurement of a 200-nm MoS_2 device from 300 to 20 K. The standard method is Hooge's empirical relationship $S_{id} = \frac{AI_d^{\beta}}{f^{\gamma}}$, where S_{id} is the current noise spectral density, f is the frequency, I_d is the current through the device channel, and A is the noise amplitude.[30] The exponents, γ and β, are ideally expected to be close to 1 and 2, respectively. The temperature dependence of the S_{id}/I_d^2 of this device is plotted in **Figure 5**a (electrical properties shown in Figure S7, Supporting Information). It can be seen that the noise level decreases with temperature, suggesting a thermal activation process. The current noise spectral density nicely follows a $1/f$ trend at all temperatures without emergence of generation-recombination bulge signatures. To investigate the dominant physical mechanism of the $1/f$ noise, S_{id}/I_d^2 and transconductance to drain current squared $(g_m/I_d)^2$ as functions of drain current I_d of the same device from 300 to 20 K are plotted in Figure 5b. It is observed that S_{id}/I_d^2 is proportional to $(g_m/I_d)^2$ at the small drain current level, indicating the carrier number fluctuation mechanism as the main source of $1/f$ noise,[30] which is consistent with previous reports on few-layer

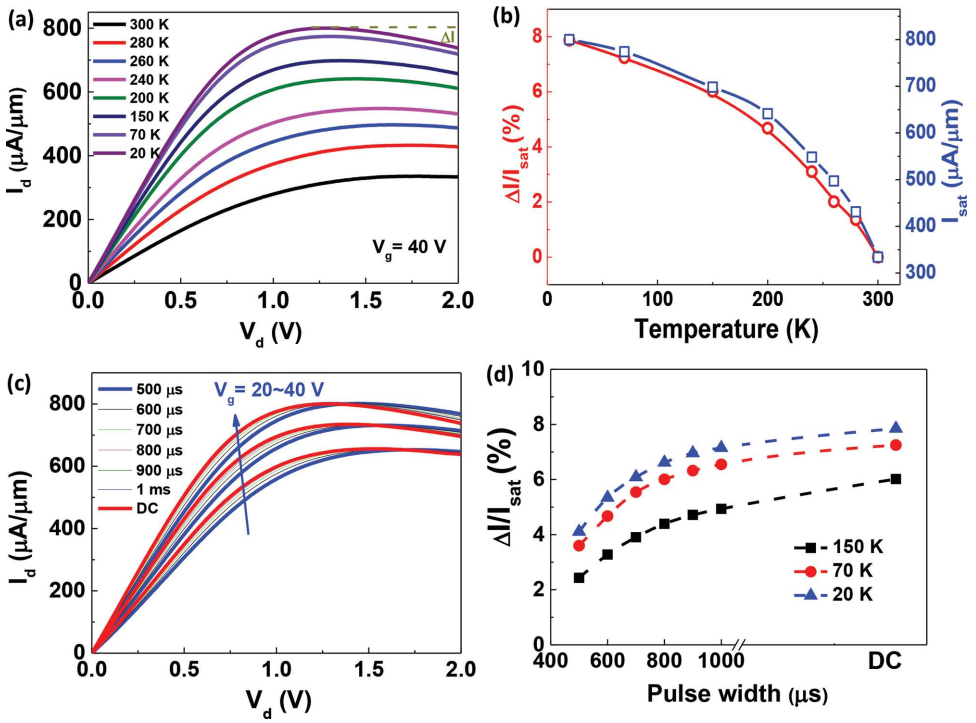

Figure 4. a) Output characteristics of the 100-nm MoS_2 device at various temperatures with V_g = 40 V. b) $\Delta I/I_{sat}$ and I_{sat} as a function of temperature for the 100-nm device. c) Output characteristics of the same device at 20 K with 10 V steps in V_g from 20 to 40 V with comparison between dc measurement and different pulse widths (pulse width = 500, 600, 700, 800, 900 μs, and 1 ms). d) $\Delta I/I_{sat}$ as a function of pulse width for the 100-nm device at three different temperatures.

MoS_2 FETs.[18,19] However, at high drain current, the noise spectral density deviates from $(g_m/I_d)^2$. The noise of homogeneous layers irrespective of the dominate noise model can be typically expressed using Hooge's empirical formula $\frac{S_{id}}{I_d^2} = \frac{\alpha_H}{f_N}$, where α_H is the Hooge parameter, N is the total number of carriers.[30] In linear region (V_d = 0.2 V) under gate overdrive conditions $V_g - V_{th} > 0$, N can be approximated as $N = (V_g - V_{th})LWC_g/e$, where C_g is the gate capacitance per unit area (38.35 nF cm^{-2} for the 90-nm SiO_2 layer), e is the elemental charge, V_{th} is the threshold voltage, and L and W are the channel length and width, respectively. The extracted Hooge parameter α_H of the same device at various temperatures are shown in Figure 5c, exhibiting a clear gate voltage and temperature dependence. The minimum α_H is 3.3×10^{-4} at room temperature, which is about one order of magnitude smaller than previous results.[16,17,19,20] At all temperatures, the Hooge parameter follows the same trend, indicating the dominated noise mechanism does not change with temperature. α_H exhibits $1/(V_g - V_{th})$ dependence when $V_g - V_{th}$ is smaller than 25 V at all temperatures, which is in agreement with carrier number mechanism. For $V_g - V_{th}$ larger than 25 V at all temperatures, α_H remains constant with minimal gate-voltage dependence, consistent with the mobility fluctuation model.[31] This result shows the noise mechanism of few-layer MoS_2 FET is dominated by mobility fluctuation at high drain current level in strong inversion, while number carrier fluctuation noise takes over at low drain current. To benchmark the performance of few-layer MoS_2 device in this work, we compare the drain current noise level S_{id}/I_d^2 against the device channel area $W \times L$ with other MoS_2 FETs in literatures, as shown in the Figure 5d. The MoS_2 device in this work has shown significant improvement in the noise level, which is down to 2.8×10^{-10} μm^2 Hz^{-1} at 10 Hz as a result of much improved contact and on state current. This result is comparable to the 1/f noise requirement of 45-nm node precision analog/RF driver mixed-signal in Si CMOS technology by International Technology Roadmap for Semiconductors.[32]

In conclusion, we have systematically investigated the high-field transport and low frequency 1/f noise in high performance-scaled MoS_2 devices at various temperatures down to 20 K. As a result of using a robust Cl-doping technique, record high drive current up to 800 μA μm^{-1} at 20 K has been achieved. We have also investigated the output power limit of these thin film transistors with self-heating effect which causes the NDR behavior. In addition, these devices exhibit substantially low noise level, reaching a record low current noise spectral density of 2.8×10^{-10} μm^2 Hz^{-1} at 10 Hz. These results demonstrate the great potential of MoS_2 for further nanoelectronic applications.

Experimental Section

Few-layer MoS_2 flakes were mechanically exfoliated from the purchased natural bulk MoS_2 (SPI Supplies) onto a 90-nm SiO_2/p^{++} Si wafer. In order to dope the MoS_2, the sample was then soaked in 1,2 dichloroethane (DCE) for 12 h. After rinsing with acetone and isopropanol, e-beam lithography was used for the source/drain region and Ni (30 nm)/Au (60 nm) were deposited to form the metal contact. The direct current and pulsed-IV characterizations were carried out in a lakeshore cryogenic probe station under vacuum (<10^{-5} Torr) using an Agilent parameter analyzer B1500A. The low frequency 1/f noise

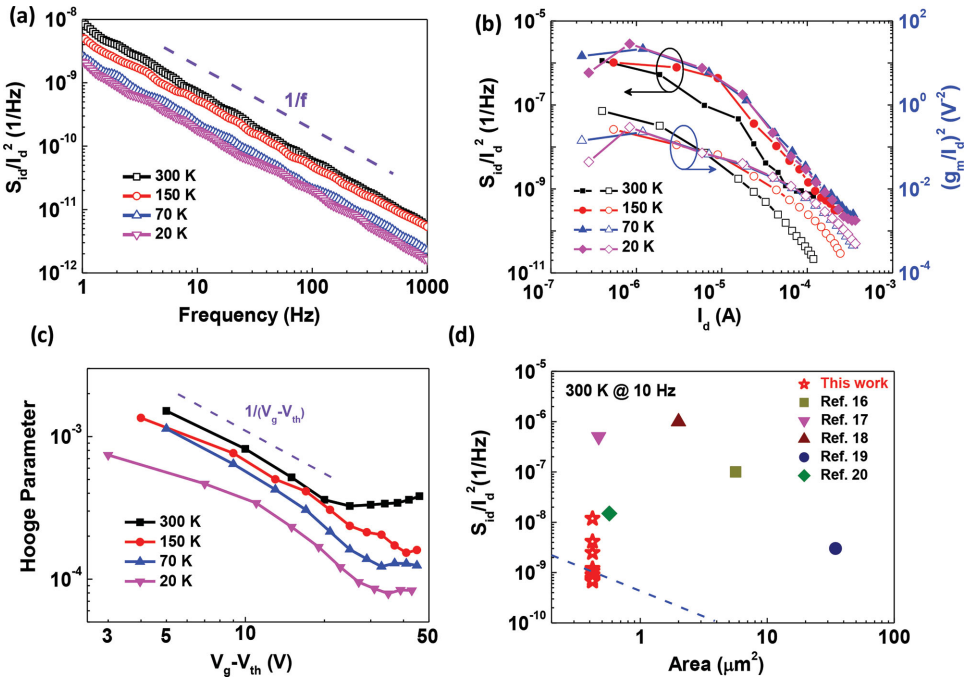

Figure 5. a) Current noise spectral density (S_{id}/I_d^2) as a function of frequency with V_g = 40 V at various temperatures for the 200 nm MoS_2 FET. The ideal 1/*f* behavior is added for comparison. b) Normalized drain current noise spectral density (S_{id}/I_d^2) and transconductance to drain current ratio squared [$(g_m/I_d)^2$] versus drain current for the MoS_2 device from 300 to 20 K. c) Hooge parameter versus $V_g - V_{th}$ at various temperatures from 300 to 20 K. d) Benchmark of current noise spectral density S_{id}/I_d^2 versus channel area for different MoS_2 FETs. The 1/*f* noise requirement of 45-nm node precision analog/RF driver of mixed-signal Si CMOS technology is added as a reference.

measurements were carried out by Agilent E4725A 1/*f* noise system with Agilent E5052B.

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