Applied Physics Letters

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Cite as: Appl. Phys. Lett. **118**, 052107 (2021); https://doi.org/10.1063/5.0039783
Submitted: 06 December 2020 . Accepted: 18 January 2021 . Published Online: 05 February 2021

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Applied Physics Letters ARTICLE scitation.org/journal/apl

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ABSTRACT

In this Letter, enhancement-mode operation in devices with 1.5 nm atomic-layer thin In_2O_3 channels over a wide range of channel lengths down to 40 nm is demonstrated using an O_2 plasma treatment at room temperature. Drain currents (I_D) in excess of 2 A/mm at a drain-to-source bias (V_{DS}) of 0.7 V are achieved in enhancement mode with significantly improved subthreshold swing down to near-ideal 65 mV/dec, suggesting that O_2 plasma treatment is very effective at reducing bulk and interface defects. By using low-temperature O_2 plasma, the fabrication process remains back-end-of-line compatible while enabling a clear route toward high-performance In_2O_3 transistors and circuitry.

Ultra-thin atomic-layer-deposited (ALD) In_2O_3[1–3] has recently been explored for high-performance back-end-of-line (BEOL) compatible electronic devices[4–11] for monolithic 3D integration. Using the as-grown In_2O_3 channels with no further treatment, the threshold voltage (V_T) in buried-gate field-effect transistors (FETs) is a strong function of the channel thickness (T_{CH}) and the best performing devices are restricted to depletion-mode operation.[1,2] This is an undesirable trade-off, and a separate method is needed to engineer V_T. An annealing process can induce the desired V_T shift, but comes at the cost of increased thermal budget, which may not be tolerable for all applications.[3] Here, we resolve this trade-off by introducing a simple process at the end of the device fabrication. By treating the devices with an O_2 plasma at room temperature, V_T can be engineered while maintaining the low thermal budget and, thus, the BEOL compatibility of the process.

Devices treated with O_2 plasma for different amounts of time are demonstrated and analyzed over a wide range of channel lengths (L_{CH}) from 1 μm to 40 nm. As in the previous work, the scaled devices are able to conduct drain currents well in excess of 2 A/mm, but now operate in enhancement mode enabled by controllably shifting V_T, making them highly attractive for BEOL transistor and circuitry applications. Furthermore, the subthreshold swing (SS) is improved significantly down to near-ideal 65 mV/dec, closely approaching the thermionic limit at room temperature, corresponding to a low interface trap density (D_{it}) of 8×10^{11} cm^{-2} eV^{-1}.

In_2O_3 transistors were fabricated as described in detail in an earlier publication.[1] A buried-gate FET structure [more specifically, a staggered bottom-gate thin-film transistor (TFT) structure] is employed with Ni serving as the gate, source, and drain electrodes. The 5 nm HfO_2 layer used as the gate dielectric and the 1.5 nm thick In_2O_3 channel layer are grown by ALD, using $[(CH_3)_2N]_4Hf$ (TDMAHf) and $(CH_3)_3In$ (TMIn) as the respective metal-organic precursors and H_2O as the oxygen source for both materials. HfO_2 and In_2O_3 were grown at 200 °C and 225 °C, respectively. An illustration of the final structure is shown in Fig. 1(a). Figure 1(b) shows a 4-in. wafer of In_2O_3 devices, enabled by the large-scale uniform ALD growth. Figures 1(c) and 1(d) demonstrate accurate thickness control of the In_2O_3 channel by ALD cycles using atomic force microscopy (AFM) and transmission electron microscopy (TEM), respectively. Figure 1(e) presents a breakdown measurement of the gate dielectric showing a hard breakdown voltage around 4 V, confirming the high quality of ALD HfO_2 on Ni. Figure 1(f) shows C–V measurements used to extract the equivalent oxide thickness (EOT) and directly

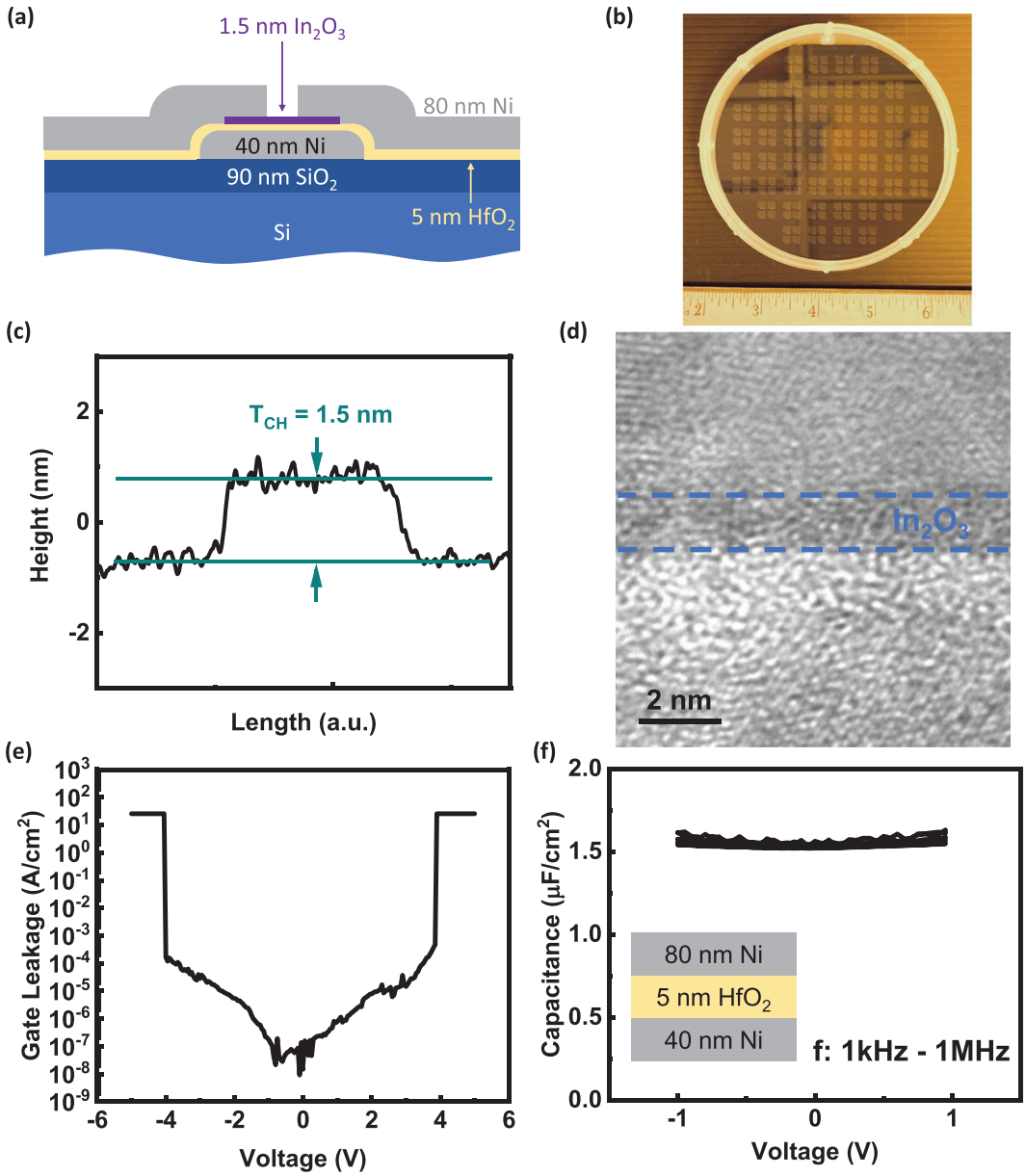

FIG. 1. (a) Schematic drawing of the buried-gate ALD In_2O_3 transistor structure used in this work. (b) 4-in. wafer with ALD-grown In_2O_3 devices. Confirmation of good ALD thickness control by (c) AFM measurement of 1.5-nm-thick In_2O_3 and (d) TEM of a 1.2-nm-thick ALD In_2O_3 layer. (e) Breakdown test of the HfO_2 gate dielectric. (f) C–V measurement used to extract EOT. The inset shows the test structure used for (e) and (f).

measure the gate oxide capacitance (C_{ox}). The EOT is 2.1 nm. After the structural fabrication was complete, the devices were exposed to an O_2 plasma generated with an RF power of 100 W at 1.25 Torr in a barrel asher at room temperature. Depending on the length of plasma exposure, V_T can be controllably tuned. Since the plasma treatment is performed after fabrication, the excellent contact resistance between Ni and the degenerately n-type native In_2O_3 under the contacts[2] is maintained, while the channel properties are modified. The process remains BEOL compatible due to the low-temperature nature of the O_2 plasma.

Transfer (I_D–V_{GS}) and output (I_D–V_{DS}) characteristics of typical short- and long-channel transistors after a 10-min O_2 plasma treatment are shown in Fig. 2. In both cases, V_T is greater than 0 V, and the dependence on L_{CH} is weakened, which can be attributed to a reduction in the intrinsic electron doping by defects.[12] Figures 2(a) and 2(b) show curves for a device with $L_{CH} = 40$ nm. The maximum on-current reaches 2.2 A/mm at a drain bias of 0.7 V and an overdrive voltage of 2.44 V (V_T is 0.56 V). V_T is determined by the linear extrapolation method. The longer channel device measured in Figs. 2(c)

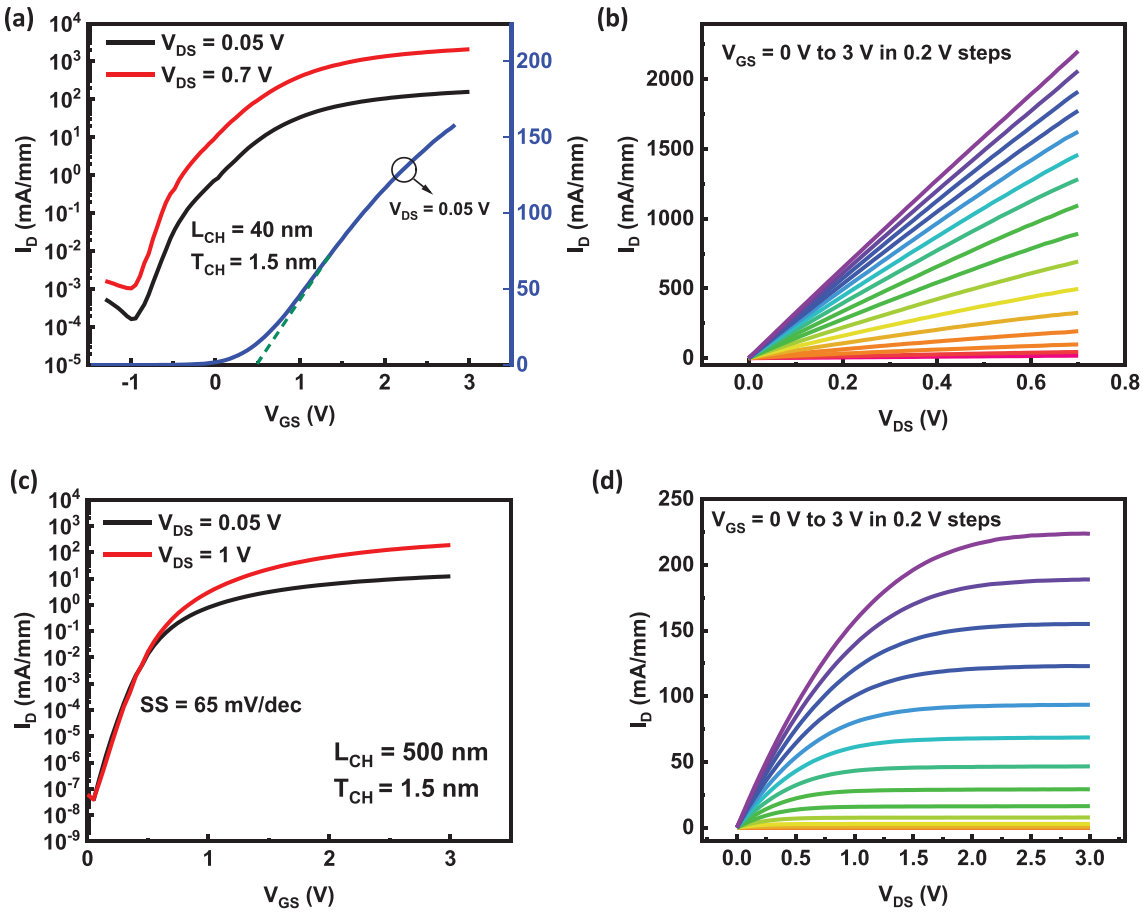

FIG. 2. Transfer and output characteristics of typical (a) and (b) 40 nm and (c) and (d) 500 nm channel length In_2O_3 transistors after O_2 plasma treatment for 10 min (1.25 Torr, 100 W RF power at room temperature). The In_2O_3 channel layer is 1.5 nm thick. The 40 nm devices achieve on-currents of 2.2 A/mm at a moderate drain bias of 0.7 V and operate in enhancement mode; the device shown has $V_T = 0.56$ V. The 500 nm device shown has a near-ideal SS of 65 mV/dec.

and 2(d) with $L_{CH} = 500$ nm shows saturation behavior at high V_{DS} with a near-ideal SS of 65 mV/dec. The interface trap density (D_{it}) at the HfO_2/In_2O_3 interface can be estimated to be 8×10^{11} cm^{-2} eV^{-1} according to $SS = 2.3\ kT/q\ (1 + C_{it}/C_{ox})$, where k is the Boltzmann constant and q is the elementary charge. The impact of depletion capacitance is negligible due to the ultrathin nature of the In_2O_3 channel.

Figure 3 shows key device performance metrics as a function of channel length for three different cases: (i) no O_2 plasma treatment, (ii) a moderate duration O_2 plasma treatment (1 min), and (iii) a longer O_2 plasma treatment (10 min). All O_2 plasma treatments were performed in an atmosphere of 1.25 Torr O_2 with an applied RF power of 100 W at room temperature. Figure 3(a) shows the average on-current (I_{ON}) at a constant gate overdrive voltage of 2.2 V achieved at a drain–source bias (V_{DS}) of 1 V (except where otherwise noted). At a given L_{CH}, I_{ON} is moderately reduced after plasma treatment. However, the currents are still so large that they push the limits of the material system—for the shortest channel lengths explored in this work, a reduced V_{DS} must be applied to avoid self-heating effects. Figure 3(b) shows the transconductance (g_m) likewise reduced by a moderate amount in O_2 plasma-treated devices compared to their counterparts at the same L_{CH}. This may be due to the reduced carrier concentration in the channel increasing the channel resistance. Similarly, Fig. 3(d) shows a reduction in μ_{FE} since it is extracted from g_m. The positive V_T shift enables the channel length scaling down to 40 nm. As a result, a high g_m value of 0.94 S/mm at a V_{DS} value of 0.7 V is achieved. Figure 3(c) shows the SS significantly improving as a longer O_2 plasma treatment is applied, closely approaching the room-temperature thermionic limit of 60 mV/dec in long-channel devices. This suggests a sizeable interface and bulk trap density in the as-grown In_2O_3 film has been reduced by the O_2 plasma treatment. Figure 3(e) shows V_T at each measured channel length. After a sufficiently long O_2 plasma exposure, the devices all operate in enhancement mode.

Although there are competing theories, it has long been thought that oxygen vacancies play a crucial role in indium oxide's electrical properties, e.g., Refs. 13–15. The specific TMIn/H_2O ALD chemistry employed in this work has been studied[16,17] and shows the same vacancy doping behavior as other growth methods. A similar O_2 plasma treatment has been studied by x-ray photoelectron spectroscopy (XPS) in much thicker (500–1000 nm) In_2O_3 layers grown by

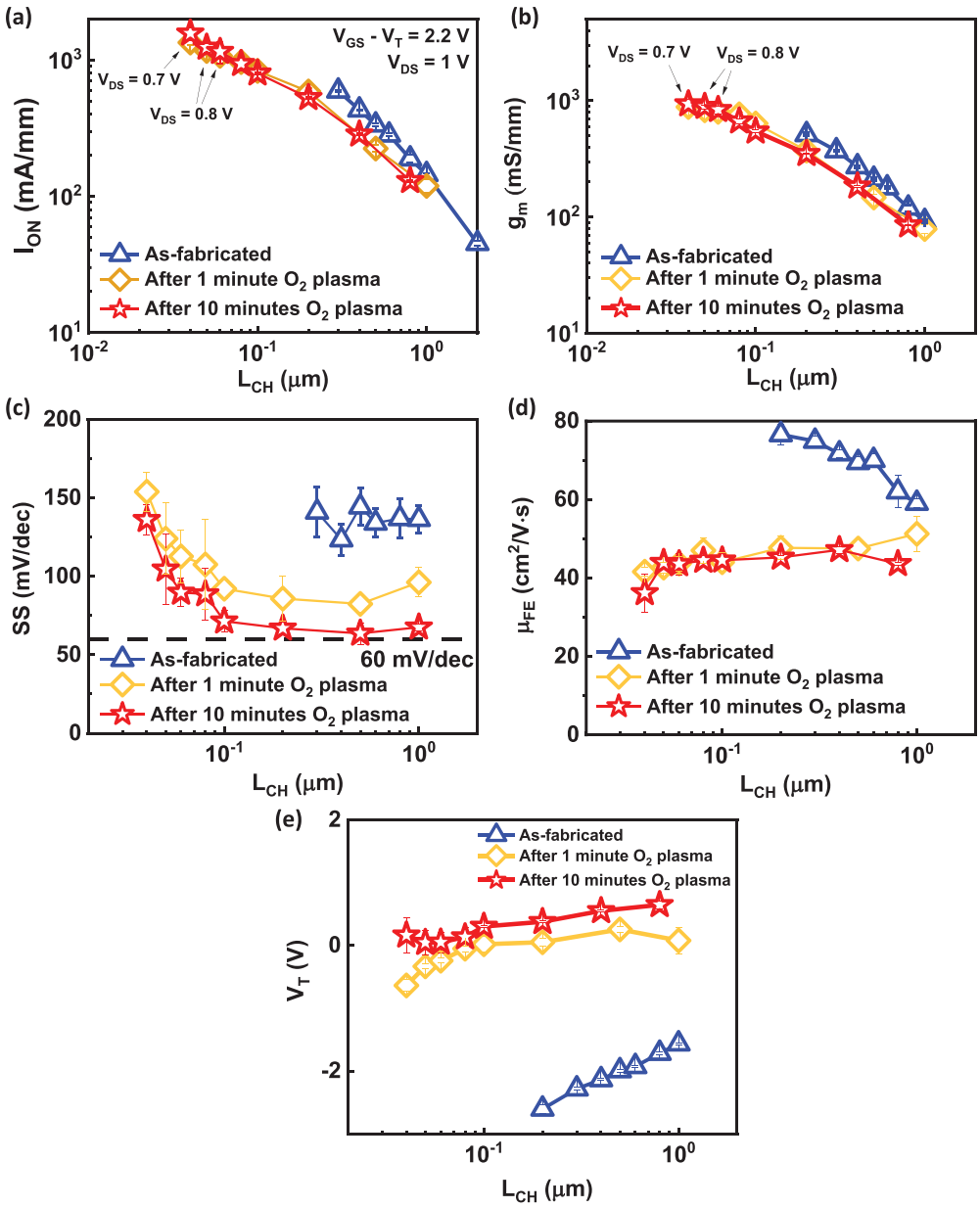

FIG. 3. (a) Average on-current for each channel length at a constant overdrive voltage of 2.2 V, with $V_{DS} = 1$ V except for the devices indicated. (b)–(e) Transconductance, SS, μ_{FE}, and V_T as functions of channel length under different plasma treatment conditions. With a sufficient O_2 plasma exposure, devices at all measured channel lengths operate in enhancement mode and show a weaker V_T–L_{CH} dependence.

plasma-assisted molecular beam epitaxy (MBE).[18] A thin layer of charge is known to exist at the surfaces of (crystalline) In_2O_3.[13,18,19] After their plasma treatment, significant band bending (away from being degenerately n-type) in the first few nanometers below the In_2O_3 surface is extracted from the XPS measurements. While the mechanism responsible is not entirely clear, this provides some further insight into the behavior. Taken together with our device data, this paints a picture of the intrinsic defects that give In_2O_3 such high electron doping and high current densities, which is appreciably removed or filled by the energetic O_2 from the plasma.

Figure 4 emphasizes the device parameters achieved in this work critical for high-performance device applications. Figure 4(a) shows the enhancement-mode operation of the devices across the measured range of channel lengths while simultaneously reaching over 2 A/mm of on-current. After a short exposure of 1 min, the devices are already close to their terminal V_T values, suggesting a saturation of the O_2 plasma effect near $V_T = 0$ V, which allows for facile controllability and

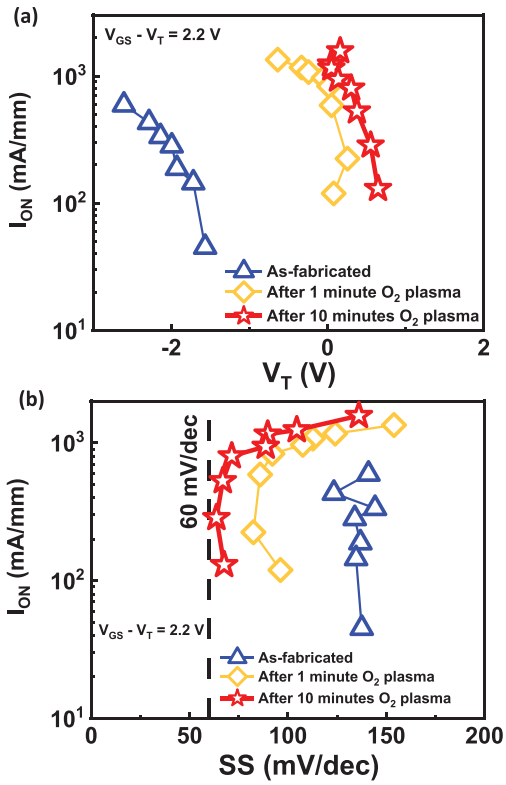

FIG. 4. Comparisons of key device parameter evolution during O_2 plasma treatment. (a) V_T is shifted while maintaining excellent I_{ON}. (b) Low SS near the thermionic limit is achieved in devices with high I_{ON} around 1 A/mm in enhancement-mode operation after sufficient treatment.

repeatability. Figure 4(b) shows an I_{ON}–SS plot, showing nearly ideal SS at currents approaching 1 A/mm in enhancement-mode In_2O_3 devices treated with O_2 plasma.

O_2 plasma treatment of atomic-layer thin In_2O_3 transistors has been demonstrated as an important process for engineering device behavior in a BEOL-compatible manner. The large controllable V_T shifts induced by the treatment are used to operate in enhancement mode with a 1.5-nm-thick In_2O_3 channel down to the channel length of 40 nm while simultaneously improving the SS. Although at a given channel length, the on-current, g_m, and μ_{FE} are reduced, overall performance is still the best for oxide semiconductors achieving an I_D value of 2.2 A/mm at $V_{DS} = 0.7$ V. This work provides a clear route to apply recent work on atomic-layer thin channel In_2O_3 transistors for BEOL transistor and circuitry applications.

The authors gratefully acknowledge X. Sun and H. Wang for the technical support on TEM imaging. This work was mainly supported by the Semiconductor Research Corporation (SRC) through the nCore IMPACT Center. This work was also supported in part by AFOSR and SRC/DARPA JUMP ASCENT Center.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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