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High-Stability Ultrathin Oxide Transistors via Defect Engineering for High-Performance Capacitorless DRAM

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The rapid development of generative artificial intelligence is driving the growing demand for high-capacity dynamic random-access memory (DRAM). Amorphous oxide semiconductor-based 2T0C DRAM has garnered considerable attention for its potential in overcoming the scaling limitations of conventional 1T1C DRAM. However, inherent stability issues have hindered device performance and practical adoption. In this work, high performance and excellent bias stability in ultrathin indium-gallium-oxide (IGO) field-effect transistors through O_3-based HfO_2 passivation is demonstrated. This improvement results from the suppression of shallow-level defects, deep-level oxygen vacancies, and hydrogen impurities, leading to a high field-effect mobility of 35 $cm^2V^{-1}s^{-1}$, a positive threshold voltage, and outstanding stability—exhibiting only a +5-mV threshold voltage shift under −5 MV cm^{-1} bias for 1 h. The resulting 2T0C DRAM cell achieves a retention time of over 30 000 s—a 100 × improvement over unpassivated devices—together with a 10 ns write speed, 4-bit storage capability, and endurance exceeding 10^{11} cycles, representing a viable platform for future high-density memory applications.

1. Introduction

Dynamic random-access memory (DRAM) is a key enabling technology for artificial intelligence and cloud computing, offering high-speed operation and substantial storage capacity. As AI models continue to grow in size, enhancing DRAM capacity has become increasingly critical.[1] Nevertheless, conventional silicon-based one-transistor-one-capacitor (1T1C) DRAM cells face considerable scaling challenges, primarily due to leakage currents caused by short-channel effects and the manufacturing difficulties associated with high-aspect-ratio capacitors.[2–4] To overcome these limitations, two-transistor-zero-capacitor (2T0C) DRAM architectures employing amorphous oxide semiconductors (AOSs) have emerged as promising alternatives for further miniaturization. AOS FETs demonstrate ultralow off-state leakage currents (<10^{-18} A μm^{-1}),[5–6] which significantly prolong the data retention time and reduce the need for refresh operations, thereby lowering power consumption.[7,8] The use of a transistor gate capacitor, in place of the conventional deep-trench or stack capacitor, enables a simpler fabrication process and a reduced cell footprint, thus increasing the storage density. Furthermore, the multi-bit operation capability of the 2T0C architecture, combined with the back-end-of-line (BEOL) compatibility and 3D-integration potential of AOS devices, offers a scalable route to achieve substantially higher storage densities for future memory applications.[7–13]

Indium-based oxides are an important class of oxide semiconductors known for their high carrier mobility.[14,15] However, pure In_2O_3 tends to exhibit electrical instability due to the high concentration of oxygen vacancy defects.[16] Doping with metals that have high oxygen-binding energies—such as Ga, Sn, or W—can mitigate this issue.[17–19] In particular, Ga_2O_3 has a similar octahedral structure to In_2O_3, which reduces lattice distortion and preserves high mobility, a key requirement for fast writing in DRAM.[20–22] These properties make indium gallium oxide (IGO) a promising material for capacitorless DRAM devices. Oxide semiconductors can be fabricated through various methods, such as magnetron sputtering and atomic layer deposition (ALD).[15,23] ALD is especially advantageous, offering low-temperature processing (<300 °C), atomic-level thickness control, and large-area uniformity with conformal coverage—key for monolithic 3D integration. Its self-limiting growth mechanism facilitates strong metal–metal and metal–oxygen bonds, resulting in a highly ordered atomic structure, which significantly improves carrier transport and mobility.[24] These properties make ALD a promising technique for producing high-performance oxide semiconductor films.

Currently, 2T0C DRAM cells using amorphous oxide semiconductors such as IGZO, IWO, and ITO have been widely studied with a focus on retention time, write speed, and storage density.[9,18,25–27] However, few experimental studies have

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addressed the impact of transistor instability on capacitorless DRAM performance. Enhancing the stability of AOS FETs is critical for their commercial adoption. These devices often exhibit threshold voltage shifts under bias stress, which is mainly attributed to defects such as oxygen vacancies and hydrogen impurities.[28–30] Several strategies—including oxygen annealing, fluoride doping, and higher gallium content—have been employed to suppress these defects and improve stability.[21,22,31–34] However, these approaches often face a trade-off between stability and the output current, as defect reduction typically lowers the carrier concentration and increases the contact resistance. Although crystallization has been explored to enhance both performance and stability,[35] the high temperatures required (>400 °C) are incompatible with monolithic 3D integration. Thus, there is a pressing need for a simple and BEOL-compatible method to increase device stability and facilitate the commercialization of oxide semiconductor-based capacitorless DRAM.

In this work, we demonstrate highly stable ultrathin IGO FETs passivated by O_3-based HfO_2 deposited via atomic layer deposition. The passivation strategy suppresses shallow- and deep-level oxygen vacancies in the oxide channel, as well as hydrogen impurities in the dielectric. This comprehensive defect control enables a high field-effect mobility of 35 $cm^2V^{-1}s^{-1}$, a positive threshold voltage, and excellent bias stability—exhibiting a negligible threshold voltage shift of only +5 mV under −5 MV cm^{-1} for 1 h. The resulting 2T0C DRAM cell incorporating HfO_2-passivated IGO FETs achieves a retention time exceeding 30000 s, with a theoretical projection reaching 10^5 s—over two orders of magnitude longer than that of their unpassivated counterparts. Furthermore, the cell delivers a 10 ns write speed, supports 4-bit multilevel storage with 1000 s retention under multibit operation, and performs over 10^{11} read/write cycles without significant degradation. These results highlight the promising potential of this technology for next-generation high-density memory applications.

2. Results

2.1. Device Structure and Electrical Characteristics

Figure 1a shows a schematic of a 2T0C DRAM cell comprising two identical back-gated IGO FETs: a write transistor and a read transistor, with the former connected to the gate of the latter. The fabrication process, outlined in Figure S1 (Supporting Information) and detailed in the Methods section, began with a high-resistivity silicon substrate topped with 300 nm SiO_2. The back-gate electrode was deposited via electron-beam evaporation, followed by the sequential atomic layer deposition (ALD) of a 10 nm Al-doped HfO_2 gate dielectric and a 3.6 nm IGO channel (Figure S2, Supporting Information). The gate dielectric capacitance was measured to be 1.3 μF cm^{-2} using a fabricated MOS capacitor (Figure S3, Supporting Information). The contact windows were then patterned and opened by reactive ion etching (RIE), and the contacts/interconnects were formed in a single electron-beam evaporation step. Finally, an ozone-based HfO_2 passivation layer was deposited via ALD under oxygen-rich conditions to enhance device stability.

Figure 1b presents the equivalent circuit of a 2T0C DRAM cell, which incorporates four operational ports: the write word line (WWL), write bit line (WBL), read word line (RWL), and read bit line (RBL). The WWL controls the turn-on and turn-off of the write transistor, whereas the WBL regulates the data written to the storage node. The RWL and RBL are used for reading the stored data. The operation of a 2T0C DRAM cell can be divided into three stages—write, hold, and read—as illustrated in Figure S4 (Supporting Information). (1) Write: The write operation is controlled jointly by the WWL and WBL. A positive voltage applied to the WWL turns on the write transistor, allowing the WBL to regulate the amount of charge transferred into the storage node (SN). (2) Hold: A negative voltage on the WWL turns off the write transistor, isolating the SN from the WBL and preserving the stored charge. (3) Read: The stored data are read by measuring the source–drain current of the read transistor, where a high current corresponds to logic “1” and a low current corresponds to logic “0”. These three steps represent ideal operational conditions. In practice, however, 2T0C DRAM faces challenges such as charge leakage, signal disturbance, and a limited sensing margin, which will be discussed in later sections. Importantly, during the retention phase, the use of a negative WWL voltage combined with a positive SN voltage raises concerns about bias stress stability in the transistors. As shown on the right side of Figure 1b, the shifts in threshold voltage due to bias stress cause variations in I_{OFF} and I_{RBL}, which in turn lead to undesirable effects such as shortened retention time and read failures. Therefore, enhancing the bias stability of oxide FETs is crucial for developing reliable capacitorless DRAM.

To enhance the stability of the IGO FETs, an O_3-based HfO_2 passivation layer was deposited via ALD. Material characterization was performed to analyze changes in the channel layer before and after passivation. X-ray photoelectron spectroscopy (XPS) was used to probe the chemical states and composition of the IGO films. Figure 1c displays the O 1s XPS spectra for samples with and without HfO_2, which are deconvoluted into three components: metal-oxygen bonds (M─O, 530 ± 0.1 eV), oxygen vacancies (V_O, 531 ± 0.1 eV), and hydrogen-related oxygen species (─OH, 532 ± 0.1 eV).[21,22] After passivation, the M─O content increased significantly from 47.84% to 80.65%, whereas V_O and ─OH contents decreased from 30.62% to 12.67% and from 21.54% to 6.68%, respectively, indicating enhanced metal-oxygen bonding and reduced defect concentrations. To further evaluate the elemental changes, particularly in the hydrogen content, secondary ion mass spectrometry (SIMS) was conducted. As shown in Figure 1d, HfO_2 passivation reduced the amount of hydrogen impurities, which can be attributed to hydrogen effusion at elevated temperatures during the ALD process.[36] Notably, the SIMS signal intensity of hydrogen following passivation slightly decreases (≈40%), indicating that the hydrogen impurity concentration in the film has not substantially decreased. Although the decrease in the hydrogen signal is modest, it remains meaningful given the critical role of hydrogen impurities in oxide transistor reliability.[30] The underlying defect-related degradation mechanisms are discussed in later sections.

We analyzed the influence of passivation on the electrical performance. Figure 1e,f compares the transfer and output characteristics of IGO FETs with and without HfO_2 passivation, respectively. The passivated device exhibited a maximum mobility of 35 $cm^2V^{-1}s^{-1}$ and a maximum output current of 208 μA $μm^{-1}$, outperforming the unpassivated device (26.4 $cm^2V^{-1}s^{-1}$ and 172 μA $μm^{-1}$, see Figure S5, Supporting Information). Changes

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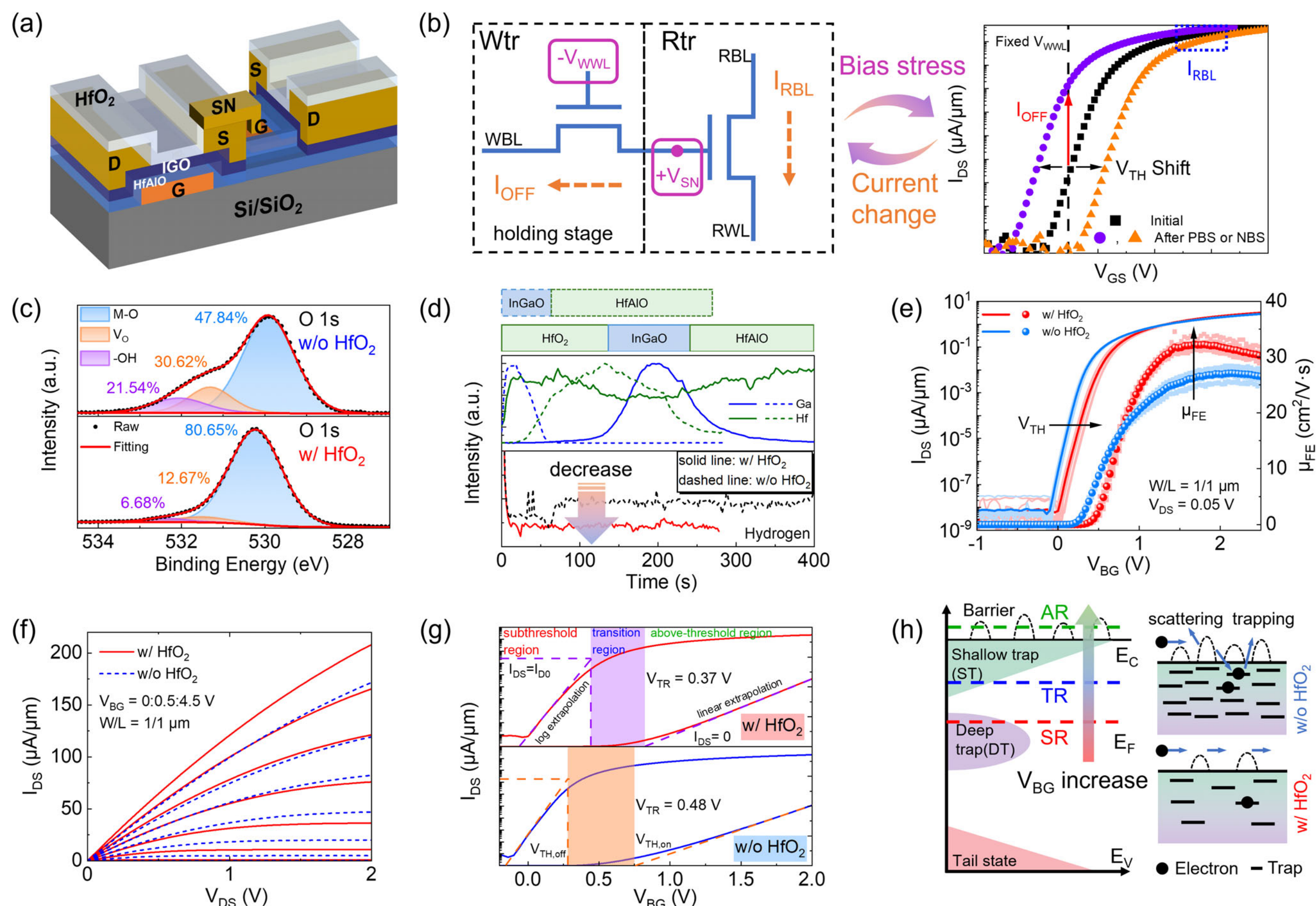

Figure 1. Structure of the 2T0C DRAM and electrical characterization of IGO FETs. a) Schematic of the 2T0C DRAM cell comprising two identical back-gated IGO FETs: a write transistor (Wtr) and a read transistor (Rtr), with the source Wtr connected to the gate Rtr to form the storage node (SN). b) Equivalent circuit (left) and schematic illustrating the impact of bias-stress-induced threshold voltage variation on DRAM performance (right). Such variations can shorten the retention time, whereas fluctuations in the on-state current (I_{ON}) may lead to read errors. c) O 1s XPS spectra comparison for IGO films with and without HfO_2 passivation. d) SIMS depth profiles of Ga, Hf, and H in the film stack with and without HfO_2. e) Transfer characteristics and mobility distribution of IGO FETs with (n = 10) and without (n = 11) HfO_2 passivation (L_{ch} = 1 µm, V_{DS} = 0.05 V). f) Output characteristics with and without HfO_2 passivation at V_{GS} from 0 to 4.5 V in 0.5 V steps. g) Comparison of the transition region voltage (V_{TR}), defined as $V_{TH,on} - V_{TH,off}$, representing the shallow trap density (N_{ST}) near the conduction band (the extraction method follows Ref.[43]). h) Energy band diagrams near the conduction band with and without HfO_2. Symbols "–" and "•" denote empty traps and electrons, respectively.

in electrical properties manifest in two primary aspects: a positive shift in threshold voltage (from 0.16 to 0.31 V) and an improvement in mobility. The positive shift in threshold voltage is likely due to the reduction in oxygen vacancies and hydrogen impurities, both of which act as electron donors in oxide semiconductors.[37–39] The increase in mobility can be understood in terms of carrier transport mechanisms in amorphous oxide semiconductors (the mechanism diagram is shown in Figure S6, Supporting Information). Above threshold, at low gate voltages ($E_F < E_C$), conduction is primarily trap-limited conduction (TLC),[40,42] characterized by frequent trapping and release events at shallow defect states near the conduction band, μ_{FE} is proportional to $n_{free}/(n_{free}+n_{trap})$, where n_{free} and n_{trap} are the free and trapped carrier densities, respectively. At higher gate voltages ($E_F > E_C$), gate-induced free carriers fill these trap states, making percolation conduction the dominant transport mechanism,[41,42] in which carriers migrate through the conduction band along the lowest-energy paths, and mobility is influenced by potential fluctuations in the conduction band. The suppression of trapping/release events due to shallow defect passivation enhances carrier transport efficiency in the channel. Furthermore, it allows carriers to more readily enter the conduction band, promoting band transport, which explains why the passivated device reaches its peak mobility at a lower gate voltage (Figure 1e), aligning well with the proposed mechanism.

To further validate that defect passivation improves device performance, we quantitatively analyzed the shallow trap density near the conduction band. As shown in Figure 1g, the transfer characteristics can be divided into three regions: the subthreshold region (SR), transition region (TR), and above-threshold region (AR). The underlying mechanism in the TR is illustrated in Figure 1h. As V_{BG} increases, the Fermi level increases within the bandgap. When it enters the range of shallow traps near the conduction band edge (E_C), these traps capture gate-induced free carriers, requiring additional gate bias to push the Fermi level above E_C and turn on the transistor. The width of the transition region

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thus reflects the density of shallow traps. The shallow trap density (N_{ST}) was extracted via the relation $V_{TR} = qN_{ST}/C_{ox}$, where V_{TR} is the voltage range of the transition region, C_{ox} is the gate capacitance per unit area, and q is the electron charge.[43] The measured V_{TR} values were 0.37 and 0.48 V for devices with and without HfO_2, corresponding to N_{ST} values of 2.89×10^{12} and 3.75×10^{12} cm^{-2}, respectively. As illustrated in Figure 1h, the reduced shallow trap density in passivated devices suppresses defect scattering and trap-limited conduction, thereby increasing mobility.[42,44]

Temperature-dependent electrical measurements further support these findings. Passivated FETs exhibited a smaller temperature-induced threshold voltage shift (−1.3 vs −5.3 mV °C^{-1} for unpassivated devices; Figure S7, Supporting Information), which is consistent with the reduced thermal excitation of carriers from shallow traps. Additionally, annealing at 300 °C in oxygen resulted in smaller performance variations in passivated devices (Figure S8, Supporting Information), confirming improved thermal stability. Our analysis confirms that the mobility in amorphous oxide FETs is intrinsically limited by shallow-level defects, including tail states arising from bulk disorder, tail states resulting from thickness fluctuations, shallow interface states, and shallow oxygen vacancies.[43] This insight provides a clear pathway for performance optimization through targeted defect mitigation.

2.2. Reliability of IGO Field-Effect Transistors

This section evaluates the influence of an HfO_2 passivation layer on the reliability of IGO FETs. Reliability was assessed by alternating measurement–stress–measurement (MSM) cycles: during the measurement phase, *I–V* transfer characteristics were recorded, whereas the stress phase involved applying a static gate bias with grounded source and drain terminals (see test setup in Figure S9, Supporting Information).[58] As shown in **Figure** 2a,b, devices with HfO_2 passivation exhibit significantly suppressed threshold voltage shifts under both positive and negative bias stress (PBS/NBS) at ±5 MV/cm, with ΔV_{TH} values of −98.5 mV (PBS) and +5 mV (NBS). These values represent a substantial improvement over unpassivated devices, which showed shifts of −244 and −570 mV, respectively. Additional tests conducted at ±1 and ±3 MV cm^{-1} further corroborated the stability enhancement afforded by passivation (Figure S10, Supporting Information). As shown in Figure 2c and Table S1 (Supporting Information), under identical bias stress conditions with a fixed duration of 1000 s, the HfO_2-passivated devices in this work exhibit a minimal threshold voltage shift, particularly under negative bias stress, outperforming previously reported AOS FETs.[32,50–53,65] These results confirm that O_3-based HfO_2 passivation provides a simple yet effective approach to significantly enhance device stability.

The bias stability of oxide thin-film transistors is strongly influenced by the properties of their constituent layers, including defects and impurities in the gate dielectric and channel, as well as the quality of the dielectric–channel interface.[45] The subthreshold swing (SS) serves as a key metric for characterizing the interface state density. Close inspection of the transfer curves in Figure 2a,b reveals nearly rigid shifts under bias stress, with no significant change in the SS. To quantitatively confirm this, we extracted SS as a function of stress time (Figure S11, Supporting Information), which exhibited a variation of less than 2%. This result indicates that the dielectric–channel interface plays a negligible role in bias instability. Therefore, subsequent mechanism analysis focuses primarily on the dielectric and channel layers.

First, we investigated the mechanism of positive bias stress (PBS). Figure 2d,e shows the threshold voltage as a function of stress time under different bias fields for devices without and with passivation, respectively. The two types of devices exhibit distinct threshold voltage trends: unpassivated devices show an initial negative shift followed by a positive shift, whereas passivated devices display the opposite behavior. This finding suggests the involvement of two competing mechanisms. Typically, under PBS, a positive threshold voltage shift is attributed to electron trapping by defects in the gate dielectric.[46] In contrast, a negative shift is often linked to hydrogen impurities within the dielectric.[46–47] In the latter case, hydrogen species migrate from the dielectric into the channel, releasing electrons into the conduction band. These released electrons leave behind protons (H^+), which subsequently bond with oxygen ions (O^{2-}) to form $[OH]^-$ defect complexes ($O^{2-} + H \rightarrow [OH]^- + e^-$). The initial negative shift in unpassivated devices indicates dominant hydrogen migration at early stages. After passivation, the reduced hydrogen content suppresses this effect, leading to an initial positive shift—indicating that electron trapping now dominates. Figure 2f schematically shows the proposed mechanism responsible for positive bias stress. These results indicate that the PBS stability is closely related to the gate dielectric quality. Enhancing this stability will require further reduction of defects and hydrogen impurities in the dielectric, potentially through optimization of the dielectric growth conditions or the adoption of alternative oxides with higher binding energies, such as MgO or GdO. This warrants further investigation in future studies.

The hydrogen-related degradation mechanism involves multiple steps—including migration, charge release, and bond formation. The following experimental evidence further substantiates this hydrogen interaction model: (1) Under a high electric field or elevated temperature (Figure S12, Supporting Information), the negative threshold voltage shift intensifies, which is consistent with accelerated hydrogen migration into the channel and the consequent release of additional electrons.[57] Passivated devices exhibit a 10–50% smaller threshold voltage shift under positive bias temperature stress (PBTS), corroborating SIMS results that indicate a partial reduction in hydrogen content. This confirms that while HfO_2 passivation is beneficial, it only partially mitigates hydrogen-related degradation. (2) No recovery is observed after PBS when a reverse bias is applied (Figure S13, Supporting Information), supporting the conclusion that hydrogen ions form stable $[OH]^-$ complexes with oxygen in the channel and do not migrate back under a reverse electric field. This irreversible behavior aligns with earlier reports.[61] Together, these results reinforce the critical role of hydrogen impurities in PBS-induced instability and highlight the need for more effective defect control strategies.

In contrast to the complex shifts under PBS, the unpassivated devices in Figure 2g show a consistent negative V_{TH} shift under NBS, which is independent of the bias voltage. In contrast, passivated devices exhibit negligible threshold voltage variation. Under NBS, the negative V_{TH} shift can be attributed to two main

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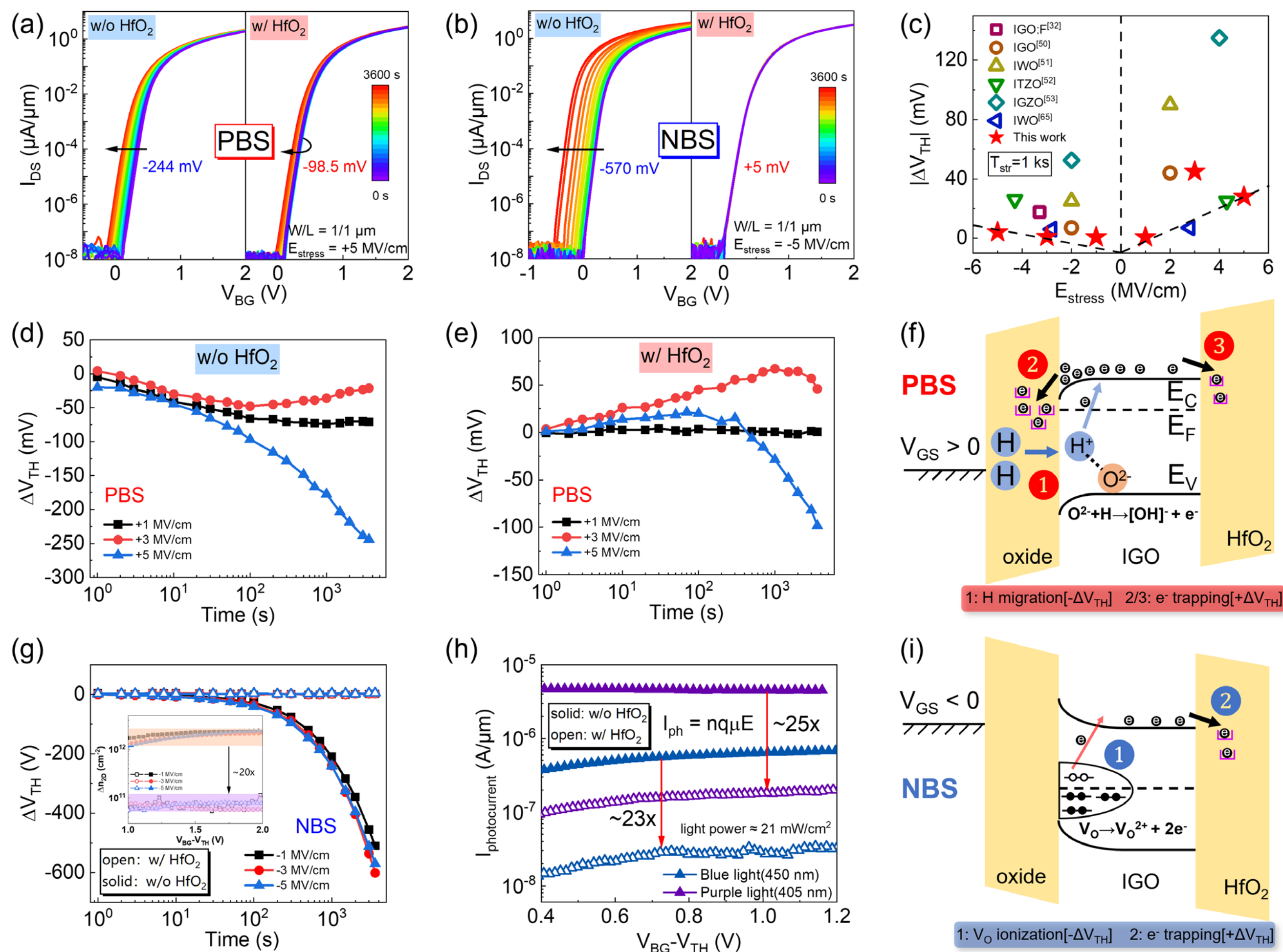

Figure 2. Bias stability of IGO FETs and mechanistic analysis. a, b) Transfer characteristics of IGO FETs with and without HfO_2 under (a) positive (+5 MV cm^{-1}) and (b) negative (−5 MV cm^{-1}) bias stresses, measured from 0–3600 s (W/L = 1 μm/1 μm, V_{DS} = 0.05 V). c) Benchmarking of maximum threshold voltage shift under varying bias fields at a fixed stress time of 1000 s, comparing this work with reported AOS FETs. d, e) Threshold voltage (extracted at 100 pA × W L^{-1}) as a function of stress time for devices (d) without and (e) with HfO_2 under different positive bias fields. f) Proposed mechanism for the PBS-induced V_{TH} shift: hydrogen migration from the dielectric to the channel causes a negative shift (step 1), whereas electron trapping at dielectric defects leads to a positive shift (steps 2, 3). g) V_{TH} shift under negative bias stress with varying field strength; the inset shows the NBS-induced change in carrier concentration. h) Photocurrent ($I_{light} - I_{dark}$) as a function of the overdrive voltage ($V_{BG} - V_{TH}$) under 450 and 405 nm illumination. i) Mechanism of NBS-induced V_{TH} shift: oxygen vacancy ionization in the channel causes a negative shift (step 1); electron trapping in the passivation layer results in a positive shift (step 2).

mechanisms: the trapping of positive charges (such as V_O^{2+}) in the dielectric, and an increase in carrier concentration due to donors such as oxygen vacancies and hydrogen.[48–49,58–59] The behavior of the transconductance (g_m) curve over stress time helps distinguish the two mechanisms. As shown in Figure S14 (Supporting Information), the simultaneous increase in the g_m peak and negative shift rules out positive charge trapping in the dielectric—which typically causes only a negative g_m shift—and suggests a dominant role of increased carrier concentration from donors.[59]

Further study is needed to pinpoint the specific donors influencing carrier concentration. The variation in carrier concentration before and after NBS testing was evaluated using the equation: $n_{2D} = I_{DS} L / (q W V_{DS} \mu_{FE})$, where I_{DS} is the on-state current, L and W are the channel length and width, respectively, q is the electron charge, V_{DS} is the source–drain voltage, and μ_{FE} is the field-effect mobility (Figure S15, Supporting Information).[62] As shown in the inset of Figure 2g, the calculated changes in carrier concentration—with and without HfO_2 passivation—were compared at a fixed overdrive voltage (V_{BG-} V_{TH}). The passivated device exhibited a 20-fold reduction in carrier concentration, indicating a corresponding decrease in the defect density responsible for supplying carriers (Note that the carrier concentration does not necessarily equal the defect concentration, as some defects can provide more than one electron). On the basis of these findings, hydrogen impurities can be excluded as the dominant source of the negative threshold voltage shift under NBS. As noted earlier, HfO_2 passivation reduces the hydrogen content by less than an order of magnitude—insufficiently to account for the observed instability. Attention thus turns to deep-level oxygen vacancy defects inherent in the oxide material. To quantify changes in the oxygen vacancy concentration,

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light-induced current–voltage measurements were performed under 450 nm (2.8 eV) and 405 nm (3.1 eV) illumination, corresponding to energy levels associated with oxygen vacancies below the conduction band.[39] Photoexcitation promotes electrons from these defects into the conduction band, increasing carrier density and output current, as described by $I_{ph} = nq\mu E$ (where I_{ph} is the photocurrent, n is the photo-induced carrier concentration, q is the electron charge, μ is the mobility, and E is the electric field between source and drain). As shown in Figure 2h, the passivated device exhibited a 23–25-fold reduction in photoconductive current, with little dependence on the optical power or wavelength (Figure S16, Supporting Information). This reduction strongly correlates with the decrease in carrier concentration under NBS, confirming that deep-level oxygen vacancies are the primary cause of the negative V_{TH} shift under negative bias stress.

The physical mechanism underlying negative bias stress (NBS) behavior is summarized as follows. As shown in Figure 2i, under a negative gate bias, the energy bands bend upward, increasing the conduction band minimum. Although band bending intensifies with increasing bias, it eventually saturates—as confirmed by the simulation in Figure S17 (Supporting Information)—beyond which the conduction band energy remains constant.[63] This saturation explains the bias-independent nature of the NBS-induced threshold voltage shift. The application of a negative gate bias shifts the Fermi level toward the valence band, enabling deep-level oxygen vacancies located above it to ionize and release electrons into the conduction band ($V_O \rightarrow V_O^{2+} + 2e$), thereby inducing a negative V_{TH} shift. When a positive voltage is applied, the ionized oxygen vacancy (V_O^{2+}) can recapture electrons from the conduction band, thereby exhibiting reversible behavior (Figure S14, Supporting Information).[61] Additionally, we attribute the slight positive V_{TH} shift in passivated devices under NBS to carrier trapping within the passivation layer. Consider a transient process: initially, under a negative bias, electrons are driven toward the passivation layer and become trapped. After a period, the channel enters a depleted state, which eventually suppresses further trapping due to the scarcity of available electrons. Since trapping occurs only at the initial stage, the positive shift in the threshold voltage rapidly saturates, as confirmed by the data shown in Figure S18 (Supporting Information).

Passivation reduces the density of these oxygen vacancies by approximately an order of magnitude (since each vacancy can release two electrons); this reduction strongly suppresses ionization and significantly improves NBS stability. High-temperature NBS tests further confirmed the efficacy of this approach, with passivated devices showing exceptional stability ($\Delta V_{TH} < 25$ mV, see Figure S19, Supporting Information). Our straightforward passivation strategy delivers dual benefits: it reduces shallow defects to enhance carrier mobility, while effectively lowering oxygen vacancy density and partially reducing the hydrogen content, thereby substantially improving bias stability.

2.3. IGO 2T0C DRAM Retention Characteristics

To evaluate the impact of bias stability on the retention performance of capacitorless DRAM, write and read operations were tested on IGO 2T0C DRAM cells with and without HfO_2 passivation. **Figure 3a** presents the voltage timing sequence for write/read operations along with the corresponding variation in the read transistor current (I_{RBL}). In Region 1, the write operation begins by applying a positive voltage to the WWL to turn on the write transistor, followed by a positive WBL voltage that injects a positive charge into the storage node (SN). This accumulated charge immediately activates the read transistor, increasing the I_{RBL}. The write process is complete when the SN potential reaches the WBL voltage, at which point the I_{RBL} stabilizes. Region 2 marks the start of the retention phase: the WWL is switched to a negative voltage (V_{hold}) to turn off the write transistor, and the WBL is disconnected. Continuous monitoring of the I_{RBL} enables tracking of the charge retained at the SN over time. To enable readout, the I_{RBL} is converted to an SN voltage (V_{SN}) via a pre-calibrated V_{SN}–I_{RBL} relationship (Figure S20, Supporting Information).

Importantly, during the holding phase, the value of the V_{SN} closely approximates that of V_{WBL}. This similarity results from intentionally minimizing the overlap between the gate and source/drain electrodes in the transistor design, as shown in the inset of Figure 3c. As demonstrated in Figure S21 (Supporting Information), overlap between the gate and source/drain electrodes introduces parasitic capacitance. This parasitic capacitance causes the potential of the SN to be affected by the voltage signals at the WWL and RBL ports via capacitive coupling. Consequently, when the voltages at these ports decrease, the potential of the SN decreases proportionally, with the proportionality constant directly related to the magnitude of the parasitic capacitance. The absence of overlap in the design substantially mitigates the effect of parasitic capacitance on the SN potential (Figure S22, Supporting Information). The minor residual potential drop may be attributed to mobile electrons accumulated in the channel and electrons trapped by defects.[60]

Figure 3b,c presents the time-dependent decay of V_{SN} in 2T0C DRAM cells without and with HfO_2 passivation, respectively. Both DRAM cells exhibit a temporal decay in V_{SN}, reflecting progressive charge leakage. As V_{hold} becomes more negative, the transistor turns off more completely, thereby reducing the leakage current and slowing the V_{SN} decay. The retention time is defined as the duration required for V_{SN} to drop by 0.1 V from its initial value. As shown in Figure 3d, the retention time varies with V_{hold} in distinct patterns for passivated and unpassivated cells. On a semi-logarithmic scale, passivated devices exhibit a highly linear dependence on V_{hold}, whereas unpassivated devices deviate significantly from this trend. Since retention time is governed by the off-state leakage current (I_{OFF}), it can be expressed as $I_{OFF} = 0.1\ V \times C_{SN} / t_{ret}$, where C_{SN} is the gate capacitance of the read transistor and t_{ret} is the retention time. Analyzing the I_{OFF}–V_{hold} relationship enables interpretation of the differing retention behaviors between the two types of devices.

As illustrated in Figure S23 (Supporting Information), charge stored in the SN can leak through multiple pathways, including gate leakage, tunneling leakage, and subthreshold leakage (dominated by thermal emission).[63] On the basis of the theoretical behavior of leakage mechanisms, both gate leakage and tunneling leakage are expected to increase under more negative gate

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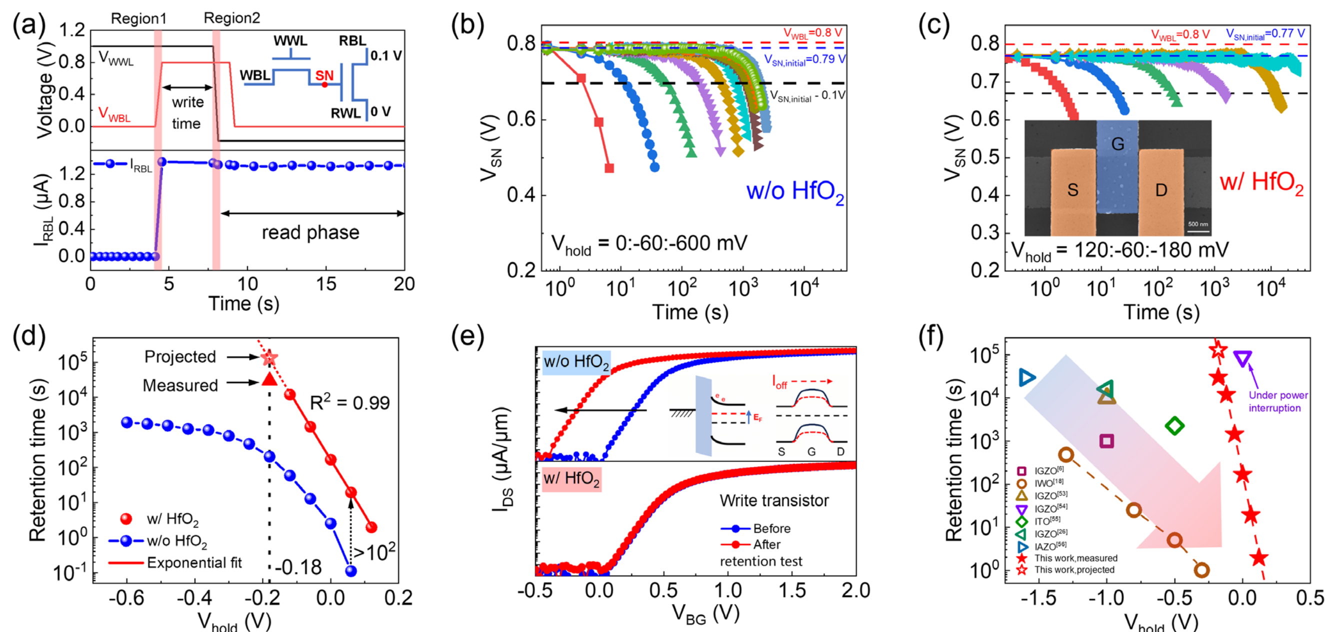

Figure 3. Data retention comparison of IGO 2T0C DRAM with and without HfO_2. a) Voltage timing diagram for write and read "1" operations, showing the corresponding read transistor current (I_{RBL}). The RBL and RWL are held at 0.1 and 0 V, respectively. Region 1 indicates the start of writing; Region 2 marks the beginning of reading (or holding). The interval between regions defines the write time. b, c) Storage node voltage (V_{SN}) over time at different hold voltages (V_{hold}) after writing "1" for devices (b) without and (c) with HfO_2. d) Retention time (defined as the duration for V_{SN} to drop by 0.1 V) versus V_{hold} for devices with and without HfO_2. The extrapolated retention time reaches ≈10^5 s at V_{hold} = −0.18 V. e) Transfer characteristics of write transistors before and after retention tests for unpassivated and passivated devices. The inset shows the mechanism of the NBS-induced I_{OFF} increase. f) Benchmark of the 2T0C DRAM retention time from this work versus other oxide semiconductors. Solid red pentagrams: experimental data; hollow pentagrams: predicted retention times.

voltages. In contrast, the subthreshold leakage current decreases under such conditions, as a higher negative gate voltage increases the conduction band minimum, thereby increasing the energy barrier for the thermal emission of electrons from the source. Since our experimental results show a clear reduction in the total leakage current with increasing negative gate bias, we conclude that subthreshold leakage constitutes the dominant leakage mechanism in these devices. The quantitative behavior of the subthreshold current is captured by the subthreshold slope (SS) extracted from the transfer curve, which reflects the linear dependence of the logarithm of subthreshold current on the gate voltage. This behavior aligns with the linear semi-logarithmic relationship observed between retention time and V_{hold} in passivated devices. As shown in Figure S24 (Supporting Information), the calculated I_{OFF}–V_{hold} relationship for a passivated 2T0C DRAM cell reveals that a 63.4 mV reduction in V_{hold} reduces I_{OFF} by one order of magnitude—closely matching the measured SS value of 62.9 mV dec^{-1}. This agreement further confirms that subthreshold leakage is the primary contributor to charge loss in these devices.

The nonlinear relationship between log(I_{OFF}) and V_{hold} in unpassivated DRAM cells indicates the presence of an additional mechanism contributing to increased leakage. Figure 3e compares the transfer characteristics of the write transistor before and after the retention test. The passivated device shows negligible change, reflecting its excellent stability under negative bias stress (NBS), whereas the unpassivated device clearly exhibits a negative shift in threshold voltage. This difference explains the deviation from linearity in the retention time–V_{hold} relationship observed in unpassivated 2T0C DRAM cells. Under negative V_{hold}, unpassivated devices experience NBS-induced degradation, where ionization of oxygen vacancies increases the carrier concentration. This raises the Fermi level toward the conduction band, thereby reducing the energy barrier for the thermal excitation of electrons. The consequent increase in subthreshold leakage current shortens the retention time. The retention behavior at 85 °C followed the same trend as at room temperature for both passivated and unpassivated DRAM cells (Figure S25, Supporting Information), although the retention time decreased at elevated temperatures under equivalent conditions. These results underscore that high NBS stability is essential for achieving the predicted long retention behavior in 2T0C DRAM cells.

Figure 3f and Table S2 (Supporting Information) compare the retention performance of our IGO 2T0C DRAM with that of other oxide-based 2T0C DRAMs under various V_{hold} values.[6,18,26,53–56] Our HfO_2-passivated DRAM achieves a retention time exceeding 30000 s under continuous power—the best reported value under such operating conditions. This performance stems not from a general reduction in I_{OFF}, but from the suppression of the NBS-induced I_{OFF} increase enabled by enhanced bias stability, allowing the intrinsic low-leakage characteristics of IGO to be maintained even near V_{hold} = 0 V without requiring more negative bias. The theoretical retention time (≈10^5 s) surpasses that under power-interrupted conditions (9 × 10^4 s).[54] Further increasing the threshold voltage of IGO FETs is expected to extend retention at V_{hold} = 0 V, paving the way toward true nonvolatile memory.

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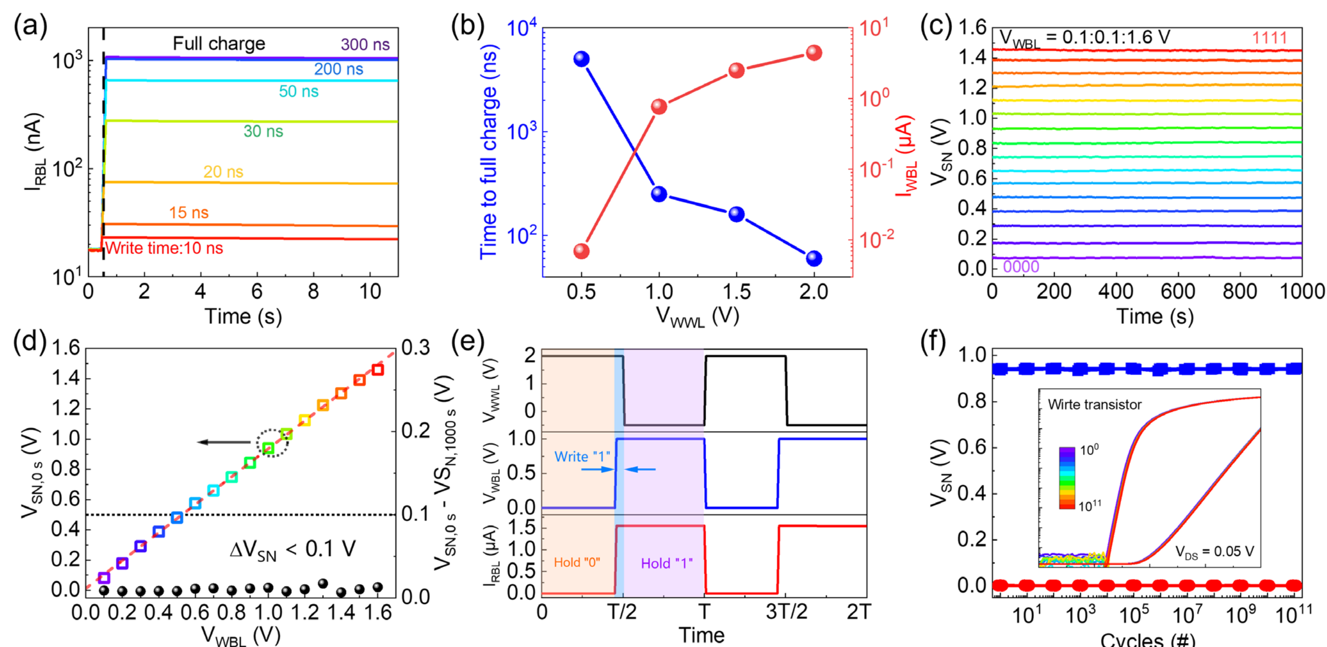

Figure 4. High-speed, multi-bit, and enduring performance of IGO 2T0C DRAM. a) I_{RBL}–time characteristics after writing "1" with write times from 10 to 300 ns. The black dashed line indicates the start of writing. b) Charge fill time and I_{WBL} as a function of V_{WWL}. Improving write transistor performance increases write speed. c) Temporal evolution of V_{SN} for 16 memory states, programmed by varying V_{WBL} from 0.1 to 1.6 V in 0.1 V steps. d) V_{SN} at 0 s and the voltage drop after 1000 s ($V_{SN,0\,s} - V_{SN,1000\,s}$) versus V_{WBL}. $V_{SN,0\,s}$ shows strong linear correlation with V_{WBL}; all 16 states retain a voltage drop below 0.1 V after 1000 s. e) Voltage timing sequence for write–read–hold operations. The cycle (write "0"–hold "0"–write "1"–hold "1") is repeated to evaluate endurance. f) V_{SN} values for logic "1" and "0" as a function of read/write cycles, measured across five devices. The V_{SN} values remain stable after 10^{11} cycles with no significant degradation. The transfer characteristics of the write transistor also show negligible variation after cycling.

2.4. IGO 2T0C DRAM Write Speed, Multi-Bit Storage, and Endurance

We further evaluated the write speed, multi-bit storage capability, and endurance of the HfO_2-passivated IGO 2T0C DRAM cell. The write speed was characterized by varying the write pulse duration from 10 to 300 ns. As shown in **Figure 4a**, the read current (I_{RBL}) increases with extended write time and exceeds its pre-write level even at 10 ns, confirming successful charge injection into the storage node. The saturation of the I_{RBL} beyond 200 ns indicates complete charging of the node. The full charging time can be further shortened by increasing the on-state current (I_{ON}) of the write transistor (Figure 4b and Figure S26, Supporting Information). These results collectively demonstrate the feasibility of 2T0C DRAM for high-speed memory applications.

The 2T0C DRAM architecture enables multibit storage by programming distinct charge states within a single memory cell, substantially increasing the storage density. By adjusting the V_{WBL}, the charge stored at the storage node (SN) is modulated, producing well-separated readout current levels. These analog current values encode multiple logic states, establishing the foundation for multibit operation. Figure 4c shows the temporal evolution of 16 clearly resolved V_{SN} levels, obtained by varying V_{WBL} from 0.1 to 1.6 V in 0.1 V steps. A strong linear correlation between V_{SN} and V_{WBL} is demonstrated in Figure 4d. All 16 states maintain a voltage drop below 0.1 V after 1000 s, indicating excellent retention during multibit operation. This linear behavior suggests that higher storage capacity can be achieved by reducing the voltage step size. However, practical implementation requires careful consideration of the read margin: smaller voltage steps lead to narrower distinctions between read current levels. This issue is compounded by device-to-device variations across the memory array, which further disperse readout signals. An insufficient read margin may render logic states indistinguishable, resulting in read failure.[53,60]

Durability under frequent write/read operations is a critical requirement for DRAM. To evaluate the endurance of our 2T0C DRAM cell, we applied a write–read–hold voltage sequence (Figure 4e), which cycles through writing "0", holding "0", writing "1", and holding "1" in a single operation. The RBL and RWL were biased at 0.1 and 0 V, respectively, to enable continuous readout—a more stringent condition than typical operation. As shown in Figure 4f, the V_{SN} levels for "1" and "0" remain stable through 10^{11} read/write cycles across five different devices, providing statistical evidence of excellent endurance uniformity. No significant degradation was observed in any of the measured devices. Consistent performance is also maintained in the transfer characteristics of the write transistors, and Figure S27 (Supporting Information) further confirms that the device parameters vary by less than 5% after the same number of cycling, meeting durability testing standards.[6,64] These results collectively demonstrate the robust and reproducible endurance of our DRAM technology.

3. Conclusion

In summary, we have successfully realized ultra-stable IGO FETs through HfO_2 passivation while simultaneously

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improving their electrical performance. This approach comprehensively suppresses multiple types of defect: the reduction in shallow-level defects enhances the field-effect mobility to 35 $cm^2V^{-1}s^{-1}$; the suppression of deep-level oxygen vacancies significantly improves the negative bias stability, limiting the threshold voltage shift to within +5 mV after 3600 s under −5 MV cm^{-1}; and the decrease in hydrogen impurities in the dielectric enhances the positive bias stability. These combined effects effectively mitigate oxygen vacancy ionization under negative bias and hydrogen migration under positive bias, ensuring reliable operation across both room and elevated temperatures.

The 2T0C DRAM constructed using these highly stable IGO FETs demonstrates a retention time exceeding 30 000 s, with theoretical predictions reaching 10^5 s. The implementation of 4-bit multi-level storage enables substantial capacity enhancement without increasing the physical cell count, while maintaining a retention time of 1000 s for each storage state. This work provides crucial insights into defect engineering for achieving ultra-long retention, fast writing (10 ns), multi-bit operation, and extended endurance (10^{11} cycles) in oxide semiconductor-based memory, thereby establishing a solid foundation for the development of next-generation high-density DRAM technologies.

4. Experimental Section

Device Fabrication: A silicon substrate with a 300 nm SiO_2 layer was cleaned using the RCA method. A gate electrode pattern was then defined by electron beam lithography (EBL), followed by electron beam evaporation (EBE) of a 3 nm Ni / 15 nm Pt stack. A 10 nm HfAlO gate dielectric (Hf: Al = 9:1) was deposited via atomic layer deposition (ALD) at 300 °C using TEMAHf, TMA, and O_3 as precursors. A 3.6 nm IGO channel (In: Ga = 1:1) was subsequently deposited by ALD at 225 °C using TMGa, TMIn, O_3, and H_2O as precursors. The channel was isolated by etching with dilute hydrochloric acid. Interconnect windows were opened by reactive ion etching (RIE) after patterning with EBL. Source/drain and interconnect metals (15 nm Ni / 15 nm Au) were deposited simultaneously via EBE. Finally, a 4 nm HfO_2 passivation layer was grown by ALD at 250 °C using TEMAHf and O_3 under oxygen-rich conditions to effectively passivate defects and enhance device stability.

Device Characterization: The devices were placed under vacuum in an electrically shielded probe stage (Lakeshore TTPX). Electrical tests were performed via Keysight's B1500A semiconductor parameter analyzer, and SPGU modules were used for DRAM speed tests.

Statistical Analysis: The experimental results are presented with mean ± standard deviation calculated by Origin 2021, if applicable. As shown in Figure S5 (Supporting Information), for the statistical V_{TH}, subthreshold swing (SS), I_{on}, and mobility (μ_{FE}), 10 IGO FETs with HfO_2 and 11 IGO FETs without HfO_2 were used. Origin 2021 software was used to conduct Gaussian fitting to determine the mean and standard deviation values.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Author Contributions

X.L. conceived and supervised the research. J.L. designed the experiments. C.Y. advised and assisted in the growth of the IGO film. J.L. performed the material characterization and analysis. J.L. carried out the fabrication of the 2T0C DRAMs, measurements, and analysis of the data. L.Z. contributed to the measurement methods. All the authors discussed the results and contributed to the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

capacitorless DRAM, indium-gallium oxide, reliability, surface passivation

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