The Impact of Parasitic Capacitance on the Memory Characteristics of 2T0C DRAM and New Writing Strategy

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***Abstract*— In this work, we systematically study the impact of capacitive coupling effect on the memory characteristics of 2T0C DRAM by both theoretical modeling and experiments. Then, based on the insights on capacitive coupling, we propose a new writing strategy for 2T0C DRAM, which can effectively enhance the memory window and retention at the same operation voltage. Finally, we demonstrate a high performance ZnO-based 2T0C DRAM cell with retention >1000 s under criterion of $\Delta V_{SN} = 0.1$ V. Through the proposed new method, the retention of 2T0C DRAM cell can be improved from 1200 s to >10000 s under criterion of V_{SN} drop to a failure voltage of 0.5 V.**

***Index Terms*— Zinc oxide, oxide semiconductor, thin-film transistor, capacitorless DRAM, capacitive coupling effect.**

I. Introduction

OXIDE semiconductor based 2T0C dynamic random-access memory (DRAM) is considered as a promising candidate for DRAM technology with the capability on monolithic 3D integration, taking advantage of its long retention time and area efficiency [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. Most research have focused on improving the performance of 2T0C DRAM by material and device engineering for lower leakage current and novel architectures [6], [7], [8], [9], [10], [11]. However, the problem of capacitive coupling in 2T0C DRAM cell has been raised [7] but has not been fully understood. The capacitive coupling effect causes a sharp voltage drop on the storage node voltage (V_{SN}), which results in narrower memory window and higher operation voltage than expected, which limited the performance improvement.

In this work, the impact of capacitive coupling effect on the memory characteristics of 2T0C DRAM is systematically studied by both theoretical modeling and experiments. The impact of capacitive coupling on the storage node voltage (V_{SN}) are derived mathematically. It is found the unintentionally V_{SN} change (ΔV_{SN}) during read and write in 2T0C DRAM cell is determined by write word line (WWL) to storage node (SN) capacitance ($C_{WWL\text{-}SN}$) and read word line (RWL) to SN capacitance ($C_{RWL\text{-}SN}$) coupling. Based on the theoretical model, a new writing time sequence of 2T0C DRAM is proposed, utilizing the capacitive coupling to enhance the memory performance. Finally, a high performance ZnO FET-based 2T0C DRAM cell with retention of 1100 s under criterion of $\Delta V_{SN} = 0.1$ V is demonstrated experimentally. Through the proposed new writing strategy, retention of 2T0C DRAM cell can be improved to >10000 s under criterion of V_{SN} drop to a failure voltage (V_F) of 0.5 V.

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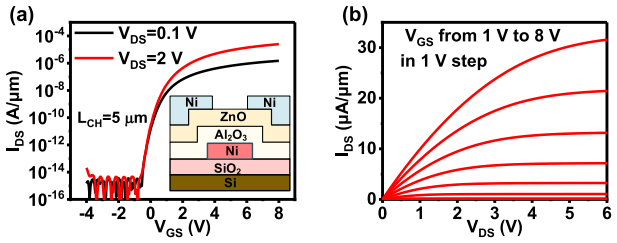


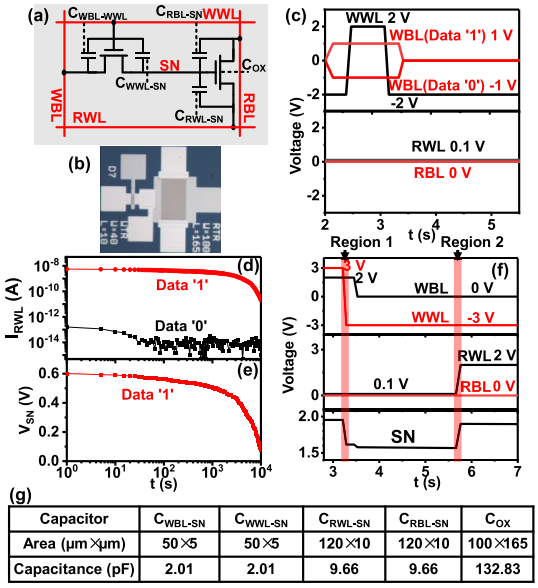
Fig. 1. (a) I_D-V_{GS} characteristics of a planar ZnO transistor with L_{CH} of 5 μm and the schematic diagram on the cross-section of a ZnO transistor. (b) I_D-V_{DS} characteristics of a planar ZnO transistor with L_{CH} of 5 μm.

II. Experiments

Fig. 1(a) presents the schematic diagram of a back-gate ZnO transistor and the I_D-V_{GS} characteristics, exhibiting a field-effective mobility (μ_{FE}) of 31.5 cm^2/Vs. The gate stack includes Ni as gate metal, Al_2O_3 as gate insulator, ZnO as semiconducting channel by atomic layer deposition (ALD) and Ni as source/drain (S/D) contacts. The fabrication of ZnO transistor and 2T0C DRAM is similar as previously reported in [14]. Fig. 1(b) shows the I_D-V_{DS} characteristics of a typical ZnO transistor. The 2T0C DRAM cell consists of two ZnO transistors with different sizes, as shown in Fig. 2(b). All electrical measurements were done with a Keysight B1500A semiconductor analyzer by source measurement unit.

III. Results and Discussion

Fig. 2(a) presents the circuit diagram of the 2T0C DRAM cell, including write bit line (WBL) to WWL capacitance ($C_{WBL\text{-}WWL}$), $C_{WWL\text{-}SN}$, $C_{RWL\text{-}SN}$ and read bit line (RBL) to SN capacitance $C_{RBL\text{-}SN}$. For write transistor, the channel length (L_{CH}) and width (W_{CH}) are 10 μm and 40 μm. For read transistor, L_{CH} and W_{CH} are 165 μm and 100 μm. Fig. 2(b) exhibits a photo image of a 2T0C DRAM based on ZnO transistor. Fig. 2(c) presents a timing diagram for read and write operations of 2T0C DRAM, as traditional writing



Capacitor	C_{WBL-SN}	C_{WWL-SN}	C_{RWL-SN}	C_{RBL-SN}	C_{OX}
Area (μm×μm)	50×5	50×5	120×10	120×10	100×165
Capacitance (pF)	2.01	2.01	9.66	9.66	132.83

Fig. 2. (a) Circuit diagram of a 2T0C DRAM considering parasitic capacitors. (b) A photo image of a 2T0C DRAM based on ZnO transistor. (c) Traditional timing diagram of write and read operations for 2T0C DRAM. (d) I_{RWL} and (e) V_{SN} versus time characteristics after writing. The retention is about 1100 s under criterion of $\Delta V_{SN} = 0.1$ V. (f) A voltage timing diagram and the corresponding V_{SN} versus time measurements for ΔV_{SN} testing. Region 1 shows C_{WWL-SN} coupling and region 2 shows the C_{RWL-SN} coupling. (g) The information of all the capacitors.

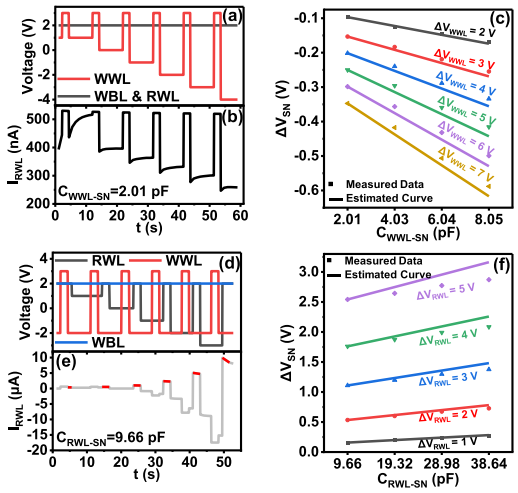


Fig. 3. (a) The specially designed waveform to characterize C_{WWL-SN} coupling. To prevent the impact of C_{RWL-SN} and C_{WBL-SN} coupling, the voltage of WBL and RWL remains at constant 2 V. The high level of each WWL pulse is the same (3 V), and the low level decreases gradually (from 1 V to −4 V in 1 V step). (b) Testing results on I_{RWL}. (c) The relation between ΔV_{SN} and C_{WWL-SN} under different ΔV_{WWL}, containing measured data (discrete points) and estimated curves (solid lines). (d) The specially designed waveform to characterize C_{RWL-SN} coupling. To prevent the impact of C_{WBL-SN} coupling, the voltage of WBL remains at constant 2 V. Each WWL pulse is the same (from −2 V to 3 V). The high level of each RWL pulse is the same (2 V) and the low level decreases gradually (from 1 V to −3 V in 1 V step). (e) Testing results on I_{RWL}. (f) The relation between ΔV_{SN} and C_{RWL-SN} under different ΔV_{RWL}, containing measured data (discrete points) and estimated curves (solid lines).

method. V_{RWL} remains at 0.1 V to monitor the I_{RWL} and V_{SN}. Fig. 2(d) and Fig. 2(e) show the measurement results of read current at RWL (I_{RWL}) and V_{SN} respectively, exhibiting a long retention of 1100 s under criterion of $\Delta V_{SN} = 0.1$ V. V_{SN} can be obtained referring to the I_D-V_{GS} characteristics of the read transistor. The initial V_{SN} is less than 1 V due to capacitive coupling. Fig. 2(f) shows a typical measurement on the impact of capacitive coupling on ΔV_{SN}. The waveform in Fig. 2(f) is used to highlight the V_{SN} change caused by the capacitive coupling effect. It is worth noting that RC effects may also affect V_{SN}change during write operation in high-speed but for simplicity of discussion, this work only focus on quasi-static effect of capacitive coupling. As can be seen, there is an obvious voltage drop at SN due to C_{WWL-SN} coupling and ΔV_{WWL} as illustrated in region 1 and voltage increase at SN due to C_{RWL-SN} and ΔV_{RWL} as illustrated in region 2. Fig. 2(g) shows the information of all the capacitors. The impact of capacitive coupling on V_{SN} is derived, according to voltage divider rule of series and parallel capacitors:

$$\Delta V_{SN} = \frac{\Delta V_{WWL} C_{WWL-SN} + \Delta V_{RWL} C_{RWL-SN}}{C_\Sigma} + \frac{\alpha \Delta V_{RWL} C_{OX}}{C_\Sigma} \quad (1)$$

where $C_\Sigma = C_{WWL-SN} + C_{RWL-SN} + C_{RBL-SN} + C_{OX}$, C_{OX} is the gate oxide capacitance of read transistor, ΔV_{WWL} is the voltage change at WWL and ΔV_{RWL} is the voltage change at RWL. α equals to 0 and 0.5 when the data of the 2T0C DRAM is data '0' and data '1', respectively. When data '0' is loaded, V_{SN} is a low voltage and the read transistor is in off-state, so the C_{OX} is independent of the capacitive coupling effect and $\alpha = 0$. When data '1' is loaded, V_{SN} is a high voltage and the read transistor is turn on. In this case, half of C_{OX} participates in the capacitive coupling effect and $\alpha = 0.5$. Note that in data '1' case, channel resistance may affect α, for the simplicity of discussion, here we assume the channel resistance is low so that can be modelled like a conductor by estimation. According to eqn. (1), ΔV_{SN} due to the capacitive coupling effect mainly consists of two parts: C_{WWL-SN} coupling and C_{RWL-SN} coupling, and C_{WWL-SN} coupling is the major origin of V_{SN} drop in 2T0C DRAM [7], [13]. To reduce the coupling capacitance, such as to use a self-aligned top-gate structure, may effectively alleviate the V_{SN} drop problem, but in some 2T0C DRAM structures, the coupling capacitance cannot be ignored such as channel-all-around IGZO 2T0C DRAM cell with a high density of $4F^2$ in [8].

To further understand the capacitive coupling effect and verify the theoretical model in eqn. (1), pulse measurements with special designed waveforms are performed. Fig. 3(a) shows a waveform with different ΔV_{WWL}. The current at RWL (I_{RWL}) is measured as shown in Fig. 3(b). Fig. 3(c) presents the relation between ΔV_{SN} and C_{WWL-SN} under different ΔV_{WWL}. The other capacitances except C_{WWL-SN} are the same as those in Fig. 2(g). Referring to eqn. (1), the estimated slopes of the ΔV_{SN} versus C_{WWL-SN} curves ($\Delta V_{WWL}/C_\Sigma$) can be calculated. Based on the slopes and the measured ΔV_{SN} of the device whose $C_{WWL-SN} = 2.01$ pF, the estimated curves of ΔV_{SN} versus C_{WWL-SN} are obtained. The small difference between the measured data and estimated curves confirms the theoretical model in eqn. (1). Note that, the intercepts of the estimated curves are not equal to zero, which is caused by other non-ideal effects (such as charge trapping) except capacitive coupling effect. Fig. 3(d) shows the waveform with different ΔV_{RWL}. The corresponding I_{RWL} is presented in Fig. 3(e). Fig. 3(f) presents the relation between ΔV_{SN} and C_{RWL-SN} under different ΔV_{RWL}. The other capacitances except C_{RWL-SN} are the same as those in Fig. 2(g). Like the method

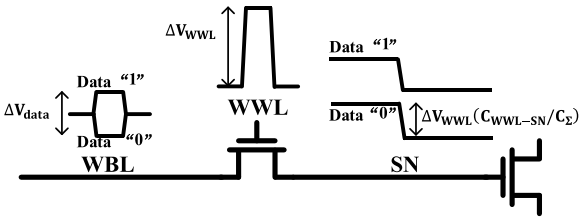


Fig. 4. Illustration of ΔV_{data} on WBL, ΔV_{WWL} on WWL and the corresponding ΔV_{SN} on SN.

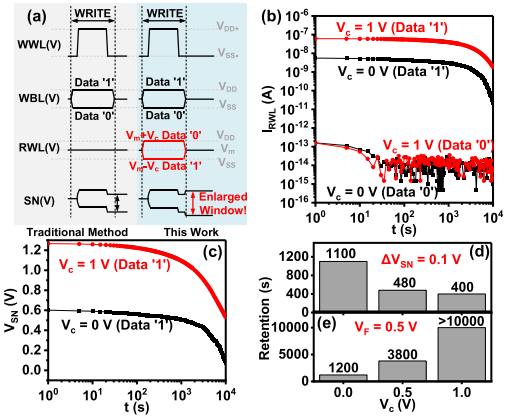


Fig. 5. (a) Writing time sequence of traditional method and the proposed new method. (b) I_{RWL} versus time characteristics after writing at $V_c = 0$ V and $V_c = 1$ V. (c) V_{SN} versus time characteristics at $V_c = 0$ V and $V_c = 1$ V. Retention time at different V_c under criterion of (d) $\Delta V_{SN} = 0.1$ V and (e) $V_F = 0.5$ V.

in Fig. 3(c), the estimated slopes of the ΔV_{SN} versus $C_{RWL\text{-}SN}$ curves ($\Delta V_{RWL}/C_\Sigma$) can be calculated. Based on the slopes and the measured ΔV_{SN} of the device whose $C_{RWL\text{-}SN} = 9.66$ pF, the estimated curves of ΔV_{SN} versus $C_{RWL\text{-}SN}$ are obtained. The linear relation between measured ΔV_{SN} and $C_{RWL\text{-}SN}$ also confirms the theoretical model in eqn. (1).

In above discussion, capacitive coupling effect can have a significant impact on the operation voltage of 2T0C DRAM. The operation voltage, defined as ΔV_{WWL} when turn on/off of the write transistor, which is the largest voltage used in 2T0C DRAM operation, can be expressed as eqn. (2):

$$\Delta V_{WWL} = \Delta V_{data} + \Delta V_{WWL}\frac{C_{WWL\text{-}SN}}{C_\Sigma} = \frac{1}{1-\frac{C_{WWL\text{-}SN}}{C_\Sigma}}\Delta V_{data} \tag{2}$$

where ΔV_{data} is the difference between the voltage level of data '1' and the data '0' at WBL and ΔV_{WWL} is the sum of ΔV_{data} and ΔV_{SN} caused by capacitive coupling, as shown in Fig. 4. As can be seen, the operation voltage is affected by the capacitive coupling factor $C_{WWL\text{-}SN}/C_\Sigma$, so it is essential to reduce the operation voltage by decreasing $C_{WWL\text{-}SN}$. Note that the operation voltage is also affected by the threshold voltage due to voltage lose when transmitting high voltage and off-voltage (V_{OFF}) of the write transistor, but is neglected here for the simplicity of discussion, which does not affect the conclusion.

Utilizing the capacitive coupling effect of $C_{RWL\text{-}SN}$, this work proposed a new writing time sequence to enhance the memory window of the 2T0C DRAM cell. Fig. 5(a) shows the comparison between traditional writing time sequence and the proposed new time sequence. In the writing region, WBL loads data '1' (high voltage level, V_{DD}) and data '0' (low voltage level, V_{SS}). WWL generates a pulse from V_{SS-} to V_{DD+} to turn on the write transistor. RWL remains as measurement voltage (V_m, 0.1 V in this work) to monitor I_{RWL} and V_{SN}. The value of V_m does not affect the measured value of V_{SN}. For the proposed new time sequence, in the writing region, V_{RWL} will swing depending on the data loaded at WBL. When WBL loads data '1', V_{RWL} will be set to ($V_m - V_c$) and when WBL loads data '0', V_{RWL} will be set to ($V_m + V_c$) inversely. Here, V_c is a compensatory voltage. The swing of V_{RWL} contributes to enlarge the voltage window of SN due to the $C_{RWL\text{-}SN}$ coupling as predicted by the capacitive couple equation in eqn. (1). After writing, V_{RWL} remains at V_m to monitor I_{RWL} and V_{SN}. V_{DD} and V_{SS} are related to the operation voltage of DRAM cell and the value of V_c is reasonable when $V_m + V_c \leq V_{DD}$ and $V_m - V_c \geq V_{SS}$.

Fig. 5(b) shows the comparison of I_{RWL} versus time characteristics after writing between traditional writing time sequence (same as Fig. 2(c)) and the proposed new writing time sequence. For data '1', I_{RWL} increases from about 5 nA to about 60 nA by the proposed new write method at the same operation voltage. The corresponding V_{SN} versus time characteristics are shown in Fig. 5(c). The initial V_{SN} is about 0.6 V for traditional method and over 1.2 V for the proposed method in this work, which verifies memory window can be enhanced as predicted. Fig. 5(d) shows the impact of V_c on retention under criterion of $\Delta V_{SN} = 0.1$ V. For traditional method, the ZnO 2T0C DRAM in this work has a long retention time of 1100 s. For $V_c = 0.5$ V and $V_c = 1$ V condition, the retention in this criterion is shorter because of a higher initial V_{SN}.

Note that, criterion of $\Delta V_{SN} = 0.1$ V may not be suitable to compare the retention at different initial V_{SN} because the data lose in DRAM is determined by how much V_{SN} remains in the storage capacitor. So, in this work we propose to use a criterion by V_{SN} decreasing to a failure voltage of V_F. In practical applications, the value of V_F need to be determined by specific technical scenarios. In this work, we chose $V_F = 0.5$ V as an example. Fig. 5(e) presents impact of V_c on the retention characteristics under the new criterion. The retention is improved from 1200 s at $V_c = 0$ V to >10000 s at $V_c = 1$ V, indicating new writing strategy is effective to enhance the retention performance of 2T0C DRAM cell.

This proposed method can effectively enlarge the memory window of 2T0C DRAM without increasing the operation voltage, which can compensate the V_{SN} drop caused by $C_{WWL\text{-}SN}$ coupling. In other words, the proposed writing strategy can reduce the operation voltage without narrowing the memory window, which is important for 2T0C DRAM in applications. It's also worth noting that extra power consumption will appear when adopting the new write scheme due to the additional pulse on RWL. Thus, there will be a tradeoff between memory window and power consumption.

IV. Conclusion

In summary, the impact of capacitive coupling on 2T0C DRAM cell is systematically studied by theoretical model and experiments. A new writing strategy for 2T0C DRAM is proposed according to the theoretical understanding to enhance the memory window and retention. A high-performance ZnO 2T0C DRAM cell with retention >10000 s under criterion of $V_F = 0.5$ V is demonstrated taking advantage of the new writing strategy.

REFERENCES

[1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, "Back-end-of-line compatible transistors for monolithic 3-D integration," *IEEE Micro*, vol. 39, no. 6, pp. 8–15, Nov. 2019, doi: 10.1109/MM.2019.2942978.

[2] S. Li, M. Tian, Q. Gao, M. Wang, T. Li, Q. Hu, X. Li, and Y. Wu, "Nanometre-thin indium tin oxide for advanced high-performance electronics," *Nature Mater.*, vol. 18, no. 10, pp. 1091–1097, Oct. 2019, doi: 10.1038/s41563-019-0455-8.

[3] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, "BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with $I_{on} = 370$ μA/μm, SS = 73 mV/dec and I_{on}/I_{off} ratio $> 4 \times 10^9$," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, Paper TH2.1, doi: 10.1109/VLSITechnology18217.2020.9265064.

[4] M. Si, Z. Lin, Z. Chen, and P. D. Ye, "First demonstration of atomic-layer-deposited BEOL-compatible In_2O_3 3D fin transistors and integrated circuits: High mobility of 113 $cm^2/V\bullet s$, maximum drain current of 2.5 mA/μm and maximum voltage gain of 38 V/V in In_2O_3 inverter," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. T2–T4.

[5] Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim, and H. Hosono, "Mobility–stability trade-off in oxide thin-film transistors," *Nature Electron.*, vol. 4, no. 11, pp. 800–807, Nov. 2021, doi: 10.1038/s41928-021-00671-0.

[6] H. Ye, J. Gomez, W. Chakraborty, S. Spetalnick, S. Dutta, K. Ni, A. Raychowdhury, and S. Datta, "Double-gate W-doped amorphous indium oxide transistors for monolithic 3D capacitorless gain cell eDRAM," in *IEDM Tech. Dig.*, Dec. 2020, pp. 613–616, doi: 10.1109/IEDM13553.2020.9371981.

[7] A. Belmonte, H. Oh, S. Subhechha, N. Rassoul, H. Hody, H. Dekkers, R. Delhougne, L. Ricotti, K. Banerjee, A. Chasin, M. J. van Setten, H. Puliyalil, M. Pak, L. Teugels, D. Tsvetanova, K. Vandersmissen, S. Kundu, J. Heijlen, D. Batuk, J. Geypen, L. Goux, and G. S. Kar, "Tailoring IGZO-TFT architecture for capacitorless DRAM, demonstrating $> 10^3$s retention, $>10^{11}$ cycles endurance and L_g scalability down to 14 nm," in *IEDM Tech. Dig.*, Dec. 2021, pp. 226–229, doi: 10.1109/IEDM19574.2021.9720596.

[8] C. Chen, X. Duan, G. Yang, C. Lu, D. Geng, L. Li, and M. Liu, "Interlayer dielectric engineering for monolithic stacking $4F^2$-2T0C DRAM with channel-all-around (CAA) IGZO FET to achieve good reliability ($>10^4$s bias stress, $>10^{12}$ cycles endurance)," in *IEDM Tech. Dig.*, Dec. 2022, pp. 620–622, doi: 10.1109/IEDM45625.2022.10019502.

[9] J. Guo, K. Han, S. Subhechha, X. Duan, Q. Chen, D. Geng, S. Huang, L. Xu, J. An, G. S. Kar, X. Gong, L. Wang, L. Li, and M. Liu, "A new surface potential and physics based compact model for a-IGZO TFTs at multinanoscale for high retention and low-power DRAM application," in *IEDM Tech. Dig.*, Dec. 2021, pp. 182–185, doi: 10.1109/IEDM19574.2021.9720700.

[10] W. Lu, Z. Zhu, K. Chen, M. Liu, B. M. Kang, X. Duan, J. Niu, F. Liao, W. Dan, X. Wu, J. Son, D. Xiao, G. Wang, A. Yoo, K. Cao, D. Geng, N. Lu, G. Yang, C. Zhao, L. Li, and M. Liu, "First demonstration of dual-gate IGZO 2T0C DRAM with novel read operation, one bit line in single cell, $I_{ON} = 1500$ μA/μm@$V_{DS} = 1$V and retention time>300s," in *IEDM Tech. Dig.*, Dec. 2022, pp. 611–614, doi: 10.1109/IEDM45625.2022.10019488.

[11] Q. Hu, Q. Li, S. Zhu, C. Gu, S. Liu, R. Huang, and Y. Wu, "Optimized IGZO FETs for capacitorless DRAM with retention of 10 ks at RT and 7 ks at 85 °C at zero V hold with sub-10 ns speed and 3-bit operation," in *IEDM Tech. Dig.*, Dec. 2022, pp. 619–622, doi: 10.1109/IEDM45625.2022.10019435.

[12] J. Liu, C. Sun, W. Tang, Z. Zheng, Y. Liu, H. Yang, C. Jiang, K. Ni, X. Gong, and X. Li, "Low-power and scalable retention-enhanced IGZO TFT eDRAM-based charge-domain computing," in *IEDM Tech. Dig.*, Dec. 2021, pp. 462–465, doi: 10.1109/IEDM19574.2021.9720576.

[13] H. Oh, A. Belmonte, M. Perumkunnil, J. Mitard, N. Rassoul, G. L. Donadio, R. Delhougne, A. Furnemont, G. S. Kar, and W. Dehaene, "Enhanced data integrity of In-Ga-Zn-oxide based capacitor-less 2T memory for DRAM applications," in *Proc. IEEE 51st Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2021, pp. 275–278, doi: 10.1109/ESSDERC53440.2021.9631811.

[14] Z. Lin, Z. Wang, J. Zhao, X. Li, and M. Si, "A low-leakage zinc oxide transistor by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 44, no. 3, pp. 536–539, Mar. 2023, doi: 10.1109/LED.2022.3233943.