Al_2O_3/β-Ga_2O_3(-201) Interface Improvement Through Piranha Pretreatment and Postdeposition Annealing

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***Abstract*— In this letter, we report on the improvement of atomic layer deposited (ALD) Al_2O_3/β–Ga_2O_3 (-201) interface quality through piranha pretreatment and postdeposition annealing (PDA). The high quality interface is verified via the temperature dependent capacitance–voltage (*C–V*) and photo-assisted (deep UV) *C–V* measurements, considering its ultra wide bandgap of 4.8 eV for β-Ga_2O_3. A low *C–V* hysteresis of 0.1 V from the measurement frequency of 1 kHz to 1 MHz is obtained, compared with the hysteresis of 0.45 V without piranha optimization. An average interface trap density (D_{it}) of 2.3 x 10^{11} $cm^{-2}\cdot eV^{-1}$ is extracted from the photo *C–V* measurements. Piranha pretreatments and PDA turn out to be an effective way to improve the ALD Al_2O_3/β–Ga_2O_3 (-201) interface for future high quality Ga_2O_3 metal–oxide–semiconductor field-effect transistors.**

***Index Terms*— β-Ga_2O_3, interface, D_{it}, hysteresis, ALD Al_2O_3, piranha, annealing.**

I. Introduction

VERY recently, β-Ga_2O_3 has been considered as a promising candidate for the next generation power electronics due to its ultra wide bandgap (E_g) of 4.8 eV compared with SiC and GaN with bandgap of 3.2 and 3.4 eV, respectively [1]–[8]. Its 4.8 eV bandgap enables the β-Ga_2O_3 to have a theoretical breakdown field (E_c) of 8 MV/cm. Even at such early development stage, a high E_c of 3.8 MV/cm has already been achieved, which exceeds the E_c of GaN and SiC [9]. Combined with the 100 cm^2/V·s room temperature electron mobility (μ), β-Ga_2O_3 possesses a high Baliga's figure of merit of 3444, defined as $\varepsilon\mu E_c^3$ [10]. In addition to its excellent material property, potential cost effective large size substrate can be realized through Czochralski method [11], [12]. However, unlike the GaN HEMT and MOSHEMT with buried channels, β-Ga_2O_3 can only form a depletion-mode MOSFET so far. Therefore, gate dielectric/oxide interface plays an important role in forming high performance MOSFETs. In general, high-k dielectric, high conduction band offset, and high oxide/β-Ga_2O_3 interface quality are major concerns in terms of obtaining high performance device characteristics [13], [14].

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There are several methods to determine the MOS interface trap densities (D_{it}), such as Terman method, hi/lo frequency (f) method and AC conductance method [15], [16]. However, some inherent limitations exist when applying those methods to β-Ga_2O_3 with 4.8 eV bandgap [17]. For instance, inaccurate estimation of the doping concentration and oxide capacitance and the negligence of deep energy level traps lead to underestimation of D_{it} by comparing the ideal C-V curve with high f C-V curve. Hi/lo f method leads to significantly underestimate the D_{it} also since it takes an extremely long time to generate holes in n-Ga_2O_3 so that low f criteria is not satisfied. AC conductance method can only detect shallow energy level (0.2-0.6 eV) D_{it} due to the limited f and temperature (T) ranges to detect the traps deeply inside the bandgap. In addition, the Ga_2O_3 trap capture cross-section σ is still undetermined yet, which makes the trap energy level in the bandgap less accurate. Photo-assisted C-V takes advantage of the ultraviolet (UV) illumination to generate electron-hole pairs in the wide bandgap materials, ensuring that all the traps in the bandgap can respond during the measurement [18], [19]. By comparing the dark high f C-V curve with the post-UV C-V curve, an overall average D_{it} can be obtained from the shift of the two curves.

II. Device Fabrication and Measurement

As received 2 inch Sn-doped β-Ga_2O_3 (-201) was first diced into 6 mm by 6 mm small pieces. The diced samples have been treated with acetone, methanol and isopropanol solvent clean for 30 minutes. Before loading into ASM F-120 ALD chamber, 6 pieces of samples were first pretreated by piranha (98% H_2SO_4: 30% H_2O_2 = 3 : 1) for 1 min. and DI water rinse. 15 nm of Al_2O_3 was then deposited by ALD at 250 °C with tri-methyl-aluminum (TMA) and H_2O as precursors. 2 pieces were then annealed in Jepelec rapid thermal annealing (RTA) furnace for 2 minutes under O_2 and N_2 atmosphere at 500 °C. 3 samples were annealed for 1 minute under O_2 atmosphere at elevated temperatures of 600, 700 and 800 °C, respectively. As a comparison purpose, 3 samples without piranha pretreatment were also deposited with 15 nm of Al_2O_3 at 250 °C, and 2 of them were annealed under the same conditions as the 2 samples with piranha pretreatment above. Serial MOS capacitors (MOSCAPs) were then fabricated with photo

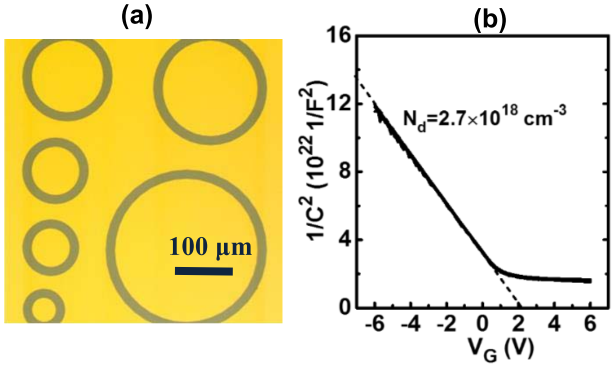

Fig. 1. (a) Top view of Al_2O_3/β-Ga_2O_3 MOS serial capacitors and (b) $1/C^2$ characteristic as a function of V_G with $N_d = 2.7 \times 10^{18}$ cm^{-3}.

lithography followed by Ti/Au (30/70 nm) lift-off process. A high precision HP4284 LCR meter was used for the capacitance measurement. Deep UV light with wavelength of 300 nm was used as the light source of the photo-assisted C-V measurements. The fabricated MOSCAPs were shown in Fig.1 (a), and the doping concentration (N_d) of the β-Ga_2O_3 is extracted to be 2.7×10^{18} cm^{-3} from the slope of $1/C^2$ [20]:

$$N_d = \frac{2}{q\varepsilon_0\varepsilon_s A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}}$$

where the gate electrode area A is 1.96×10^{-5} cm^2, and ε_0 and ε_s of 9.5 are vacuum permittivity and relative dielectric constant of β-Ga_2O_3.

III. Results and Discussion

Fig. 2 shows the f-dependent C-V hysteresis measurements of two optimized samples with and without piranha pretreatments, respectively. The measurements start from depletion to accumulation and then sweep back to depletion. The existence of the interface and bulk traps leads to a shift of the flat-band voltage (V_{FB}) due to the trapping and de-trapping at the bi-directional sweeps. The sweep rate for the C-V hysteresis measurement is 1.0 second per 0.1 V step and the forward to reverse sweep hold time is 10 seconds. With piranha pretreatment, the hysteresis is 0.1 V, while on the other hand the hysteresis is 0.45 V without piranha pretreatment. The trapped electrons or detectable interface trap quantity (Q_{it}) can be roughly estimated through the V_{FB} shift by using the equation: $Q_{it} = C_{ox} \times \Delta V/q$, where $C_{ox} = 0.5$ μF/cm^2 and ΔV are the oxide capacitance and V_{FB} difference, respectively. The Q_{it} is reduced from 1.4×10^{12} cm^{-2} without piranha treatment to 3.2×10^{11} cm^{-2} after treatment. The piranha pretreatment is found to be useful in smoothing the sample surface and removing carbon-based organic contamination [21]. The root mean square (RMS) surface roughness after piranha is 0.17 nm, while the sample without piranha pretreatment is 0.26 nm, as shown in Fig.2 (c) and (d).

Fig.3 summarizes the post deposition annealing (PDA) influences on the piranha pretreated samples. Both room temperature and high temperature (T= 150 °C) C-V curves are presented. Deep depletion behavior is observed due to the wide bandgap of Ga_2O_3 so that inversion layer is not formed

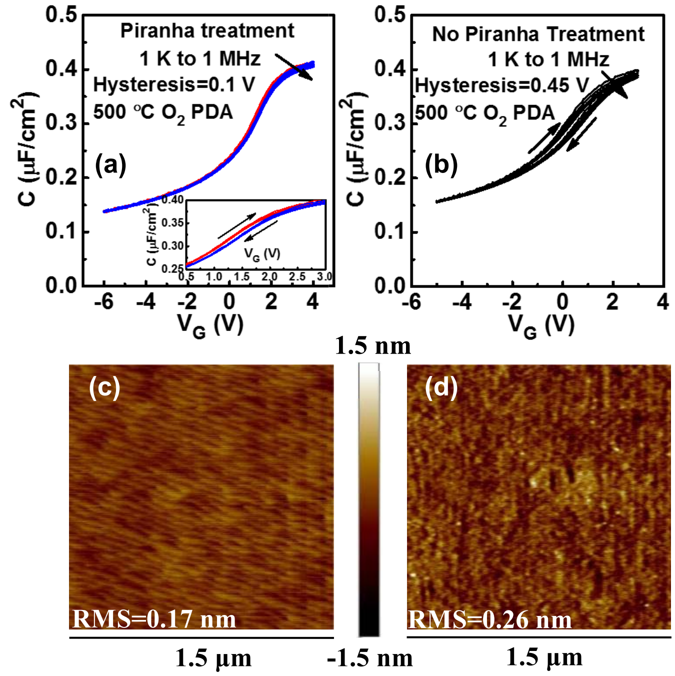

Fig. 2. C-V hysteresis measurement of 2 samples with 500 °C O_2 annealing, (a) with piranha pretreatment and (b) without piranha pretreatment. Fig.2 (a) inset shows the zoomed in view of the C-V hysteresis measurement. (c) and (d) are atomic force microscopy images of β-Ga_2O_3 with and without piranha treatment, respectively.

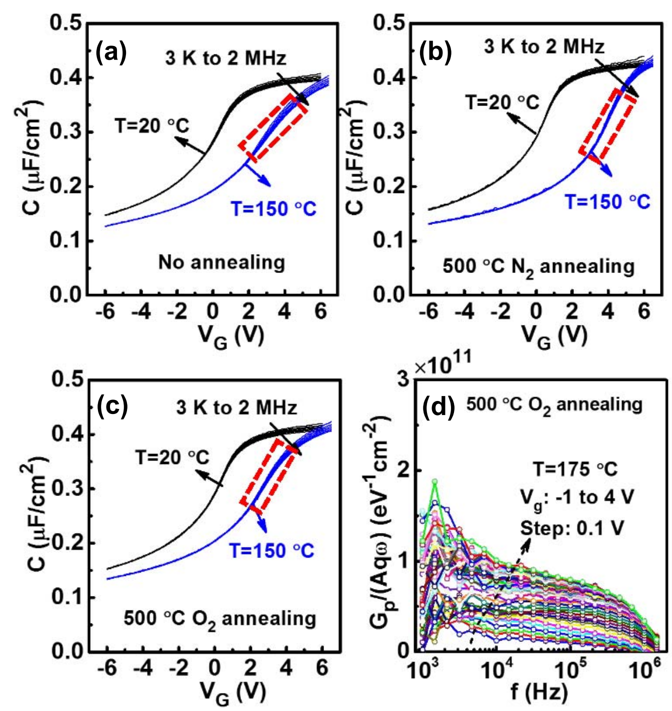

Fig. 3. F-dependent C-V measurements of different PDA MOS capacitors: (a) No annealing, (b) 500 °C N_2 annealing and (c) 500 °C O_2 annealing at T = 20 °C and T = 150 °C and (d) Extracted $G_p/Aq\omega$ at T = 175 °C from AC conductance method. There is no G_p/ω peak at such f and T. The red rectangles in (a), (b) and (c) highlight different f-dispersion under different PDAs. (c) has less annealing temperature dependent V_{FB} shift of 2.5 V compared to 3.5 V shift in (b).

at 3 kHz-2 MHz. At room temperature, there is no significant difference between unannealed and annealed samples with no obvious stretch out near depletion and slight frequency

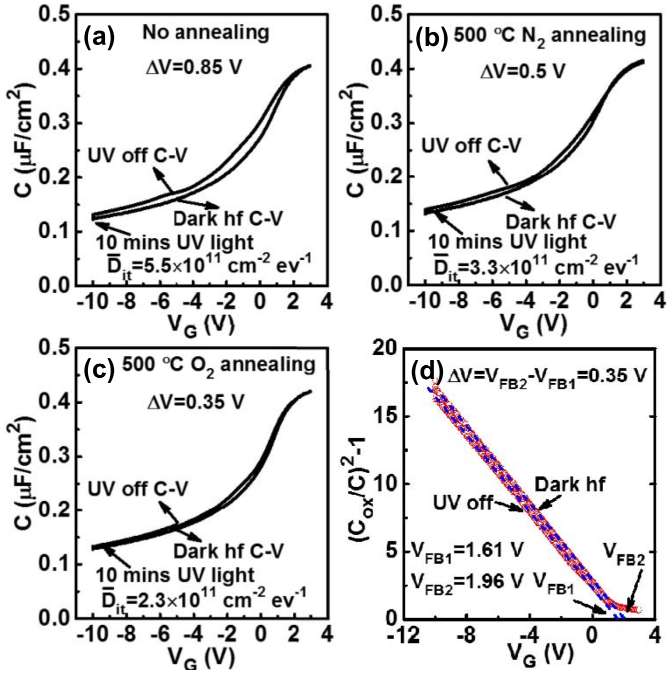

Fig. 4. Photo-assisted C-V measurements of different PDA MOS capacitors: (a) No annealing, (b) 500 °C N_2 annealing, (c) 500 °C N_2 annealing and (d) $(C_{ox}/C)^2 - 1$ as a function of V_G to extract the V_{FB} of sample (c).

dispersion at accumulation. Compared with room temperature C-V curves, there is a right shift of high temperature C-V curves, showing the existence of negative charge at the Al_2O_3/Ga_2O_3 interface. Similar right shift at high temperatures is also observed by Wong *et al.* [2]. Room temperature C-V measurement at accumulation region allow border traps capturing electrons and represent themselves as "negative" fixed charges, which leads the flatband voltage shifted to left compared to the ones measured at high temperatures [14]. One big issue for β-Ga_2O_3 is its low thermal conductivity from room temperature to elevated temperatures, which degrades the device performances, such as electron mobility. The large flatband or V_T shifts are observed at elevated temperatures. At high temperatures, unannealed MOSCAP has higher frequency dispersion compared with annealed ones, as highlighted by the red rectangles, indicating that PDA can help to further increase the interface quality. Moreover, AC conductance method is also used to extract the D_{it} of the MOSCAP. The V_G is limited to the depletion of the MOSCAP. No obvious normalized conductance ($G_p/Aq\omega$) peaks are observed even at T= 175 °C. It is likely that even at this high temperature of 175 °C, the conductance method cannot detect deep trap energy levels in our experiment, since Ga_2O_3 has a wide bandgap of 4.8 eV.

Because of the wide bandgap of Ga_2O_3, photo-assisted C-V method becomes a reliable approach to evaluate the MOS interface and extract the average D_{it}. The measurements started with biasing V_G at accumulation for 10 s to make sure traps are filled with electrons, and then sweeping V_G from deep depletion to accumulation at high f= 1 MHz in dark. Then, V_G is kept biased at deep depletion with V_G =-10 V and deep UV light is on for 10 minutes to generate electron-hole pairs and forcing generated holes to move to the Al_2O_3/Ga_2O_3 interface. After turning off the UV light and then sweeping the C-V from depletion to accumulation again in dark, a UV off C-V curve is obtained. UV generated holes recombine with those trapped electrons so that after UV exposure the interface is "donors" dominated compared to "acceptors" dominated interface without UV illumination. Therefore, a left shift of the C-V curves is observed and this V_{FB} shift can be translated into the average D_{it} by the equation:

$$D_{it} = \frac{C_{ox} \times \Delta V}{q \times E_g}$$

The V_{FB} is determined through the extrapolated line of the $C_{ox}^2/C^2 - 1 \sim V_G$ at $C_{ox}^2/C^2 - 1 = 0$, as shown in Fig. 4 (d) [22]. Fig.4 (a)-(c) describes the originally measured photo-assisted C-V comparisons with dark high frequency C-V curves. The gate leakage currents at both sweeps are limited to 10 μA/cm^2. Both the 500 °C N_2 and O_2 PDA can help to minimize the average D_{it}, which confirms that PDA is needed to optimize the Al_2O_3/β-Ga_2O_3 interface. The improved interface quality after O_2 annealing is related to the compensation of oxygen vacancies [23]. The achieved minimal average D_{it} is 2.3×10^{11} cm^{-2} eV^{-1} with 0.35 V V_{FB} shift. Increased annealing temperature at 600, 700 and 800 °C starts to degrade the interface in our experiments. Both our work and the work from Zeng *et al.* [13] show a decent interface trap density less than 10^{12} cm^{-2}eV^{-1}, which is favorable for device applications. Compared to Ref.[13], we have taken a further step to optimize the interface through piranha pretreatment and PDA, which might be useful to further improve β-Ga_2O_3 MOS interface for device applications.

IV. Conclusion

We have investigated the piranha pretreatment and PDA effects on Al_2O_3/β-Ga_2O_3 (-201) interface through frequency and temperature-dependent and photo-assisted C-V measurements. Low C-V hysteresis of 0.1 V, reduced high-temperature frequency dispersion and reduced V_{FB} shifts are benefited from the improved interface quality. Finally, a low average D_{it} of 2.3×10^{11} cm^{-2} eV^{-1} is achieved through photo-assisted C-V measurements. Piranha pretreatment and PDA process are demonstrated to effectively improve the Al_2O_3/β-Ga_2O_3 interface, making the Al_2O_3/β-Ga_2O_3 (-201) MOS structure possible for future power electronics.

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