High-Performance InAlN/GaN MOSHEMTs Enabled by Atomic Layer Epitaxy MgCaO as Gate Dielectric

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Abstract—We have demonstrated high-performance InAlN/GaN MOS high-electron-mobility-transistors (MOSHEMTs) with various channel lengths ($L_{ch}$) of 85–250 nm using atomic-layer-epitaxy (ALE) crystalline Mg0.25Ca0.75O as gate dielectric. With a nearly lattice matched epitaxial oxide, the interface between oxide and barrier is improved. The gate leakage current of MOSHEMT is reduced by six orders of magnitude compared with HEMT. An off-state leakage current of $3 \times 10^{-13}$ A/mm, on/off ratio of $4 \times 10^{12}$, almost ideal subthreshold swing of 62 mV/decade, low drain current noise with Hooge parameter of $10^{-4}$, and negligible current collapse and hysteresis are realized. The 85-nm $L_{ch}$ MOSHEMT also exhibits good on-state performance with $I_{d,\text{max}} = 2.25$ A/mm, $R_{\text{ON}} = 1.3 \Omega \cdot \text{mm}$, and $g_{\text{max}} = 475$ mS/mm, showing that ALE MgCaO is a promising gate dielectric for GaN device applications.

Index Terms—InAlN/GaN, MOSHEMT, ALE, epitaxial oxide.

I. INTRODUCTION

RECENTLY, GaN-based high-electron-mobility-transistors (HEMTs) have attracted enormous attention in the areas of high frequency [1]–[3], high power [4], high voltage switching [5] and low noise [6] applications. The lattice-matched InAlN/GaN HEMT structure provides a higher two-dimensional electron gas (2DEG) density than AlGaN/GaN structures due to a larger spontaneous polarization difference between the barrier and channel, and minimized short-channel-effects due to a thinner barrier. However, due to its limited Schottky barrier height and thin barrier, devices suffer from high gate leakage ($I_g$).

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resulting in low forward gate bias swing and poor off-state performance. In this case, metal-oxide-semiconductor HEMTs (MOSHEMTs) are proposed with a thin epitaxial oxide layer in between gate and barrier to solve the aforementioned two problems [7]. The MOSHEMT turns out to be an effective way to suppress gate leakage and passivate the surface in the gate-source and gate-drain regions at the same time.

Some progresses have been made on GaN MOSHEMTs, and many gate oxides/dielectrics have been investigated, such as SiO2 [8], SiN [9], [10], Al2O3 [11]–[14], HfO2 [15], La2O3 [16], LaLuO3 [17] and AlN [18]. Although the gate leakage is improved, most of them only yield drain current on/off ratios of $10^{7}$–$10^{10}$, much lower than expected when considering the wide bandgap nature of GaN (3.4 eV). One reason is relatively poor interface between oxide and barrier. In addition, those interface defects also degrade the device low frequency noise performances, with Hooge parameters usually within the range of $10^{-2}$–$10^{-3}$ [19], [20]. In this letter, we have demonstrated a lattice-matched epitaxial MgCaO on the InAlN/GaN MOSHEMT with improved on/off ratio exceeding $10^{12}$ and reduced Hooge parameter of $10^{-2}$.

II. DEVICE FABRICATION AND MEASUREMENT

Fig. 1 shows a schematic view of an InAlN/GaN MOSHEMT on a SiC substrate. The barrier is undoped InAlN and the buffer is undoped GaN without back barrier. It has a sheet resistance ($R_{\text{sh}}$) of $260 \ \Omega/\square$, a 2-dimensional electron gas density of $2 \times 10^{13}$ cm$^{-2}$ and mobility of $1200$ cm$^2$/V$\cdot$s, determined by Hall measurement with ALE passivation. Device fabrication started with mesa isolation by Cl$_2$/BCl$_3$ etching to a depth of 150 nm. Then, Ohmic contacts were formed by depositing Ti/Al/Au (15/60/50 nm) followed by
775 °C rapid thermal anneal in N₂ atmosphere, yielding a contact resistance (Rc) of 0.3 Ω·mm. After that, the wafer was pretreated by diluted BOE (BOE:H₂O=1:5) for 30 s to remove native oxides followed by soaking sample in the NH₄OH solution for 10 min for surface passivation. 4 nm of epitaxial Mg₀.25Ca₀.75O capped with 2 nm of amorphous Al₂O₃ were then deposited by ALE. The Al₂O₃ is used as capping layer to avoid MgCaO absorbing water in the following processes. The growth temperature of MgCaO was 310 °C, using bis(N,N’-di-tert-butylacetamidinato) calcium, bis(N,N’-di-sec-buty lacteamidinato)magnesium, and water vapor as precursors [21]. The ratio of Mg and Ca is controlled by alternating between 1 cycle of MgO and 3 cycles of CaO. A high-resolution TEM image of ALE MgCaO on the InAlN barrier confirms the epitaxial structure of MgCaO as shown in Fig. 1(b). The success of epitaxial growth is determined by X-ray diffraction (XRD) experiment, which provides a high-quality oxide/InAlN interface. Finally, 30 nm of Ni were deposited as the gate metal followed by lift-off process. All the lithography processes were carried out using a Vistec VB6 e-beam lithography system.

All the devices have a gate width of 20 μm, scaled channel lengths (Lch) of 85-250 nm and a source to drain spacing (Lsd) of 1 μm. The gate is centered between the source and drain. The DC measurements were carried out using current amplifier and digital signal analyzer [22].

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the well-behaved output characteristics (Id-Vds) of a GaN MOSHEMT with Lch = 85 nm and Lsd = 1 μm. Due to a 6 nm thick gate oxide, a high forward gate bias (Vgs) of 4 V is applied and thereby a maximum drain current (Idsmax) of 2.25 A/mm is realized at Vds = 9 V. The on-resistance (Ron) of 1.3 Ω·mm is extracted from linear region of Id-Vds. Fig. 2(b) depicts the transconductance (gm) and Id transfer plot in the linear region with Vgs biased from -5 V to 4 V. Despite a wide gate to channel spacing, the GaN MOSHEMT still exhibits a peak extrinsic gm (gmax) of 475 mS/mm at Id = 350 mA/mm and Vds = 5 V. The threshold voltage (VT) is obtained from linear extrapolation of the drain current from the point of peak transconductance, yielding VT = -3.65 V at Vds = 5 V.

Fig. 2(c) is the transfer characteristic at the log-scale plot at Vds = 2.5 V and 5 V. Even with a 85 nm Lch, this device still has a ultra-high on/off ratio of 4 x 10¹² and 4 x 10¹¹ for Vds = 2.5 V and 5 V, respectively. Traditional HEMT devices are not able to have such a high on/off ratio because of their large gate leakage currents (Ids). The Id of the MOSHEMT at off-state is 10⁻¹² to 10⁻¹³ A/mm, which is reduced by 6 orders compared with the Id of a HEMT with the same structure. The MgCaO has conduction band offset of greater than 2 eV with respect to the InAlN barrier [23], allowing 4 nm of MgCaO and 2 nm of Al₂O₃ to provide enough barrier height to minimize the tunneling current from the gate electrode to the 2DEG channel. The high on/off ratio also indicates a high quality oxide/barrier interface, otherwise the channel would not be depleted completely at the off-state.

In addition to the ultra-high on/off ratio, the MOSHEMT also has a low subthreshold swing (SS) of 64 and 68 mV/dec for Vds = 2.5 V and 5 V, respectively. The low SS is mostly from the high quality interface, low equivalent oxide thickness, and ultra-thin thickness of the 2DEG.

Fig. 2(d) describes the Idmax, gmax and SS scaling behavior of GaN MOSHEMTs with Lch of 85-250 nm. Each error bar is the standard deviation of 6 devices on the same chip. On-state performance weakly improves with Lch scales from 250 nm down to 85 nm, since Lsd is much larger than Lch. SS is increased when Lch is scaled, which shows the typical short channel effect. The minimum SS achieved is 62 mV/dec for both forward and reverse sweep. The short channel effects can be further reduced by improving the confinement of the 2DEG in the channel by adding back barriers [24].

Fig. 3(a) shows measured room temperature capacitance-voltage (C-V) at the frequency (f) of 1 K to 2 MHz. The Al₂O₃/MgCaO/InAlN MOS capacitor has a diameter of 75 μm.
As shown in the Fig. 3(a), there is almost zero frequency dispersion in the typical frequency ranges. The dielectric constant of MgCaO is calculated to be \( \sim 10 \) by subtracting the capacitance of the InAlN barrier. By integration of the C-V curve from depletion to accumulation, we can get an ultra-high electron density of \( 3 \times 10^{13} \) cm\(^{-2} \) at \( V_g = 5 \) V. Note that we don’t observe a second sharp increase of the capacitance until we increase \( V_g \) to 5 V, shortly before the oxide failed at \( V_g = 5.5 \) V. The second sharp increase is observed in the oxide (or insulator)/AlGaN systems [13], [16], [25], caused by electrons in the 2DEG channel spilling into barrier. The second capacitance increase is also observed in InAlN MOSHEMT when 2DEG density is up to \( 1.4 \times 10^{13} \) cm\(^{-2} \) [26]. In our devices, we suggest that the negligible introduction of the extra positive charge at the oxide/barrier interface is attributed to the suppression of the 2\(^{nd} \) capacitance increase before \( V_g = 5 \) V. The oxide/barrier positive charge will help to pull down the conduction band of the barrier so that electrons will be easier to spill over the barrier to the oxide/barrier interface to induce the second C-V step. This positive charge is typically observed at the ALD amorphous oxide/barrier interface [11], [27], [28]. To prove this suggestion, we also fabricated ALD amorphous Al\(_2\)O\(_3\)/InAlN/GaN MOS capacitor with 6 nm of Al\(_2\)O\(_3\). Compared with C-V curve of previous MgCaO/InAlN/GaN MOS capacitor, the latter one shows a negatively shifted \( V_T \) and a second C-V step. The negatively shifted \( V_T \) confirms the existence of the positive charges at Al\(_2\)O\(_3\)/InAlN interface, which finally induces the 2\(^{nd} \) C-V step as aforementioned. In our case, MgCaO can effectively confine electrons in the channel even at a high 2DEG density of \( 3.5 \times 10^{13} \) cm\(^{-2} \). This is very favorable to the device operation since electrons will have a much higher mobility in the low bandgap GaN layer compared with a lower mobility in a wider bandgap InAlN layer. Meanwhile, we also carried out AC conductance measurements to extract the measured overall interface trap density (\( D_{it} \)) from 25 °C to 150 °C for both MgCaO and Al\(_2\)O\(_3\) devices as shown in Fig. 3(b). The extracted \( D_{it} \) is within the range of \( 0.5 \) to \( 3.4 \times 10^{11} \) cm\(^{-2} \) eV\(^{-1} \) for the MgCaO sample and \( 0.3 \) to \( 6.0 \times 10^{12} \) cm\(^{-2} \) eV\(^{-1} \) for the Al\(_2\)O\(_3\) sample. Note that the measured overall \( D_{it} \) is neither simply from the dielectric/InAlN interface nor from the InAlN/GaN interface. More experiments and modeling work are needed to distinguish the traps from two different interfaces in the complex GaN MOSHEMT structures.

To analyze the trapping and detrapping phenomena in InAlN/GaN MOSHEMT, 1/f low noise spectra with various drain currents are also measured. Fig. 4 shows the normalized power spectral density with various \( V_g \) and drain current at \( f = 10 \) Hz.

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\[ f = 10 \text{ Hz}, \quad V_{ds} = 0.05 \text{ V} \quad \text{and} \quad L_{ch} = 140 \text{ nm} \]

The Hooge parameter (\( \alpha_H \)) is calculated to be \( \sim 10^{-4} \) by using following equation [29]: 

\[ \alpha_H = \frac{S_{IDS}}{I_{DS} \times q \times \mu \times V_{DS}} \]

where \( q \) is the elementary electron charge and \( \mu \) is the electron mobility of 1200 cm\(^2 \)V\(^{-1} \)s\(^{-1} \). The \( \alpha_H \) of our epitaxial oxide MOSHEMT is comparable to the HEMT (\( \sim 10^{-4} \)) [30], [31]. On the other hand, MOSHEMTs with amorphous gate dielectric usually suffer from relatively high oxide/barrier interface state densities. The carrier trapping between the oxide and barrier resulted in the increase of \( \alpha_T \), with general \( \alpha_T \) value of \( 10^{-3} \) \( \sim 10^{-2} \). The one or two order of magnitudes lower \( \alpha_T \) of epitaxial oxide MOSHEMT is consistent with near zero frequency dispersion C-V data and also further confirms that our lattice-matched epitaxial oxide has an unprecedented high quality interface with the InAlN barrier.

Fig. 5(a) is the pulsed I-V measurement of the device with \( L_{ch} = 140 \text{ nm} \). The pulse width and pulse period are 500 ns and 500 \( \mu \)s, respectively. The quiescent bias points are set at \( (V_{GSQ}, V_{DSQ}) = (−5, 0) \) and \( (−5, 8) \) for gate and drain pulse, respectively. Effective suppression of the current collapse by MgCaO is demonstrated with little difference between the DC and gate and drain pulsed drain currents. Fig. 5(b) is the \( I_{DS}-V_{GS} \) hysteresis measurement of the same device. A negligible hysteresis of 20 mV is observed when \( V_{gs} \) is sweeping from \( V_{gs} = −4.5 \) to 4 V and then sweeping back, which further confirms an ultra-high quality interface between MgCaO and InAlN barrier.

IV. Conclusion

We have experimentally demonstrated an epitaxial oxide InAlN/GaN MOSHEMT by using ALE technique. Benefiting from a lattice-matched interface, the off-state drain leakage current is reduced to \( 3 \times 10^{-13} \) A/mm, yielding a high drain current on/off ratio of \( 4 \times 10^{12} \). A low Hooge parameter of \( 10^{-4} \) is obtained, showing the high quality interface between epitaxial oxide MgCaO and InAlN barrier. In addition, pulse and hysteresis measurements reveal that the current collapse and hysteresis are suppressed. Combined with the high device performance of \( I_{max} = 2.25 \text{ A/mm} \), \( R_{on} = 1.3 \Omega \cdot \text{mm} \), and \( g_{max} = 475 \text{ mS/mm} \), the MgCaO MOSHEMT turns out to be a good candidate for GaN device applications.

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