Ferroelectric FET Based Coupled-Oscillatory Network for Edge Detection

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Abstract—**Coupled-oscillatory networks are an emerging paradigm for efficiently solving optimization problems. In this work, we demonstrate the application of ferroelectric field-effect transistor (FeFET) for energy-efficient coupled-oscillatory networks. A CMOS-compatible FeFET was fabricated having > 1V of hysteresis window and 57 mV/dec of minimum subthreshold swing. With our proposed FeFET oscillator circuits and optimized biasing schemes, a 2× wider synchronization range and up to 276× lower energy per cycle were achieved compared to previous FeFET-based oscillators. Moreover, we employ FeFET coupled-oscillatory network for an edge detection task. Our simulations considering FeFET non-idealities and process variations with a 5-bit quantized image show that the edge detection output closely follows the ideal output.**

Index Terms—**Ferroelectric, FeFET, HZO, CMOS compatible oscillator, synchronization, FeFET coupled-oscillatory network.**

I. INTRODUCTION

COUPLED oscillator networks, motivated by natural phenomena such as human neural system and flashing fireflies [1], has the potential to achieve low energy consumption while being able to efficiently solve optimization problems. However, there is a lack of theoretical analysis of coupled-oscillatory networks, which is indispensable to understand its applicability in different application scenarios. Although such systems can be implemented in standard CMOS, there are several challenges because the CMOS devices do not inherently mimic the oscillators. [2] used Schmitt triggers for oscillators, however, it requires 10 Transistors (T) and 2 Capacitors (C) for a single oscillator circuit, especially, 6T alone are used for Schmitt trigger functionality. Hence, there have been several works which utilize emerging devices for mimicking coupled-oscillator networks. For example, there are spin-torque oscillator (STO) [3]–[5] and metal-insulator transition (MIT)-based
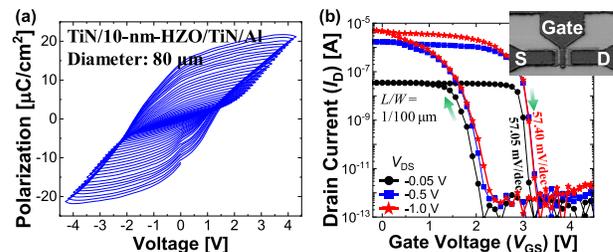
Fig. 1. Experimental results. (a) *P-V* curves of fabricated ferroelectric capacitor and (b) transfer curves of fabricated pFeFET with a SEM image.

oscillator [6]. However, these devices are not Si compatible and have limitations: STO uses current injection as input which induces large energy consumption: VO_2-based oscillator is temperature sensitive [6]. We believe Ferroelectric Field-Effect Transistors (FeFETs) can be a natural choice because of the inherent hysteric polarization-voltage (P-V) characteristics, leading to efficient coupled-oscillatory circuits. Several works have explored FeFET-based coupled oscillators [7]–[9]. For example, the design in [8] used $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) capacitor connected to FET to implement oscillators. However, such designs are difficult to scale. In this letter, we fabricate Si-compatible $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based p-type FeFET (pFeFET) for the design of coupled-oscillators. The proposed FeFET oscillator has 4T and 2C. Note that only one pFeFET and one n-type FET (nFET) are required to mimic the Schmitt trigger operation [9], thanks to the inherent hysteresis of FeFET. The optimum operation regime of the oscillator circuit is examined to secure controllable input range based on a multi-domain FeFET model. Moreover, theoretical approaches for better understanding of these systems are dealt.

II. EXPERIMENTAL DETAILS AND FABRICATION RESULTS

We first fabricated an HZO-based capacitor, the P-V loops of which are shown in Fig. 1(a), validating ferroelectric behavior. Thereafter, a pFeFET was fabricated. After thinning SOI layer by dry oxidation, ion implantation was conducted with As at 35 keV. Active isolation and S/D ion implantation with BF_2 at 35 keV were performed followed by rapid-thermal annealing (RTA) at 1000°. H_2O_2 cleaning was conducted to form SiO_2 interfacial layer. Subsequently, 2-nm Al_2O_3/10-nm HZO/1-nm Al_2O_3 were serially deposited by atomic-layer deposition (ALD). The first Al_2O_3 layer was to prohibit Hf ions from diffusion towards Si which can degrade carrier mobility. As a capping layer of HZO, 1-nm Al_2O_3 and 30-nm TiN were deposited by ALD right on the HZO layer. The top Al_2O_3 layer was to block metal ions from diffusing into
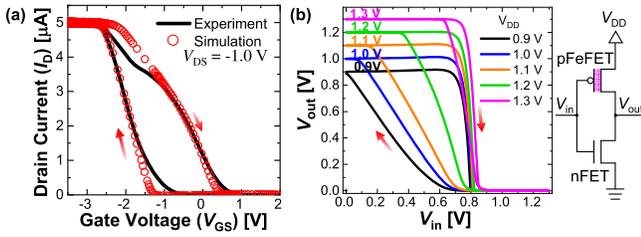
Fig. 2. Simulation results. (a) Model fitting result with experimental data and (b) VTC curves of the inverter composed of one pFeFET and one nFET.

the HZO layer [10]. S/D patterning and Ni deposition were performed. The ferroelectricity activation and silicide were carried out by RTA at 500°C for 30 sec under N_2 ambient. A 10-nm-thick HZO was chosen for FeFET oscillator to secure a sufficient hysteresis window. Fig. 1(b) shows the results of our fabricated device. The full voltage sweep range was from $+6$ V to -6 V. The device has > 1V of hysteresis window and 57 mV/decade of minimum *SS*. Gate leakage current is also well suppressed as low as $<1.3 \times 10^{-10}$ A.

III. DEVICE MODELING AND IMPLEMENTATION OF A SINGLE OSCILLATOR UTILIZING HYSTERESIS OF FeFET

Having a Si compatibility with sufficient hysteresis window are the advantages of the fabricated pFeFET. We utilize the pFeFET in implementing an oscillator circuit. Before that, the experimental data of pFeFET was modeled using predictive technology model (PTM) [11] in conjunction with calibrated Preisach model [12], which is suitable for devices having many grains/domains. Also, the effectiveness of capturing ferroelectric dynamics with Preisach model in transient domain has been verified [13]–[15]. nFETs are also simulated with PTM model. In model parameter calibration, V_{GS} is shifted at the amount of -2.37 V for inverter operation. Fig. 2(a) shows the good agreement of the simulation result with the used models and the experimental data.

Fig. 2(b) shows the voltage-transfer characteristic (VTC) of an FeFET-based inverter where the input voltage (V_{in}) sweep range is between 0 and V_{DD}. Because of the hysteresis effects of pFeFET, VTC curves behave like Schmitt trigger. The similar VTC characteristics can also obtained with nFeFET and pFET. The hysteresis in VTC depends on the relative strength between pFeFET and nFET. For an oscillatory circuit operation, there needs to be a change in the strength of the pFeFET during the forward and reverse sweeps induced by polarization switching, thereby mimicking the Schmitt trigger operation. When V_{in} goes from 0 to V_{DD}, the VTC is mostly driven by the nFET which tries to pull down against the pFeFET. During the reverse sweep, the trip point increases at higher V_{DD} due to stronger pFeFET. Higher V_{DD} flips the polarization of pFeFET more strongly, leading to a stronger pFeFET. This leads to smaller hysteresis in VTC as V_{DD} increases. Unlike typical memory applications of FeFETs, which demand a large change in polarization to achieve high distinguishability between the memory states, the oscillatory circuit operation has relaxed requirements. Even a small change in the pFeFET polarization induces enough hysteresis in the VTC. Hence, the relatively small voltage operation is possible for the oscillator design.

Using the hysteresis effects, an oscillator is designed by introducing an input capacitor (C_{in}), an output capacitor
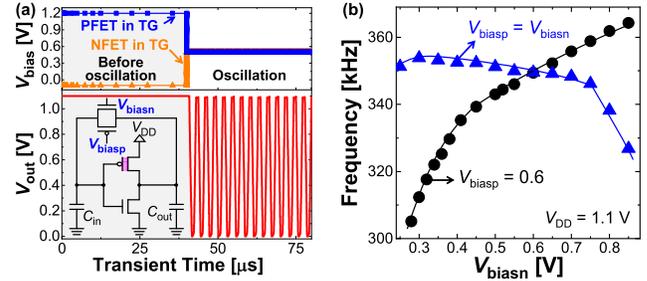

Fig. 3. Single oscillator with FeFET. (a) Pulsing scheme of a single oscillator circuit. (b) f vs. V_{biasn} at $V_{biasp} = 0.6$ V (circle) and at $V_{biasp} = V_{biasn}$ (triangle).
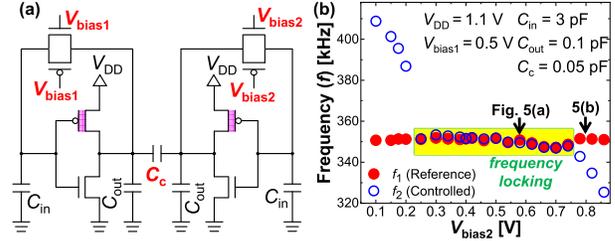

Fig. 4. FeFET coupled oscillator. (a) Schematic of a coupled-oscillator circuit. (b) f vs. V_{bias2} at $V_{bias1} = 0.5$ V.

(C_{out}), and a transmission gate (TG) [9]. The FeFET oscillator circuit and its pulsing scheme are shown in Fig. 3(a). Initially, the TG is turned off and the input node is kept to 0, thereby C_{out} charges to V_{DD}. Once TG is turned on, oscillation is triggered by the interactions between the feedback loop C_{in}-TG-C_{out} and hysteretic VTC. Fig. 3(b) indicates the oscillation frequency (f) controlled by adjusting the gate voltage of TG, V_{bias}. We observe that depending on the TG biasing method, the f range changes differently. With a fixed V_{biasp}, f changes largely by V_{biasn} compared to the case when $V_{bias} = V_{biasp} = V_{biasn}$. For oscillators coupling, the latter scheme is more suitable for synchronization, which occurs when different f's are within a sufficient range.

Moreover, f of the oscillator circuit is modelled as (1).

$$f = \left(2\alpha \cdot \left\{R_{on} \cdot C_{out,eff} + C_{in,eff} \cdot (R_{on} + R_{TG})\right\} + t_{p,LH} + t_{p,HL}\right)^{-1} \quad (1)$$

Here, the factor α relates the (dis)charging delay of C_{in} to the voltage swing at the input node. The on-state resistances (R_{on}) of pFeFET and nFET are assumed to be similar. $C_{in,eff}$ and $C_{out,eff}$ are the effective input and output capacitances, respectively. The delay of the inverter (t_d) for a single oscillation period is the combination of $t_{p,LH}$ and $t_{p,HL}$. $t_{p,LH}$ is the delay when V_{out} changes from low to high; $t_{p,HL}$ is *vice versa*. There are some ways of increasing f with parameters of FeFET: 1) maintaining a thicker t_{FE} since its scaling increases the gate charging time and the actual polarization switching time [16]; 2) the gate length scaling. Energy consumption (E) per cycle of the circuit is also investigated. Operation at V_{DD} up to 1.2 V show E in the range of 0.87–3.97 nJ/cycle, which is at least 29× lower energy consumption compared to [8] (115–240 nJ/cycle). The energy consumption mostly coming from short-circuit current of the oscillator circuit and this draws the difference in energy consumption. Additionally, E of the proposed circuit does not grow linearly as V_{DD}
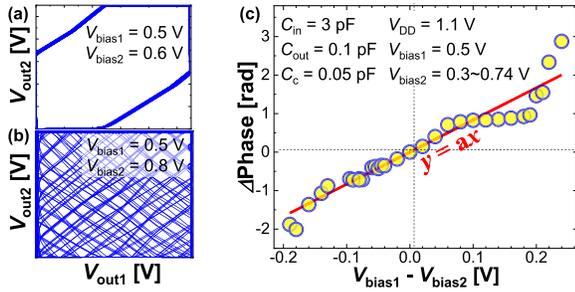
Fig. 5. Phase characteristics of FeFET coupled oscillator when (a) synchronized and (b) asynchronized. (c) Δ Phase within the f locking range.
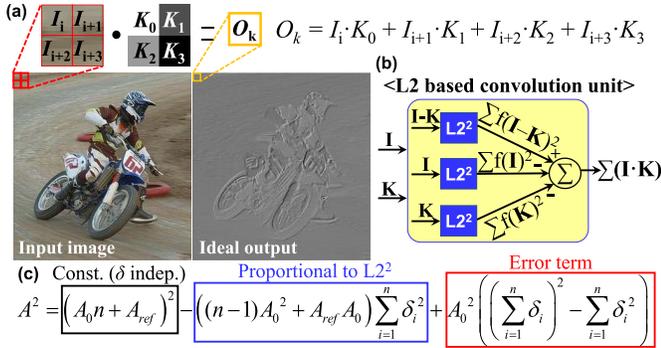

Fig. 6. FeFET coupled-oscillatory network. (a) Convolutional operation from the input image. (Image from PASCAL VOC 2007) (b) Convolution functional block and (c) relation with A and L2.

increases since the major power consuming factor, short-circuit current, is proportional to $(V_{DD} - V_{th})^3$.

IV. FeFET COUPLED OSCILLATOR

Fig. 4(a) shows the circuit of two oscillators being coupled by a coupling capacitor (C_c). Here, one oscillator (Osc$_1$) is considered as a reference and the other (Osc$_2$) is controlled. V_{bias} of Osc$_1$ (V_{bias1}), V_{bias} of Osc$_2$ (V_{bias2}), and C_c are the variables affecting oscillator synchronization. Osc$_1$ and Osc$_2$, initially having different f as f_1 and f_2 due to different V_{bias1} and V_{bias2}, respectively, can be synchronized (*i.e.*, f locking) by C_c. To find out f locking range, V_{bias1} is fixed and V_{bias2} is swept from 0.1 to 0.9 V. Fig. 4(b) depicts how f_2 changes with V_{bias2} at fixed V_{bias1}. Fig. 5(a) and (b) show phase maps when oscillators are synchronized or not, respectively. When V_{bias1} is in 0.35–0.75 V, f locking range of 0.5 V is obtained, which is 2× better compared to [9]. This is due to controlling both gates together in TG as mentioned in previous section. Importantly, phase difference between Osc$_1$ and Osc$_2$ changes linearly within the f synchronization range at fixed V_{bias1} (Fig. 5(c)). This can be used in Euclidean distance (ED, L2 norm) computations [5], and one application is explored next.

V. FeFET COUPLED-OSCILLATOR BASED EDGE DETECTION

Convolutional neural network (CNN) is one of the most important tools for processing visual imagery [17]. Here, we performed edge detection based on CNN with FeFET coupled- oscillatory network, harnessing its phase dynamics in the f locking range. Fig. 6(a)-(c) show the basic computations in CNNs and how they can be mapped on
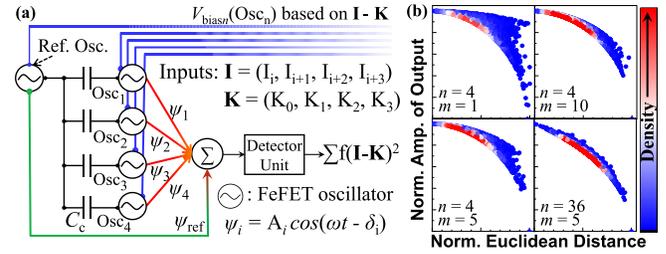

Fig. 7. Coupled-oscillatory network analyses. (a) Single L2 unit. (b) Normalized A vs. L2 plots to reduce error by parameters control. ($A_{ref} = m \times A_i$).
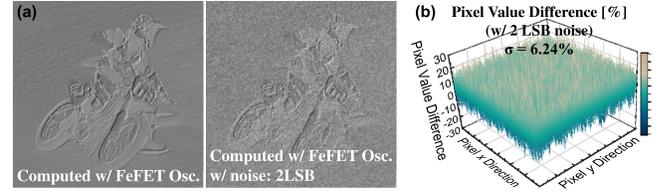

Fig. 8. Computation with FeFET oscillators. (a) Edge detection results and (b) pixel differences between the ideal output and the output from FeFET oscillator network with 2 LSB noise.

FeFET coupled- oscillators. For edge-detection, a 2×2 kernel (Gabor filter) is slided through the input image to generate the output map. For each output pixel, a dot product needs to be computed between the input pixel vector (**I**) and kernel (**K**). This can be achieved by using three L2 units having inputs of **I-K**, **I**, and **K**, respectively (Fig. 6(b)).

Each L2 unit has four FeFET oscillators coupled with a single reference oscillator as shown in Fig. 7(a). The inputs to the L2 unit are mapped into different V_{biasn} within the f locking range, such that each oscillator has the same f but different phases. The outputs of coupled oscillators have the sinusoidal functions (ψ_i) and summed to produce the L2. This summation of ψ_i and the amplitude (A) is confirmed to be proportional to the L2, as per the Harmonic addition theorem [18] and the *cosine* approximation (Fig. 6(c)) [5]. The approximated derived equation in Fig. 6(c) has two ways to mitigate the error term: 1) increasing the amplitude of the reference signal (A_{ref}); 2) increasing the number of oscillators (n). Fig. 7(b) plots the distributions of amplitude for 10,000 sets of vectors **I** and **K**, where the values are randomly chosen in the f locking range. By increasing m and n, the plots become well converged to a parabola.

With the theoretical basis, we perform an edge detection for an image with 5-bit quantization, and the obtained output is in Fig. 8(a). Considering the device non-linearity and process variations, the case having random noise of 2 LSB errors is also included. It is observed that the output with the FeFET oscillator computations closely match the ideal output, with a standard deviation of 6.24% in the pixel values (Fig. 8(b)).

VI. CONCLUSION

An HZO-based pFeFET was experimentally demonstrated having > 1V of hysteresis window and 57 mV/dec of minimum SS. Using the FeFET in our proposed oscillator, we secured a 2× wider f locking range and up to 276× lower E compared to previous works. Linearly increasing phase in FeFET coupled-oscillatory network is mathematically analyzed and an edge detection application is demonstrated.

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