A Low-Leakage Zinc Oxide Transistor by Atomic Layer Deposition

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***Abstract*— In this work, we report an atomic layer deposited (ALD) zinc oxide (ZnO) transistor with low off-state leakage current (I_{OFF}) ~3 x 10^{-18} A/μm at high temperatures up to 147 °C, measured by devices with interdigitated electrodes with a wide channel width (W_{ch}) of 10000 μm, where the low I_{OFF} is still under the detection limit. The impact of ALD growth temperature and annealing on the electrical performance is systematically studied. It is found that low temperature deposition and post deposition annealing are effective to enhance the performance of the ALD ZnO transistors. μ_{FE} as high as 32.8 cm^2/V·s, on/off ratio ~10^{12} and subthreshold slope (SS) down to 75.3 mV/dec at room temperature are achieved. These results suggest ALD ZnO is a promising channel material for low off-state leakage current device applications.**

***Index Terms*— Atomic layer deposition, zinc oxide, thin-film transistor, low leakage current.**

I. Introduction

OXIDE semiconductor transistors have attracted wide attention due to their high mobility, low subthreshold slope (SS), low off-state leakage current (I_{OFF}), low growth temperature, and low cost for large-area fabrication. Oxide semiconductor transistors are regarded as one of the best candidates as driving component in display panel and recently considered to be promising as back-end-of-line (BEOL) compatible devices for monolithic 3D integration. In both applications, I_{OFF} is critical which influences refresh rate in display panel [1] and retention time in BEOL-compatible dynamic random-access memory (DRAM) [2], [3], [4].

The large bandgap and unique electronic structure of oxide semiconductors lead to a much lower I_{OFF} compared to conventional semiconductors such as Si and III-V [5]. I_{OFF} below 10^{-20} A/μm in crystalline indium−gallium−zinc oxide devices [6] and indium−zinc oxide transistors [7], fabricated by sputtering deposition, have been achieved, demonstrating the potential of oxide semiconductors for low off-state leakage application. However, although oxide semiconductors by sputtering deposition have shown excellent low I_{OFF}, it is not possible to form conformal film in high aspect ratio 3D structures by sputtering, such as a vertical channel access transistor of DRAM [4].

Atomic layer deposition (ALD) is a more preferred method to grow oxide semiconductors with advantages such as atomic thickness control, CMOS compatible process, and especially with the capability of conformal ultra-thin film deposition on 3D structures [8], [9], [10], [11]. High-performance ALD oxide semiconductor transistors with high mobility, high drive current and steep SS have been demonstrated [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], where ZnO by ALD is one of the most studied semiconducting oxides due to its precursor availability, high growth rate, and relatively high stability and decent mobility compared to other oxide semiconductors [12], [13], [15]. For example, ALD ZnO with high mobility >40 cm^2/V·s have been demonstrated [15]. However, I_{OFF} of ALD oxide semiconductor transistors has not been systematically investigated. Considering the film formation process of ALD is very different from sputtering deposition, such as the introduction of C impurities due to organic precursors, it is important to investigate the off-state performance of ALD oxide semiconductor devices.

In this work, ALD ZnO transistors with low I_{OFF} are demonstrated. The impact of ALD growth temperature and annealing on the electrical performance is systematically studied. It is found that low temperature deposition and post deposition annealing are effective to enhance the performance the ALD ZnO transistors. μ_{FE} as high as 32.8 cm^2/V·s and 26.3 cm^2/V·s are achieved before and after annealing. Devices with interdigitated electrodes are used with a channel width (W_{ch}) of 10000 μm in order to improve the detection limit, achieving a low I_{OFF} on the order of 10^{-18} A/μm even at a high temperature of 147 °C. These results suggest ALD ZnO is a promising channel material for low off-state leakage current device applications, such as access transistor of DRAM.

II. Experiments

Fig. 1(a) shows the schematic diagram of a back-gate ALD ZnO transistor in this work. Fig. 1(b) shows top-view photo images of ALD ZnO transistors with normal W_{ch} of 40 μm and wide W_{ch} of 10000 μm. Interdigitated electrodes are used to obtain large W_{ch} for low I_{OFF} measurement. The device fabrication process is summarized in Fig. 1(c). P+ Si substrate with 90 nm thermal grown SiO_2 was first cleaned by standard

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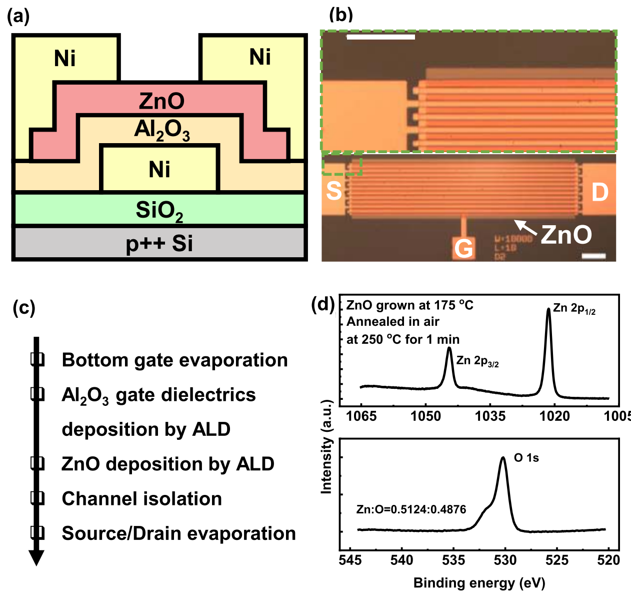

Fig. 1. (a) Schematic diagram and (b) Top-view photo image of back-gate transistors with ZnO channel. Interdigitated electrodes are used to achieve large channel width up to 10000 μm. The length of scale bars is 100 μm. (c) Process flow of ZnO back-gate transistors. (d) XPS spectra of ALD ZnO.

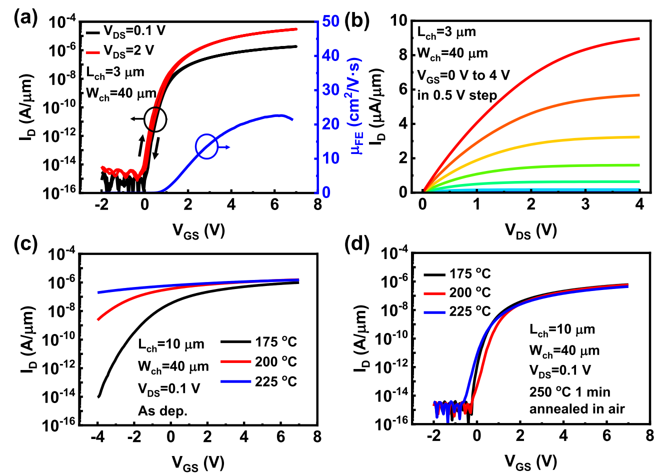

Fig. 2. (a) Transfer characteristics and extracted μ_{FE} at $V_{DS} = 0.1$ V of an ALD ZnO transistor. (b) Output characteristics of the same device as in (a). Transfer characteristics of ALD ZnO transistors with different ZnO growth temperatures (c) before and (d) after annealing.

solvent cleaning process before device fabrication. A bilayer photolithography (LOR10A+AZ5214) process was employed to form the back-gate pattern. Then 40 nm Ni was deposited by thermal evaporation and lift-off. 12 nm ALD Al_2O_3 grown by ALD at 200 °C is used as gate oxide. ZnO was grown by ALD at 175 °C, 200 °C, or 225 °C with diethylzinc (DEZn) and H_2O as precursors of Zn and O, respectively. The thickness of ZnO (T_{ch}) is 21 nm unless otherwise specified. The growth rate of ZnO is about 1.9 Å/cycle, which is insensitive to growth temperature. The channel region was patterned by single layer photolithography (AZ5214), followed by diluted hydrochloric acid wet etching for channel isolation. 40 nm Ni source/drain electrode was patterned by bilayer photolithography and lift-off, and was deposited by thermal evaporation. The devices were annealed in air at 200 °C, 250 °C or 300 °C for 30 seconds or 1 minute. Electrical characterization was done from room temperature to 147 °C in vacuum under 10^{-5} Torr. The formation of stoichiometric ZnO was confirmed by X-ray photoelectron spectroscopy (XPS, AXIS-ULTRADLD) as shown in Fig. 1(d).

III. Results and Discussion

Fig. 2(a) and 2(b) present typical transfer and output characteristics of a ZnO transistor with channel length (L_{ch}) of 3 μm, and with ALD growth temperature of 175 °C and annealing temperature of 250 °C. The device exhibits a high on/off ratio$>10^{10}$, μ_{FE} of 22.6 cm^2/V·s and a small hysteresis. Threshold voltage (V_{TH}) was extracted by linear-extrapolation method at V_{DS} of 0.1 V, achieving a positive V_{TH} of 2.7 V for enhancement-mode operation. Fig. 2(c) studies the impact of ALD growth temperature of ZnO on transfer characteristics, where V_{TH} shifted negatively at higher growth temperature, suggesting a higher carrier concentration, most likely due to higher oxygen vacancies, introduced during ALD process [12], [18]. The high carrier concentration can be suppressed by annealing after device fabrication, as shown in Fig. 2(d). Significant positive V_{TH} shift and on/off ratio increase are achieved by 250 °C annealing in air, indicating annealing in air is efficient to passivate the oxygen vacancies generated during ALD process [12], [19]. The ALD ZnO transistors with different ALD growth temperatures show similar properties after rapid annealing in air ambient, indicating a large process temperature window of ALD ZnO transistors, which benefits elemental doping for performance enhancement [20], [21].

The impact of ALD growth temperature on device performance is summarized in Fig. 3. Fig. 3(a) shows V_{TH} versus ZnO growth temperature before and after annealing. V_{TH} shifts from −4.7 V to 1.0 V while decreasing ZnO growth temperature from 225 °C to 175 °C, suggesting that oxygen vacancies are very sensitive to ZnO growth temperature. The reason is that oxygen vacancies are oxidized by oxygen in air, where oxygen vacancies behave like shallow donors [12]. V_{TH} increases to about 2.7-2.8 V after 250 °C annealing in air, meanwhile a much smaller standard deviation is achieved compared to as-deposited devices, suggesting annealing can contribute to the reduction of device variation. Fig. 3(b) compares the impact of ZnO growth temperature and annealing on μ_{FE}. μ_{FE} drops slightly after annealing, as expected because of the increase on contact resistance leads to the reduction of μ_{FE} instead of the intrinsic carrier mobility. Thus, the intrinsic mobility may not drop as much [22]. μ_{FE} as high as 32.8 cm^2/V·s and 26.3 cm^2/V·s is achieved before and after annealing.

Fig. 3(c) presents SS versus ZnO growth temperature after annealing. Although similar V_{TH} are achieved with different ZnO growth temperature after annealing, however, a much smaller SS is obtained at ALD growth temperature of 175 °C, suggesting high temperature ZnO growth not only introduce oxygen vacancies in bulk, but also results in interfacial defects generation, which cannot be effectively passivated by low temperature annealing in this work. Therefore, low temperature ALD growth of ZnO is preferred for high-performance device applications. Fig. 3(d) shows the V_{TH} scaling metrics with L_{ch} down to 3 μm of ALD ZnO transistor with ALD growth

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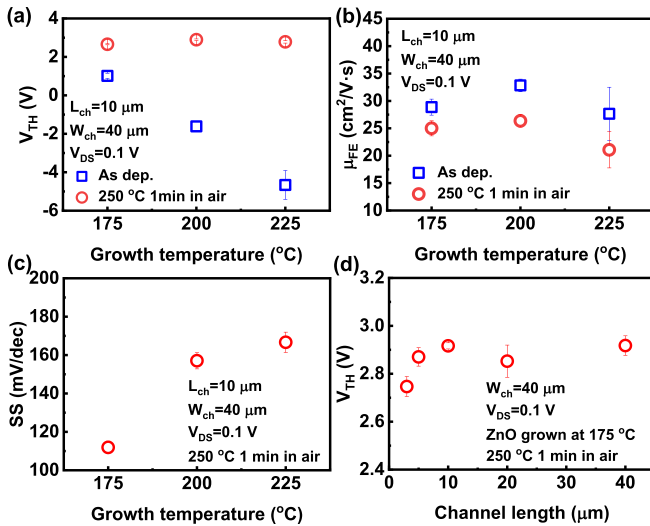

Fig. 3. (a)-(c) V_{TH}, μ_{FE} and SS of ALD ZnO transistor with different ZnO growth temperatures before and after annealing at 250 °C for 1 minute in air ambient. (d) V_{TH} scaling metrics of ALD ZnO transistors.

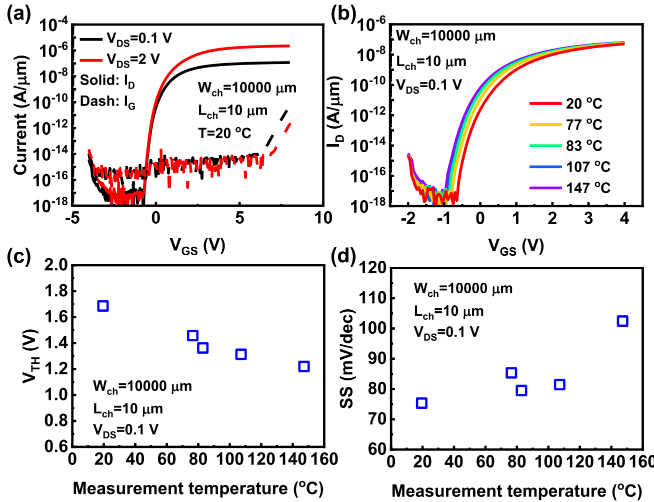

Fig. 4. (a) Transfer characteristics of an ALD ZnO transistor with W_{ch} of 10000 μm. (b) Temperature-dependent transfer characteristics. (c) V_{TH} and (d) SS characteristics at different measurement temperatures.

temperature of 175 °C and annealed at 250 °C for 1 minute in air. V_{TH} roll-off is not significant at this length scale.

A device with interdigitated electrodes is used with a wide W_{ch} of 10000 μm and L_{ch} of 10 μm (Fig. 1(b)) in order to measure I_{OFF} with higher resolution. The high-resolution source measurement unit (HRSMU) used in this work has a current detection limit of about 10^{-14} A, considering a W_{ch} of 10000 μm, the current detection limit of this work is about 10^{-18} A/μm. Fig. 4(a) shows the transfer characteristics of an ALD ZnO transistor with W_{ch} of 10000 μm, where I_{OFF} is about 3×10^{-18} A/μm, which is still at the detection limit of the measurement equipment. A high on/off ratio $\sim 10^{12}$ is achieved. This device has 15 nm thick Al_2O_3 as gate insulator and 17 nm thick ZnO as active layer and was annealed in air ambient at 200 °C for 30 seconds.

Fig. 4(b) presents the temperature-dependent transfer characteristics from room temperature to 147 °C. The device in Fig. 4(b) has 12 nm thick Al_2O_3 as gate insulator and 17 nm

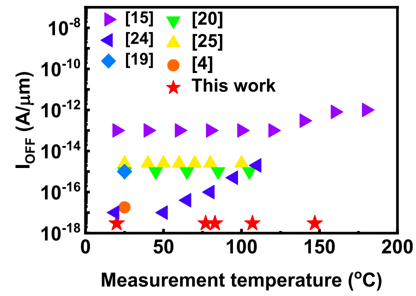

Fig. 5. Benchmark of I_{OFF} at different measurement temperatures of ALD ZnO transistors in this work with other reported ALD oxide semiconductor transistors.

thick ZnO as active layer and was annealed in air ambient at 300 °C for 1 minute. Here, annealing temperatures at the range from 200-300 °C have minor impact on device performance, and slightly different device parameters and annealing temperature have no impact on the conclusion. As can be seen, I_{OFF} is still below the detection limit even at 147 °C. As I_{OFF} is expected to be exponentially dependent on temperature, it can be speculated that the intrinsic I_{OFF} of the ALD ZnO transistor at room temperature is much lower than 10^{-18} A/μm. The ultra-low leakage is achieved due to large bandgap of ZnO and the unique energy distribution of defects [5].

Fig. 4(c) shows the temperature-dependent V_{TH}, extracted from Fig. 4(b). V_{TH} shifted negatively at higher temperature, which may be attributed to thermal activated carrier generation, as also reported in other works [13], [20], [23], [24]. Fig. 4(d) shows the temperature-dependent SS, also extracted from Fig. 4(b), achieving a minimum SS of 75.3 mV/dec (extracted at I_D of 10^{-16} A/μm). SS of this device is much smaller than devices with W_{ch} of 40 μm because a lower D_{it} inside the bandgap. A smaller I_D corresponds to a deeper fermi level inside band gap, thus a lower D_{it}. Therefore, the difference in detected SS is due to the difference in detect resolution of devices with W_{ch} of 10000 μm and devices with W_{ch} of 40 μm. The SS at lower I_D can be even smaller, if not limited by the current detection limit. Fig. 5 benchmarks the temperature-dependent I_{OFF} of ALD ZnO transistors in this work with other reported ALD oxide semiconductor transistors, where we have demonstrated lowest I_{OFF} and still under the detect limit even at 147 °C, among oxide semiconductor devices by ALD.

IV. Conclusion

In conclusion, ALD ZnO transistors with ultra-low I_{OFF}, steep SS and relatively high μ_{FE} are demonstrated. It is found that low temperature deposition and post deposition annealing are very effective to enhance the performance of the ALD ZnO transistors. Devices with interdigitated electrodes are used with a W_{ch} of 10000 μm, achieving a low I_{OFF} on the order of 10^{-18} A/μm and still under the detect limit even at 147 °C. The low I_{OFF} devices have potential in BEOL-compatible DRAM applications especially with the capability of integration with 3D structures.

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