

# On the Accurate Evaluation of Intrinsic Electron Mobility on Oxide Semiconductor Transistors

Chen Wang, Longzhong Liao, Kai Jiang, Ziheng Wang<sup>id</sup>, Jinxiu Zhao<sup>id</sup>, *Student Member, IEEE*, Guo Zhou, and Mengwei Si<sup>id</sup>, *Member, IEEE*

**Abstract**—In this work, the evaluation of intrinsic electron mobility ( $\mu$ ) in oxide semiconductor transistors is investigated by different methods. Indium oxide ( $\text{In}_2\text{O}_3$ ) transistors with maximum field-effective mobility ( $\mu_{FE\_max}$ ) of  $97.8 \text{ cm}^2/\text{Vs}$  were fabricated, where the impact of contact resistance on  $\mu_{FE}$  was excluded. The  $\mu_{FE}$ , effective mobility ( $\mu_{eff}$ ) and temperature-dependent Hall mobility ( $\mu_{Hall}$ ) of  $\text{In}_2\text{O}_3$  transistors are compared. It is found that the deviation of  $\mu_{FE}$  from  $\mu$  is caused by the dependence of  $\mu$  on gate voltages, because of the impact of percolation conduction and surface roughness scattering mechanisms.  $\mu_{eff}$  and  $\mu_{Hall}$  align with the global average definition of intrinsic  $\mu$ , while  $\mu_{FE}$  characterizes its differential response to gate modulation. Therefore,  $\mu_{eff}$  and  $\mu_{Hall}$  are more suitable to represent the intrinsic  $\mu$ . This work provides a theoretical guideline on the accurate evaluation and further improvement of the mobility of oxide semiconductor transistors.

**Index Terms**—Oxide semiconductors, mobility, scattering mechanism.

## I. INTRODUCTION

OXIDE semiconductor transistors have been widely adopted in display technologies and are considered as the promising candidate for monolithic 3D applications, benefiting from their low leakage current, high mobility, steep subthreshold swing and low thermal budget [1], [2]. Indium-rich oxide semiconductors by atomic layer deposition (ALD), such as indium oxide ( $\text{In}_2\text{O}_3$ ) [3], [4], indium tin oxide (ITO) [4], indium tungsten oxide (IWO) [5], indium zinc oxide (IZO) [6], indium gallium zinc oxide (IGZO) [7], [8], etc., have been reported achieving high mobility. However, in literature, field-effect mobility ( $\mu_{FE}$ ) is commonly used to represent the intrinsic mobility ( $\mu$ ), which is often overestimated. In many cases, this overestimation is a result of artifacts arising from non-ideal contacts, as reported in [9] and [10].

Received 1 August 2025; revised 22 August 2025; accepted 27 August 2025. Date of publication 2 September 2025; date of current version 24 October 2025. This work was supported in part by STI 2030-Major Projects under Grant 2022ZD0210600, in part by the National Natural Science Foundation of China under Grant 62274107 and Grant 92264204, and in part by Shanghai Pilot Program for Basic Research-Shanghai Jiao Tong University under Grant 21TQ1400212. The review of this letter was arranged by Editor S. Zhang. (Corresponding author: Mengwei Si.)

Chen Wang, Kai Jiang, Ziheng Wang, Jinxiu Zhao, and Mengwei Si are with the State Key Laboratory of Micro-Nano Engineering Science and the School of Information Science and Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: mengwei.si@sjtu.edu.cn).

Longzhong Liao and Guo Zhou are with the 13th Research Institute, CETC, Shijiazhuang 050051, China.

Digital Object Identifier 10.1109/LED.2025.3604471

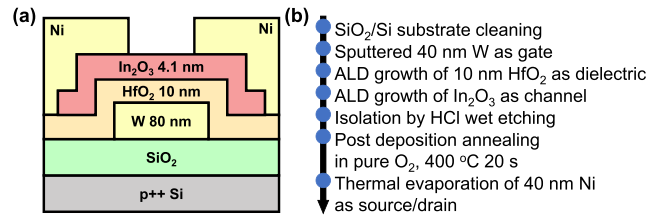


Fig. 1. (a) Schematic diagram of an  $\text{In}_2\text{O}_3$  transistor with 10 nm  $\text{HfO}_2$  as insulator and  $T_{ch}$  of 4.1 nm. (b) Fabrication process flow of the bottom-gate  $\text{In}_2\text{O}_3$  transistor.

For the high mobility oxide semiconductor transistors with good ohmic contact, the  $\mu_{FE}$  may still be overestimated. The  $\mu_{FE}$  is typically extracted from the transconductance ( $g_m$ ) of transfer curves, where  $\mu_{FE}$  first increases to its maximum value ( $\mu_{FE\_max}$ ) and then rapidly decreases with gate-to-source voltage ( $V_{GS}$ ), which is far less than the effective mobility ( $\mu_{eff}$ ). Therefore, the usage of  $\mu_{FE}$  to evaluate the  $\mu$  of oxide semiconductor transistors may not be reliable. However, the physical origin of the deviation has been ignored and has not been understood.

In this work,  $\text{In}_2\text{O}_3$  transistors with high  $\mu_{FE}$  are fabricated. Ohmic contacts are formed at source/drain (S/D) with post-deposition annealing process, so that the influence of S/D contacts on mobility evaluation can be excluded.  $\mu_{FE}$ ,  $\mu_{eff}$  and Hall mobility ( $\mu_{Hall}$ ) measurements are performed. It is found  $\mu_{FE}$  in oxide semiconductor transistors deviates from  $\mu$  because of the  $V_{GS}$ -dependence of  $\mu$ , leading to the overestimation at low  $V_{GS}$  and underestimation at high  $V_{GS}$ . Therefore,  $\mu_{eff}$  and  $\mu_{Hall}$  are more suitable to evaluate the intrinsic  $\mu$ . Moreover, the dependence of  $\mu$  on  $V_{GS}$  is found to likely originates from the percolation conduction and surface roughness scattering mechanisms.

## II. EXPERIMENTS

Fig. 1(a) shows the schematic diagram of a back-gate  $\text{In}_2\text{O}_3$  transistor in this work. The device fabrication process is summarized in Fig. 1(b). 80 nm W gate was deposited by magnetron sputtering. 10 nm  $\text{HfO}_2$  insulator was grown by ALD at 200 °C.  $\text{In}_2\text{O}_3$  channel was grown by ALD at 225 °C. Post-deposition annealing was carried out in  $\text{O}_2$  at 400 °C for 20 s. 40 nm Ni S/D electrodes were deposited by thermal evaporation. The thickness of  $\text{In}_2\text{O}_3$  ( $T_{ch}$ ) was determined by atomic force microscopy (AFM). Electrical characterization was done at room temperature in vacuum under  $\sim 5 \text{ Pa}$ . I-V and C-V were completed by Keysight B1500 and E4980, respectively. Hall bar devices were fabricated together with

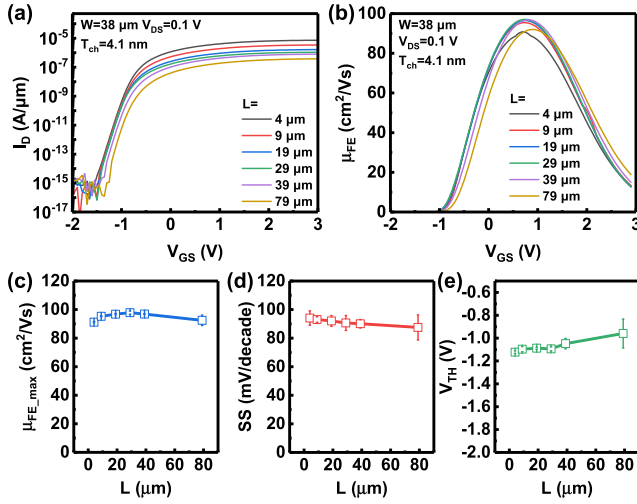


Fig. 2. (a) Transfer curves and (b) extracted  $\mu_{FE}$  at  $V_{DS}$  of 0.1 V of  $\text{In}_2\text{O}_3$  transistors with  $T_{ch}$  of 4.1 nm and different  $L$ . (c)-(e)  $L$ -dependent  $\mu_{FE\_max}$ , SS and  $V_{TH}$  of  $\text{In}_2\text{O}_3$  transistors. Each data point represents the average of 3 different devices.

transistors to evaluate  $\mu_{Hall}$  and sheet carrier density ( $n_{sheet}$ ) with channel length ( $L$ ) of 200  $\mu\text{m}$  and channel width ( $W$ ) of 60  $\mu\text{m}$ . The Hall measurement was carried out in a physical property measurement system (PPMS) (DynaCool-14T).

### III. RESULTS AND DISCUSSION

Fig. 2(a) presents the transfer curves of  $\text{In}_2\text{O}_3$  transistors with different  $L$ . The drain current ( $I_D$ ) in linear region ( $V_{DS} \ll V_{GS} - V_{TH}$ ) can be written as [11]

$$I_D = \frac{W}{L} \mu Q_n V_{DS} = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \quad (1)$$

where  $Q_n$  is the mobile carrier density,  $C_{ox}$  is the gate capacitance,  $V_{TH}$  is the threshold voltage, and  $V_{DS}$  is the drain-to-source voltage. The  $\mu_{FE}$  is defined using  $g_m$  [11]

$$\mu_{FE} = \frac{L}{WC_{ox}V_{DS}} \left( \frac{\partial I_D}{\partial V_{GS}} \right) = \frac{g_m L}{WC_{ox}V_{DS}} \quad (2)$$

However, the definition of  $\mu_{FE}$  deviates from the physical definition of  $\mu$ , which is  $\mu = \sigma/qn_e$ , where  $\sigma$  is the conductivity,  $q$  is the electron charge and  $n_e$  is the carrier density. The  $\mu$  calculated from  $\mu = \sigma/qn_e$  is consistent with the basic definition of intrinsic  $\mu$ , which describes the “average mobility” of carriers at conduction band. Eqn. (2) is only achieved by assuming  $\mu$  is constant, that is,  $\mu = \mu_{FE} = \partial\sigma/q\partial n_e$ .  $\mu_{FE}$  of devices in Fig. 2(a) is extracted as shown in Fig. 2(b).  $\mu_{FE}$  increases to  $\mu_{FE\_max}$  and then rapidly drops. Transistors with different  $L$  have similar  $\mu_{FE}$ , suggesting that good ohmic contacts are formed at S/D. Therefore, the peak in  $\mu_{FE}$ - $V_{GS}$  characteristics is unrelated with contact resistance. The extracted  $\mu_{FE\_max}$ , SS and  $V_{TH}$  scaling metrics are plotted in Fig. 2(c)-2(e). The devices exhibit a high on/off ratio  $> 10^{10}$ , a high  $\mu_{FE\_max}$  of 97.8  $\text{cm}^2/\text{Vs}$ , a SS of  $\sim 90$  mV/decade, and a  $V_{TH}$  of  $\sim -1$  V. The contact resistance ( $R_C$ ) is extracted by the transfer length method (TLM), which is much lower than total resistance ( $R_{tot}$ ) at  $V_{GS}$  from  $-2$  V to 3 V. It suggests that an excellent ohmic contact is formed and the  $R_C$  will not have an obviously impact on the

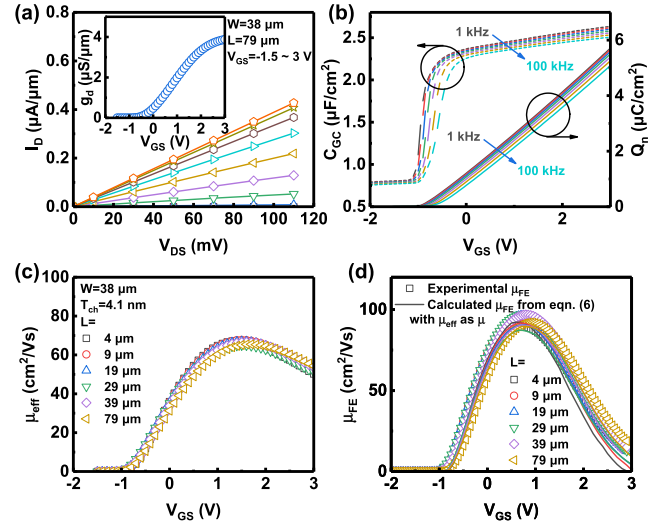


Fig. 3. (a) Output curves of an  $\text{In}_2\text{O}_3$  transistor with  $T_{ch}$  of 4.1 nm. The inset is the  $g_d$  versus  $V_{GS}$  characteristics. (b)  $C_{GC}$  and the corresponding  $Q_n$  versus  $V_{GS}$  characteristics. The frequency varies from 1 kHz to 100 kHz. (c)  $\mu_{eff}$  of  $\text{In}_2\text{O}_3$  transistors with different  $L$ . The  $C_{GC}$  is acquired at 1 kHz. (d) Comparison between experimental  $\mu_{FE}$  and that calculated from  $\mu_{eff}$ .

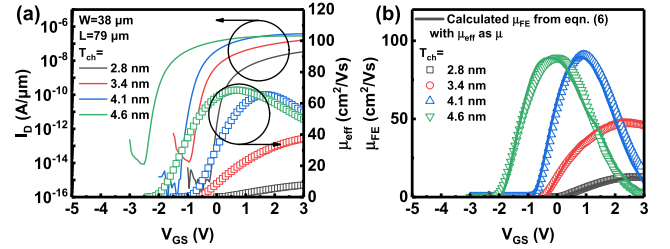


Fig. 4. (a) Transfer curves,  $\mu_{eff}$  and (c) experimental  $\mu_{FE}$  and that calculated from  $\mu_{eff}$  of  $\text{In}_2\text{O}_3$  transistors with different  $T_{ch}$ .

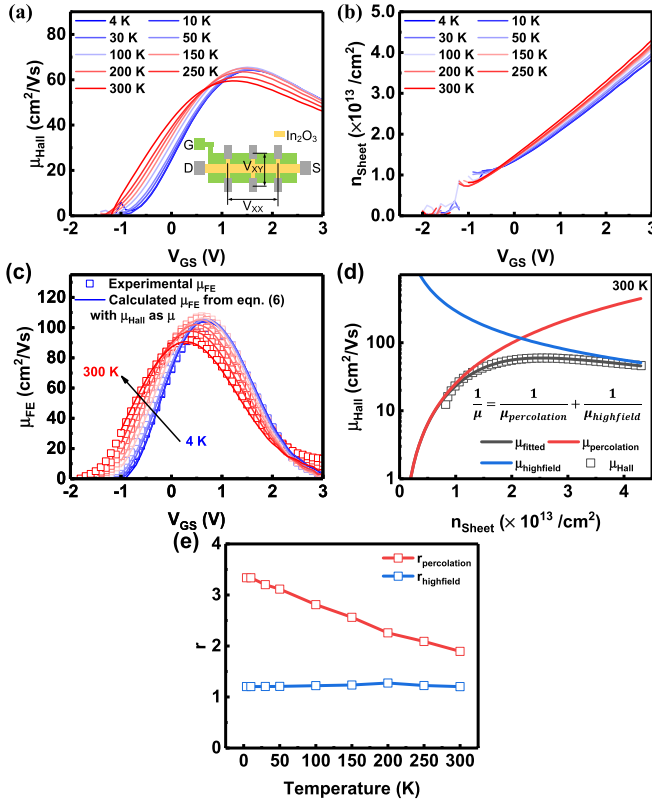
transfer characteristics. It is also confirmed that  $\mu_{FE}$  extracted in linear region does not change with  $V_{DS}$ , so the laterally field will not affect  $\mu_{FE}$  for  $\text{In}_2\text{O}_3$  transistors with  $L > 1\ \mu\text{m}$ .  $\mu_{eff}$  is typically defined by [11]

$$\mu_{eff} = \frac{L}{WQ_n} \frac{\partial I_D}{\partial V_{DS}} = \frac{Lg_d}{WQ_n} \quad (3)$$

where  $g_d$  is the drain conductance. The definition of  $\mu_{eff}$  conforms to the physical definition of intrinsic  $\mu$ . The  $Q_n$  is typically acquired from the integral of gate-to-channel capacitance ( $C_{GC}$ ) by C-V measurements, where  $Q_n$  can be written as [11]

$$Q_n = \int_{-\infty}^{V_{GS}} C_{GC} dV_{GS} \quad (4)$$

It is more reliable than to calculate  $Q_n$  using  $C_{ox}(V_{GS} - V_{TH})$ , because it avoids the uncertainty around  $V_{TH}$ . Fig. 3(a) shows the output curves of  $\text{In}_2\text{O}_3$  transistors with  $V_{GS}$  from  $-1.5$  V to 3 V and  $V_{DS}$  from 0 mV to 110 mV. The devices are in linear region due to the relatively small  $V_{DS}$ . The  $g_d$  extracted from output curves is plotted in the inset of Fig. 3(a). Fig. 3(b) shows the  $C_{GC}$  and the corresponding  $Q_n$  of  $\text{In}_2\text{O}_3$  transistors with S/D electrodes grounded. The frequency dispersion of  $C_{GC}$  is likely due to electron generation and recombination from the subgap defect states [12].  $C_{GC}$  measured at low frequency is adopted to extract the  $\mu_{eff}$ . Fig. 3(c) shows the



**Fig. 5.** (a)  $\mu_{Hall}$  and (b)  $n_{sheet}$  versus  $V_{GS}$  characteristics from 4 K to 300 K of an  $In_2O_3$  device with  $T_{ch}$  of 4.1 nm. (c) Comparison between the experimental  $\mu_{FE}$  in Hall bar and that calculated from  $\mu_{Hall}$  using eqn. (6) at 4 K ~ 300 K. (d) Numerical fitting of  $\mu_{Hall}$  versus  $n_{sheet}$  characteristics at 300 K by percolation and high field scattering mechanisms. (e) Temperature-dependent  $r_{percolation}$  and  $r_{highfield}$  from 4 K to 300 K.

$\mu_{eff}$  of  $In_2O_3$  transistors with different  $L$ . The maximum  $\mu_{eff}$  is  $\sim 65$  cm<sup>2</sup>/Vs, which is smaller than  $\mu_{FE\_max}$ . The decrease of  $\mu_{eff}$  under high  $V_{GS}$  is also smaller than that of  $\mu_{FE}$ . The reason for the difference between  $\mu_{FE}$  and  $\mu_{eff}$  is because the dependence of  $\mu$  on  $V_{GS}$  is ignored when calculating  $\mu_{FE}$  in eqn. (2), where

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{WC_{ox}V_{DS}}{L} \frac{\partial}{\partial V_{GS}} \left( \mu \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \right) \quad (5)$$

By combining eqn. (2) and (5), the  $\mu_{FE}$  can be written as

$$\mu_{FE} = \frac{\partial \mu}{\partial V_{GS}} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) + \mu \quad (6)$$

In general,  $\mu_{FE}$  is close to  $\mu$  because  $\partial \mu / \partial V_{GS}$  can be ignored, such as in the case of silicon. However, in oxide semiconductor transistors, the existence of  $\partial \mu / \partial V_{GS}$  will cause a large error when evaluating  $\mu$  by  $\mu_{FE}$ , which might be caused by percolation or other scattering mechanism.

According to the definition of  $\mu_{eff}$  in eqn. (3), there is no derivative to  $V_{GS}$ , so it is closer to  $\mu$ . If  $\mu_{eff}$  is used as  $\mu$  in eqn. (6), the corresponding  $\mu_{FE}$  can be calculated. Fig. 3(d) compares the experimental  $\mu_{FE}$  and that calculated from eqn. (6) with  $\mu_{eff}$  as  $\mu$  in transistors with different  $L$ . The experimental  $\mu_{FE}$  and that calculated with  $\mu_{eff}$  as  $\mu$  match well for all devices, which further confirms that the overestimation of  $\mu_{FE\_max}$  is caused by the dependence of  $\mu$  on  $V_{GS}$ . The transfer curves,  $\mu_{eff}$ , experimental  $\mu_{FE}$  and

that calculated from  $\mu_{eff}$  of  $In_2O_3$  transistor with different  $T_{ch}$  are plotted in Figs. 4(a) and (b), respectively. For  $In_2O_3$  transistors with different  $T_{ch}$ , the experimental  $\mu_{FE}$  and that calculated from  $\mu_{eff}$  match well, which further confirms that  $\mu_{eff}$  represents the intrinsic  $\mu$  more accurately.

Hall effect measurement is a widely adopted approach to measure the  $\mu_{Hall}$  and  $n_{sheet}$ . Figs. 5(a) and (b) present the  $\mu_{Hall}$  and  $n_{sheet}$  at temperatures from 4 K to 300 K.  $\mu_{Hall}$  exhibits the similar relation with  $V_{GS}$  as  $\mu_{eff}$ .  $\mu_{FE}$  is also extracted from the Hall bar, where the impact of  $R_C$  can be avoided using a 4-point approach, so that it is more accurate than that in a transistor. Fig. 5(c) gives the experimental  $\mu_{FE}$  and that calculated according to eqn. (6) with  $\mu_{Hall}$  as  $\mu$  at 4 K ~ 300 K, which match better than that calculated with  $\mu_{eff}$  as  $\mu$ . The  $\mu_{FE\_max}$  corresponds to peak  $d\sigma/dn$  values during new conductive channel formation, confirming its origin as a fundamental physical feature of carrier transport in oxide semiconductor. It also confirms that  $\mu_{Hall}$  can better represents the  $\mu$  of  $In_2O_3$  transistors than  $\mu_{eff}$ , because Hall measurements directly measure the  $n_{sheet}$  so that it can avoid the error caused by frequency dispersion in C-V.

To further investigate the dependence of  $\mu$  on  $V_{GS}$ , Fig. 5(d) depicts  $\mu_{Hall}$  versus  $n_{sheet}$  characteristics of  $In_2O_3$  transistors at 300 K. Note that  $n_{sheet}$  increases linearly with  $V_{GS}$ , suggesting the fast decrease of  $\mu_{FE}$  at high  $V_{GS}$  is not because of the overestimation of free carrier density by  $C_{OX}$ , also indicating a low trap density at high  $V_{GS}$ . At low carrier density ( $n_{sheet} < 2 \times 10^{13}$  /cm<sup>2</sup>),  $\mu_{Hall}$  increases with  $n_{sheet}$ , which is likely caused by percolation mechanism [13] and trap-limited conduction [14]. At high carrier density  $n_{sheet} > 2 \times 10^{13}$  /cm<sup>2</sup>,  $\mu_{Hall}$  decreases with  $n_{sheet}$  because of the high field scattering due to surface roughness or phonon, as described by  $\mu_{highfield} = \mu_{h0} (n_{sheet}/n_{h0})^{-r_{highfield}}$ , where  $\mu_{h0}$ ,  $n_{h0}$  and  $r_{highfield}$  are fitting parameters. In Fig. 5(d),  $\mu_{Hall}$  versus  $n_{sheet}$  characteristics at 300 K is fitted by percolation conduction and high field scattering according to Matthiessen's rule, i.e.,  $\mu_{Hall}^{-1} = \mu_{percolation}^{-1} + \mu_{highfield}^{-1}$ . The mobility limited by percolation is  $\mu_{percolation} = \mu_{p0} (n_{sheet}/n_{p0})^{-r_{percolation}}$ , where  $\mu_{p0}$ ,  $n_{p0}$ , and  $r_{percolation}$  are fitting parameters [13]. It is found that the percolation conduction and high field scattering can match well with the experimental results. The  $\mu_{Hall}$  versus  $n_{sheet}$  characteristics from 4 K to 300 K are also fitted (data not shown), and the corresponding  $r_{percolation}$  and  $r_{highfield}$  are plotted in Fig. 5(e).  $r_{percolation}$  decreases at high temperature, consistent with the thermal activation characteristics of the percolation conduction [13], [15]. For high field scattering, when  $r_{highfield}$  is equal to 0.3, it corresponds to phonon scattering, while when  $r$  is 2, it corresponds to surface roughness scattering [16]. The fitted  $r_{highfield}$  of  $\sim 1.2$  hardly changes with temperature. Therefore, surface roughness scattering is likely to be the dominant high field scattering mechanism.

#### IV. CONCLUSION

In conclusion, the overestimation of  $\mu$  by  $\mu_{FE\_max}$  in oxide semiconductor is well explained by the dependence of  $\mu$  on  $V_{GS}$ , due to the percolation conduction and surface roughness scattering related mechanisms. It is proposed that  $\mu_{eff}$  and  $\mu_{Hall}$  can better represent  $\mu$  compared with  $\mu_{FE}$ . The reported  $\mu_{FE}$  and its engineering methods in literature may need to be revisited.

## REFERENCES

- [1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: [10.1038/nature03090](https://doi.org/10.1038/nature03090).
- [2] X. Duan, K. Huang, J. Feng, J. Niu, H. Qin, S. Yin, G. Jiao, D. Leonelli, X. Zhao, Z. Wang, W. Jing, Z. Wang, Y. Wu, J. Xu, Q. Chen, X. Chuai, C. Lu, W. Wang, G. Yang, D. Geng, L. Li, and M. Liu, "Novel vertical channel-all-around (CAA) In-Ga-Zn-O FET for 2T0C-DRAM with high density beyond  $4F^2$  by monolithic stacking," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2196–2202, Apr. 2022, doi: [10.1109/TED.2022.3154693](https://doi.org/10.1109/TED.2022.3154693).
- [3] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," *Nature Electron.*, vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: [10.1038/s41928-022-00718-w](https://doi.org/10.1038/s41928-022-00718-w).
- [4] K. Han, Y. Kang, X. Chen, Y. Chen, and X. Gong, "Indium-tin-oxide thin-film transistors with high field-effect mobility ( $129.5 \text{ cm}^2/\text{Vs}$ ) and low thermal budget ( $150^\circ\text{C}$ )," *IEEE Electron Device Lett.*, vol. 44, no. 12, pp. 1999–2002, Dec. 2023, doi: [10.1109/LED.2023.3329481](https://doi.org/10.1109/LED.2023.3329481).
- [5] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, "BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with  $I_{\text{on}} = 370 \mu\text{A}/\mu\text{m}$ ,  $\text{SS} = 73 \text{ mV}/\text{dec}$  and  $I_{\text{on}}/I_{\text{off}}$  ratio  $> 4 \times 10^9$ ," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, Paper TH2.1, doi: [10.1109/VLSITECHNOLOGY18217.2020.9265064](https://doi.org/10.1109/VLSITECHNOLOGY18217.2020.9265064).
- [6] H.-M. Kim, S.-H. Ryu, S. Kim, K.-H. Lee, and J.-S. Park, "C-axis aligned composite InZnO via thermal atomic layer deposition for 3D nanostructured semiconductor," *ACS Appl. Mater. Interfaces*, vol. 16, no. 12, pp. 14995–15003, Mar. 2024, doi: [10.1021/acsami.3c16879](https://doi.org/10.1021/acsami.3c16879).
- [7] J. Sheng, T. Hong, H.-M. Lee, K. Kim, M. Sasase, J. Kim, H. Hosono, and J.-S. Park, "Amorphous IGZO TFT with high mobility of  $70 \text{ cm}^2/(\text{Vs})$  via vertical dimension control using PEALD," *ACS Appl. Mater. Interfaces*, vol. 11, no. 43, pp. 40300–40309, Oct. 2019, doi: [10.1021/acsami.9b14310](https://doi.org/10.1021/acsami.9b14310).
- [8] S. Samanta, U. Chand, S. Xu, K. Han, Y. Wu, C. Wang, A. Kumar, H. Velluri, Y. Li, X. Fong, A. V.-Y. Thean, and X. Gong, "Low subthreshold swing and high mobility amorphous indium-gallium-zinc-oxide thin-film transistor with thin  $\text{HfO}_2$  gate dielectric and excellent uniformity," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 856–859, Jun. 2020, doi: [10.1109/LED.2020.2985787](https://doi.org/10.1109/LED.2020.2985787).
- [9] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, "An experimental study of contact effects in organic thin film transistors," *J. Appl. Phys.*, vol. 100, no. 2, Jul. 2006, Art. no. 024509, doi: [10.1063/1.2215132](https://doi.org/10.1063/1.2215132).
- [10] C. Wang, C. Zeng, W. Lu, H. Ning, F. Li, and F. Ma, "High performance Schottky barrier TFTs with indium-gallium-zinc-oxide/Mo Schottky junction," *IEEE Electron Device Lett.*, vol. 44, no. 4, pp. 646–649, Apr. 2023, doi: [10.1109/LED.2023.3244583](https://doi.org/10.1109/LED.2023.3244583).
- [11] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006, doi: [10.1002/0471749095](https://doi.org/10.1002/0471749095).
- [12] Z. Wang, Z. Lin, M. Si, and P. D. Ye, "Characterization of interface and bulk traps in ultrathin atomic layer-deposited oxide semiconductor MOS capacitors with  $\text{HfO}_2/\text{In}_2\text{O}_3$  gate stack by C-V and conductance method," *Frontiers Mater.*, vol. 9, May 2022, Art. no. 850451, doi: [10.3389/fmats.2022.850451](https://doi.org/10.3389/fmats.2022.850451).
- [13] K. Abe, A. Sato, K. Takahashi, H. Kumomi, T. Kamiya, and H. Hosono, "Mobility- and temperature-dependent device model for amorphous In-Ga-Zn-O thin-film transistors," *Thin Solid Films*, vol. 559, pp. 40–43, May 2014, doi: [10.1016/j.tsf.2013.11.066](https://doi.org/10.1016/j.tsf.2013.11.066).
- [14] M. J. Kim, H. J. Park, S. Yoo, M. H. Cho, and J. K. Jeong, "Effect of channel thickness on performance of ultra-thin body IGZO field-effect transistors," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2409–2416, May 2022, doi: [10.1109/TED.2022.3156961](https://doi.org/10.1109/TED.2022.3156961).
- [15] K. Abe, K. Takahashi, A. Sato, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Operation model with carrier-density dependent mobility for amorphous In-Ga-Zn-O thin-film transistors," *Thin Solid Films*, vol. 520, no. 10, pp. 3791–3795, Mar. 2012, doi: [10.1016/j.tsf.2011.10.060](https://doi.org/10.1016/j.tsf.2011.10.060).
- [16] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994, doi: [10.1109/16.337449](https://doi.org/10.1109/16.337449).