Reliability of Atomic-Layer-Deposited Gate-All-Around In_2O_3 Nano-Ribbon Transistors with Ultra-High Drain Currents

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Abstract— In this work, we systematically investigate the reliability of atomic-layer-deposited (ALD) gate-all-around (GAA) single-channel In_2O_3 nano-ribbon field-effect transistors (FETs) with 5 nm HfO_2 gate dielectric and a maximum on-state current (I_{ON}) approaching 20 mA/μm at drain voltage (V_{DS}) of 1.7 V. A channel length (L_{ch}) and channel width (W_{ch}) independent positive threshold voltage (V_T) shift under negative gate bias stress (NBS) and a negative V_T shift under positive gate bias stress (PBS) are observed universally in all GAA In_2O_3 FETs, which is opposite to bias instability of the conventional Si CMOS and IGZO thin film transistors (TFTs). This unusual behavior can be simply explained by the concept of the trap neutral level (TNL) which is deeply aligned inside the In_2O_3 conduction band and the generation of donor- and acceptor-like traps in different gate bias stress conditions. In addition, other reliability issues including stress and recovery, gate bias dependence and temperature dependence are also studied. This comprehensive reliability analysis establishes ALD In_2O_3 as a competitive channel material of the back-end-of-line (BEOL) compatible FETs for 3D monolithic integration into next generation ICs.

I. Introduction

As the front-end-of-line semiconductor technology advances to 3 nm node and beyond, more attentions have been attracted towards the BEOL technology for monolithic 3D integration. Amorphous oxide semiconductors, a mature and widely used technology for display applications [1], have been considered as possible candidates for BEOL transistor channels. Recently, the ALD In_2O_3 FETs has achieved outstanding performance with controllable channel thickness (T_{IO}) down to 0.7 nm, mobility over 100 $cm^2/V\cdot s$ and on/off ratio up to 10^{17} [2-4]. Compared to the sputtering technique, ALD offers accurate film thickness control in large wafer scale as well as high uniformity and conformability on 3D structures. The relatively low process temperature makes ALD In_2O_3 well-suited for BEOL integration. Indeed, the only remaining challenge is to demonstrate that the transistors are sufficiently stable/reliable for practical applications.

In this work, high performance ALD GAA In_2O_3 FETs with maximum I_{ON} near 20 mA/μm at V_{DS} of 1.7 V are demonstrated using short-pulse electrical measurement to alleviate self-heating effects (SHE) [5,6]. The reliability is thoroughly characterized for the first time on this kind of novel devices with ultrahigh drain currents. A positive V_T shift under NBS and a negative V_T shift under PBS are found in all GAA In_2O_3 FETs, being independent on L_{ch}, W_{ch} and other geometric factors. Although the V_T shift trends are different from the conventional devices, this anomalous phenomenon can be explained comprehensively by the unusual band-alignment of metal and dielectric on In_2O_3. The charge neutrality level (CNL) at metal/In_2O_3 interface and the TNL at HfO_2/In_2O_3 interface are deeply aligned inside the In_2O_3 conduction band [7,8]. This specific band-alignment makes the metal contact resistivity on In_2O_3 extremely small and scaling benefit for ultra-short channels down to sub-10 nm possible [4,9]. The counter-intuitive V_T shifts after electrical stresses is easily explained by the newly generated donor- and acceptor-like interface traps.

II. Experiments

The 3D device schematic of a GAA single-channel In_2O_3 FET is presented in Fig. 1. 40 nm Ni was deposited by e-beam evaporation onto the substrate as the bottom gate. 5 nm HfO_2 and 3.1 nm In_2O_3 were grown by ALD at 200 °C and 225 °C in sequence. The film thickness is accurately controlled by ALD cycles. Channel was isolated by dry etching with deposition of Ni as source/drain contacts. Another 5 nm HfO_2 was grown to wrap the In_2O_3 channel as the dielectric with subsequent 5 min O_2 annealing at 250 °C. The final surrounding gate was formed by deposition of 40 nm Ni with dry etching first to connect with the bottom gate. Note the whole process is BEOL compatible with low thermal budget of 250 °C. Fig. 2 shows the energy dispersive x-ray spectroscopy (EDS) cross section view of a fabricated GAA In_2O_3 FET with L_{ch} of 40 nm.

The electrical characterization was carried out with the Keysight B1500 system in a Cascade probe station. A B1530A waveform generator fast measurement unit (WGFMU) was used in pulsed I-V measurement. For the reliability tests, GAA In_2O_3 FETs were under different gate bias ranging from -3 to 3 V with source and drain grounded, stress time up to 10^4 s and temperature from 20-100 °C. All threshold voltages are extracted by linear extrapolation method based on the transfer characteristics at V_{DS} of 0.1 V. More than 40 devices were measured with typical characteristics shown in this work.

III. Results and Discussion

The typical transfer and output characteristics of a long channel GAA In_2O_3 FET with L_{ch} of 1 μm and W_{ch} of 30 nm are shown in Figs. 3 and 4, with drain current saturation at a large V_{DS}. Figs. 5 and 6 present the transfer and output characteristics of a short channel GAA In_2O_3 FET with L_{ch} of 30 nm. The open circle indicates the data measured by normal DC setup and the solid circle refers to the data obtained from pulsed I-V method, with a data averaging time of 500 ns, V_{GS} and V_{DS} pulse width of 1 μs and pulse period of 100 ms to eliminate severe SHE in high V_{GS} and V_{DS} region. A maximum I_{ON} near 20 mA/μm, simply normalized by W_{ch}, is achieved. It is about one order of magnitude higher than any conventional semiconductor devices [5]. This ultrahigh I_{ON} is attributed to

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the high carrier density and high band velocity of ALD In_2O_3 [9]. An on/off ratio over 10^6 is also achieved. In addition, all devices with different L_{ch} and W_{ch} have the same V_T around -2.6 V due to the ultrathin In_2O_3 channel and GAA structure with strong immunity to the short channel effects.

Figs. 7-8 compare the time evolution of ΔV_T of three GAA In_2O_3 FETs with different L_{ch} and W_{ch} under NBS of -3 V and PBS of 3 V for 2×10^3 s, respectively. We note that here the NBS and PBS are defined relative to V_{GS}=0 instead of conventional definition for inversion-mode devices where V_T is considered as the reference point. This is because In_2O_3 FETs are depletion-mode devices and surface potential should be around zero when S/D is grounded and low biased. V_G cannot be biased reliably beyond -4 V either because 5 nm HfO_2 breaks down. The time evolution of ΔV_T curves are almost the same for all devices with different sizes in both NBS and PBS conditions, indicating bias instability independent of geometry. Figs. 9-10 show the time evolution of transfer characteristics of GAA In_2O_3 FETs under NBS of -3 V and PBS of 2 V for 10^4 s separately. Surprisingly, the transfer curve shifts positively with time under NBS whereas it shifts negatively with time under PBS. Such phenomenon is opposite to the bias instability in other amorphous oxide semiconductors TFTs such as IGZO, where the transfer curve usually shifts positively under PBS and negatively under NBS [10-17]. It is widely known in IGZO that the electrons are trapped in the gate dielectric and/or at the channel/dielectric interface under PBS, leading to a lower effective gate voltage and a positive V_T shift, and de-trapped under NBS. However, for this observed anomalous V_T shift behavior in GAA In_2O_3 FETs, we propose a different model based on the special alignment of the TNL in In_2O_3 (Fig. 11) and use donor-like and acceptor-like trap generation to explain the experiments [18-20]. As shown in the band diagram, TNL is aligned deeply in the conduction band with E_F located closely to it as a depletion-mode In_2O_3 FETs. During PBS condition, E_F will move above the TNL further and generate more donor-like interface traps after electrical stress, resulting in an increase of a positive V_T shift. Conversely, E_F will be moved far below the TNL under NBS and generate more acceptor-like interface traps, causing a negative V_T shift. The extracted time evolution of ΔV_T under NBS of -3 V and PBS of 2 V from Figs. 9-10 is plotted in Figs. 12-13. An empirical exponential function for the donor- and acceptor-like trap generation is used in the fitting:

$$\Delta V_T(t) = C_{dt/at}\left(1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right),$$

where $C_{dt/at}$ and τ are voltage and temperature dependent coefficients of donor- or acceptor-like trap formation, while β is the voltage and temperature independent power exponent [20]. The black dash lines exhibit a highly consistence with the experimental results ($\beta\sim0.37$ for NBS and 0.38 for PBS), verifying the anomalous V_T shift behavior due to donor- and acceptor-like trap generation and it is *not* really anomalous. Fig. 14 shows the time evolution of subthreshold slope (SS) shift under NBS and PBS. The SS maintains approximately the same value during 10^4 s stress, except for a slight change at the initial stage that could be ascribed to electrons trapping in preexisting states. Fig. 15 shows the time evolution of off-state current (I_{OFF}) and gate leakage current (I_G) under NBS of -3 V extracted from Fig. 9. The decreasing I_{OFF} is caused by electrons trapping in acceptor-like traps generated during NBS and the constant I_G indicates a highly robust HfO_2 dielectric without any degradation during 10^4 s stress. Stress and recovery tests were also performed on GAA In_2O_3 FETs with NBS of -3 V and PBS of 3 V for 10^3 s during the stress phase and subsequent gate bias of 0 V for 10^3 s during the recovery phase as shown in Figs. 16-17. It can be seen the positive V_T shift under NBS and negative V_T shift under PBS exist in every stress phase followed by normal recovery stage. To illustrate the self-affine periodicity in V_T shift, all five stress and recovery cycles in NBS and PBS conditions are shifted to the origin and plotted in Figs. 18-19. Obviously, a nearly perfect overlapping between different cycles can be achieved by a further ΔV_T scaling factor, confirming the universal V_T shift mechanism in GAA In_2O_3 FETs. Figs. 20-21 compare the time evolution of ΔV_T of GAA In_2O_3 FETs under different NBS and PBS. Positive V_T shifts are observed in all NBS conditions and negative V_T shifts are found in all PBS conditions with larger V_T shift under larger gate bias stress voltage, indicating E_F in as-fabricated devices located very closely to the TNL. Figs. 22-23 present the time evolution of ΔV_T under NBS and PBS at different temperatures. V_T shifts larger at higher temperatures because of a faster generation of donor- and acceptor-like traps. Fig. 24 shows a benchmark of reliability and field-effect mobility (μ_{FE}) of GAA In_2O_3 FETs with other amorphous oxide TFTs [10-17]. The stability is estimated from the V_T shift after a gate bias stress of 5000 s. In general, ALD GAA In_2O_3 FETs with 5 nm HfO_2 gate dielectric demonstrate a decent stability, much higher mobility and on-state performance.

IV. Conclusion

In conclusion, ALD GAA In_2O_3 FETs with remarkable device performance are demonstrated and the bias instability is systematically investigated. The unusual positive V_T shift under NBS and positive V_T shift under PBS can be understood by the model of generated donor- and acceptor-like traps with TNL located deeply in the conduction band. This comprehensive reliability study provides the foundation for ALD In_2O_3 being considered as a promising BEOL oxide semiconductor channel material for monolithic 3D integration. The work is supported by SRC nCore IMPACT Center, AFOSR and DARPA/SRC JUMP ASCENT Center.

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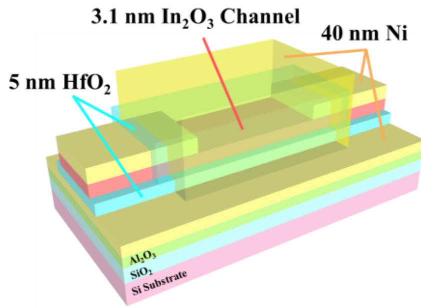

Fig. 1. 3D device schematic of a GAA In_2O_3 FET with T_{IO} of 3.1 nm and dielectric of 5 nm HfO_2.

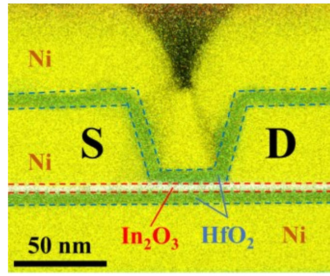

Fig. 2. TEM cross-section image of a GAA In_2O_3 FET with L_{ch} of 40 nm.

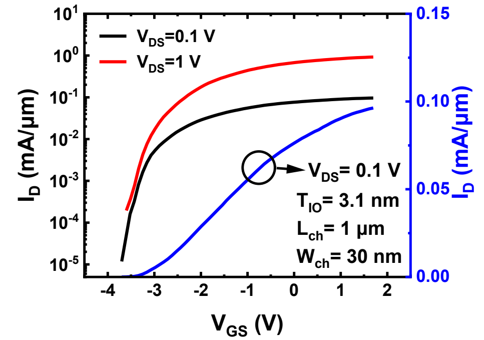

Fig. 3. Transfer characteristics of a typical GAA In_2O_3 nanoribbon FET with L_{ch} of 1 μm and W_{ch} of 30 nm.

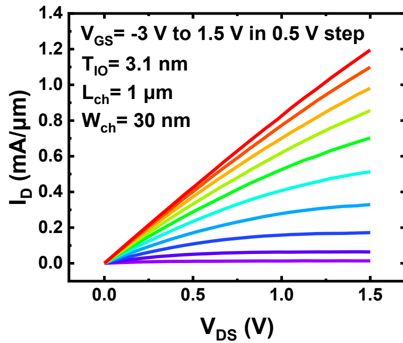

Fig. 4. Output characteristics of a GAA In_2O_3 nanoribbon FET with L_{ch} of 1 μm, showing saturation at large V_{DS}.

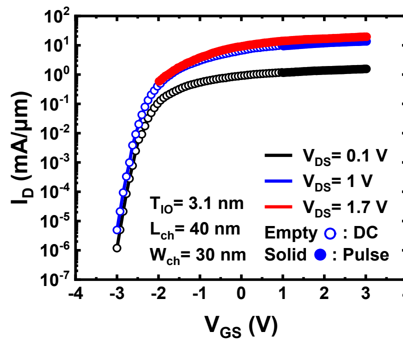

Fig. 5. Transfer characteristics of a GAA In_2O_3 nanoribbon FET with L_{ch} of 40 nm and W_{ch} of 30 nm measured in both DC and short-pulses.

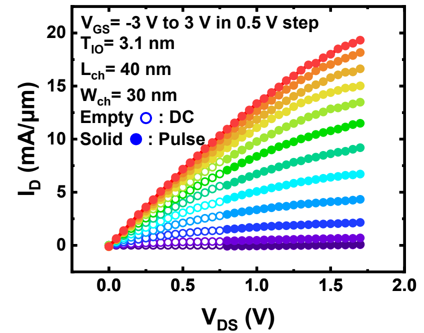

Fig. 6. Output characteristics of a GAA In_2O_3 nanoribbon FET with L_{ch} of 40 nm and maximum I_{ON} near 20 mA/μm.

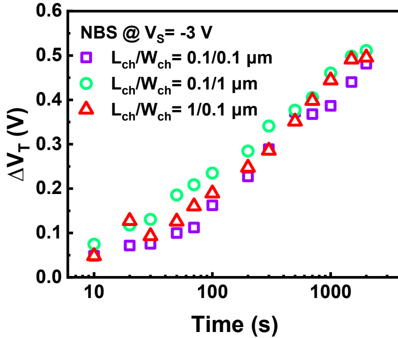

Fig. 7. Time evolution of ΔV_T of GAA In_2O_3 FETs with different channel dimensions under NBS of -3 V.

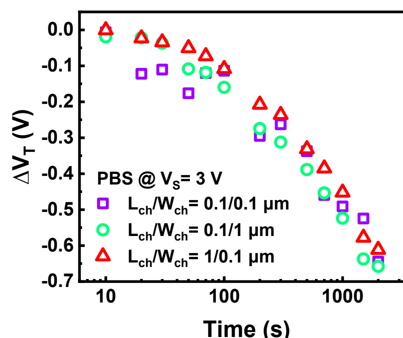

Fig. 8. Time evolution of ΔV_T of GAA In_2O_3 FETs with different channel dimensions under PBS of 3 V.

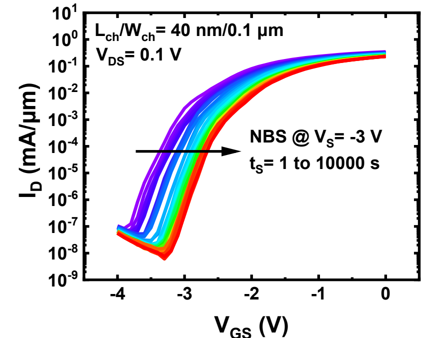

Fig. 9. Evolution of transfer characteristics of a GAA In_2O_3 FET under NBS of -3 V from 1 s to 10^4 s. V_T is shifted to positive.

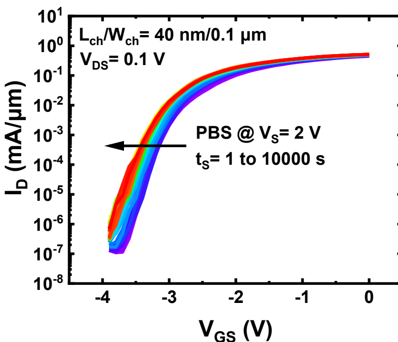

Fig. 10. Evolution of transfer characteristics of a GAA In_2O_3 FET under PBS of 2 V from 1s to 10^4 s. V_T is shifted to negative.

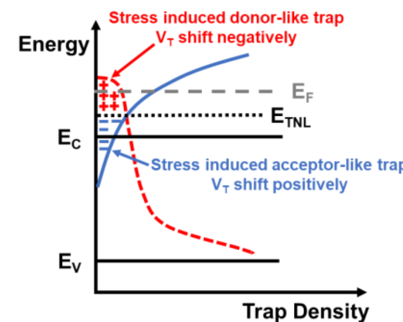

Fig. 11. Model of V_T shifts under NBS/PBS on GAA In_2O_3 FETs. E_{TNL} is located deeply inside the conduction band.

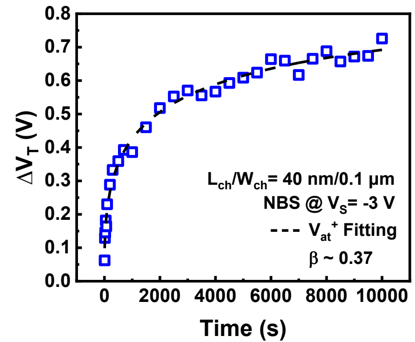

Fig. 12. Time evolution of ΔV_T of a GAA In_2O_3 FET under NBS of -3 V, fitted by acceptor-like trap generation model.

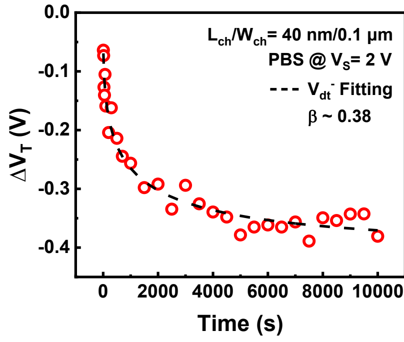

Fig. 13. Time evolution of ΔV_T of a GAA In_2O_3 FET under PBS of 2 V, fitted by donor-like trap generation model.

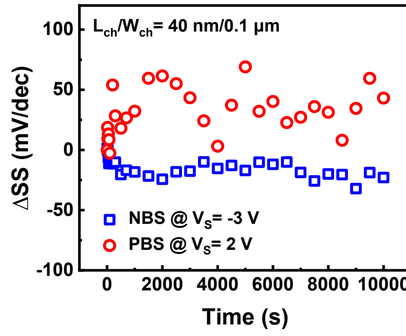

Fig. 14. Time evolution of ΔSS of GAA In_2O_3 FETs under NBS/PBS of -3/2 V for 10^4 s.

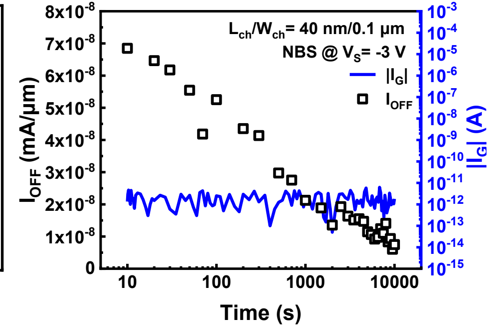

Fig. 15. Time evolution of I_{off} and $|I_G|$ of a GAA In_2O_3 FET under NBS of -3 V for 10^4 s.

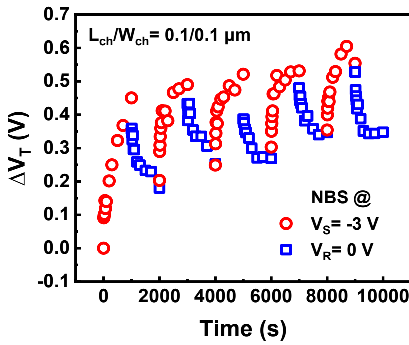

Fig. 16. Time evolution of ΔV_T of a GAA In_2O_3 FET under NBS of -3 V and recovery cycles of 0 V for 10^4 s.

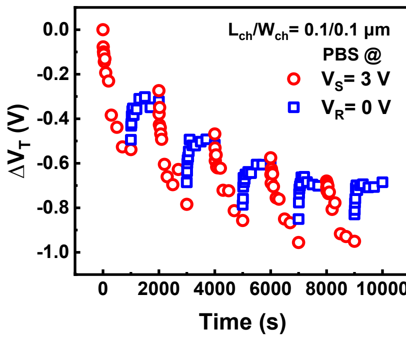

Fig. 17. Time evolution of ΔV_T of a GAA In_2O_3 FET under PBS of -2 V and recovery cycles of 0 V for 10^4 s.

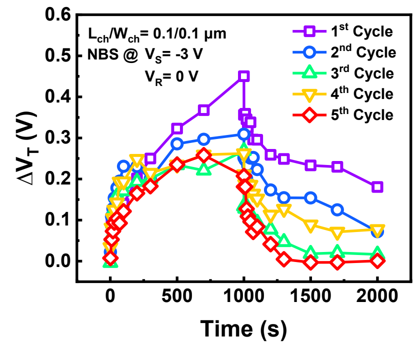

Fig. 18. Time evolution of ΔV_T of a GAA In_2O_3 FET in different NBS and recovery cycles, showing a universal behavior.

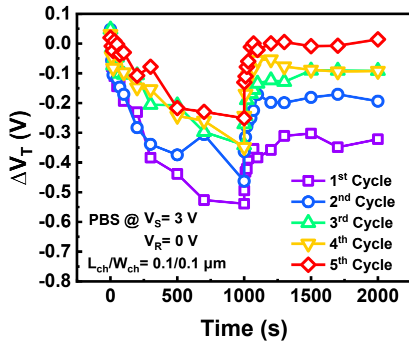

Fig. 19. Time evolution of ΔV_T of a GAA In_2O_3 FET in different PBS and recovery cycles, showing a universal behavior.

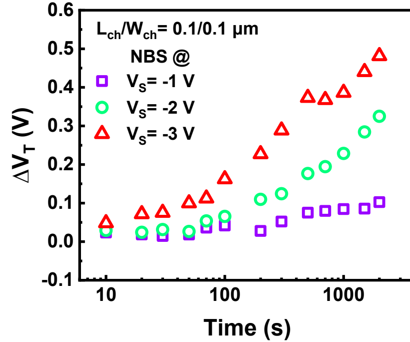

Fig. 20. Time evolution of ΔV_T of GAA In_2O_3 FETs under different NBS. Zero is chosen as the reference voltage due to a D-mode device.

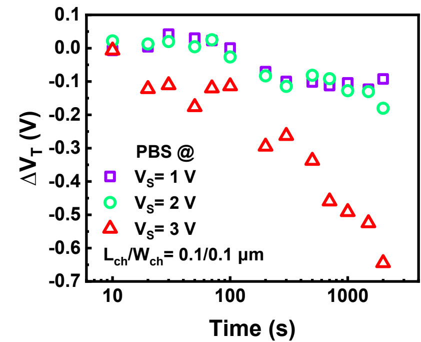

Fig. 21. Time evolution of ΔV_T of GAA In_2O_3 FETs under different PBS.

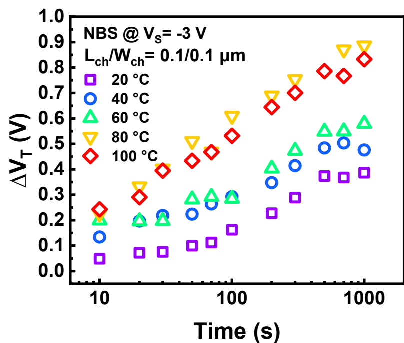

Fig. 22. Time evolution of ΔV_T of GAA In_2O_3 FETs under NBS of -3 V at different temperatures.

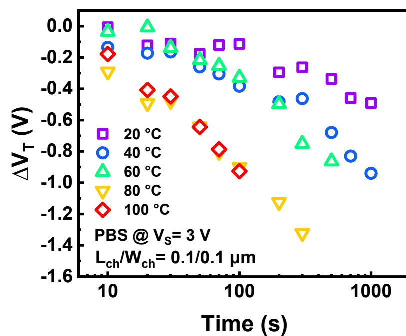

Fig. 23. Time evolution of ΔV_T of GAA In_2O_3 FETs under PBS of 3 V at different temperatures.

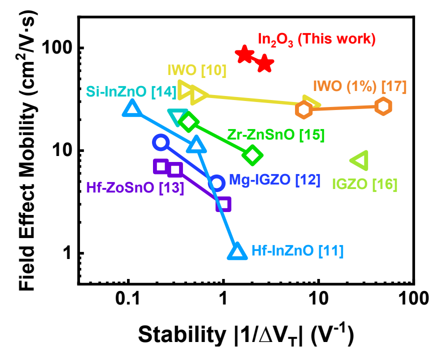

Fig. 24. Benchmark of stability and field-effect mobility of amorphous oxide TFTs. For GAA In_2O_3 FETs, μ_{FE}= 86/70 $cm^2/V\cdot s$.