Few-Layer Black Phosporous PMOSFETs with BN/Al_2O_3 Bilayer Gate Dielectric: Achieving I_{on}=850μA/μm, g_m=340μS/μm, and R_c=0.58kΩ·μm

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Abstract**—**In this paper, high-performance few-layer black phosphorus (BP) PMOSFETs have been demonstrated by using MOCVD BN and ALD Al_2O_3 as the top-gate dielectric as well as the passivation layer. Highest I_{on} of 850μA/μm (V_{ds} = -1.8V) and g_m of 340μS/μm (V_{ds} = -0.8V) have been achieved with the 200nm chancel length (L_{ch}) devices. Record low contact resistance (R_c) of 0.58kΩ·μm has been obtained on BP transistors by contact engineering. The gate leakage of the BN/Al_2O_3 bilayer gate dielectric is less than 10^{-12}A/μm^2 (V_g = -1V) with an EOT of 3nm. SS and hysteresis voltage as low as 70mV/dec and 0.1V have been achieved, indicating a high quality interface between BP and BN.

I. Introduction

BP is an exceptional two-dimensional (2D) material for high-performance transistor applications due to its excellent transport properties: i) intrinsically high electron and hole mobilities, i.e., hole mobility as high as 300-1000cm^2/Vs at room temperature [1,2]; ii) direct bandgap semiconductor with the bandgap of 0.35-2.0eV depending on the number of layers, which can find wide applications in electronics and photonics [3,4]. However, the device performance of BP PMOSFETs such as I_{on}, g_m, EOT, and R_c in literature are still far below what is expected due to the instability of BP in ambient reacting with O_2 and/or H_2O [5,6].

In this work, a bilayer gate dielectric of 1.6nm MOCVD sp^2-BN and 1.3nm ALD Al_2O_3 was used to passivate the BP channel from oxidation. Compared with un-passivated devices, the passivated devices showed significant performance improvement. Hysteresis as low as 0.1V and SS as low as 70mV/dec are achieved. Record high I_{on} of 850μA/μm (V_{ds} = -1.8V) and g_m of 340μS/μm (V_{ds} = -0.8V) have been demonstrated with a 200nm L_{ch} device. The gate leakage is less than 10^{-12}A/μm^2 (V_g = -1V) with an EOT of 3nm. Meanwhile, R_c as low as 0.58 kΩ·μm has also been demonstrated by contact engineering. It is shown that BN/Al_2O_3 is a high quality and scalable gate dielectric as well as an effective passivation layer for BP.

II. Experiment

Fig. 1 shows the schematic diagram of a BP MOSFET with BN/Al_2O_3 as gate dielectric. A top view SEM image of two connected100nm L_{ch} BP MOSFETs is shown in Fig. 2(a). Fig. 2(b) shows the element analysis along the gate stack direction, namely AA' in Fig. 1. Fig. 3 illustrates the STM image of a 4.5nm by 4.5nm freshly cleaved BP surface with 0.3V scanning bias showing the puckered structures with atomic resolution. The detail of fabrication is shown in Fig. 4. The sp^2-BN was grown by MOCVD at 1050°C on 1/4 2'' sapphire wafers. The roughness of BN on sapphire is less than 0.1nm and the film thickness is ~1.6nm measured by AFM, as shown in Fig. 5(a) and (b). Bulk BP was synthesized from red phosphorus using SnI_4/Sn as catalyst in sealed ampoules. Firstly, PMMA A10 and PDMS were coated on BN/sapphire wafers. The sapphire substrate was peeled after a few hours' soak in BOE. BP flakes (thickness of 4-12 nm) were exfoliated onto a 90nm SiO_2/p^{++} Si substrate. The PDMS/PMMA/BN film was transferred to the substrate after baking at 120°C for 30 minutes. The processes of BP exfoliation and BN transfer were all performed in a glovebox with H_2O and O_2 concentration less than 0.5ppm. The sample was baked at 100 °C for 30 minutes to improve the adhesion between BP and BN. PMMA and PDMS was removed by solvent cleaning followed by N_2 annealing at 180°C. After Source/Drain pattern, an optional low power O_2/Ar plasma etching was used to open the BN windows at the S/D regions. The samples were immediately loaded into a metallization chamber after etching. 5nm Pt/ 8nm Ni/ 30nm Al or 12nm Ni/ 30nm Al was deposited as the contact metals. Fig. 6 shows a cross-sectional TEM image of the S/D region with BN etched. After metal lift-off, 1.3nm Al_2O_3 was deposited with ALD at 200 °C. Finally, 10nm Ti/50nm Au was deposited as the top gate metal.

All patterns were defined with a VISTEC VB6 UHR e-beam lithography. Dry etching was performed with a Panasonic E620 high density plasma etcher. A HORIBA LabRAM HR800 Raman spectrometer was used for the Raman measurement with a 632.8nm wavelength He-Ne laser. All the devices were measured with a Keithley 4200 semiconductor parameters analyzer at room temperature.

III. Results and Discussion

BP has anisotropic hole motilities as the hole effective mass of armchair direction is 6-8 times larger than that of zigzag direction from DFT calculation [1]. Consequently, the armchair direction is identified with polarized Raman spectra and used as the channel direction for all devices, as shown in Fig. 7(a). Fig. 7(b) shows the time dependence of integrated intensity of A^1_g Raman mode of BP samples without BN, with BN, and with

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BN/Al_2O_3, respectively. Laser illumination is used to accelerate the degradation of BP [7]. Exposed in air, the normalized A^1_g Raman intensity of the freshly cleaved BP flake decreases exponentially within one hour, indicating its fast degradation in ambient. The degradation speed slows down when it is covered by BN only. Interestingly, no sign of degradation is observed when BP is covered by BN and Al_2O_3 with EOT of 3nm thick. It is shown that BN/Al_2O_3 bilayer dielectric can effectively suppresses the degradation of BP in ambient.

Fig. 8 (a) shows the C-V characteristics of 1.6nm BN and 6nm Al_2O_3. The extracted relative dielectric constant of the MOCVD BN is about 3.0, which is in agreement with the reported dielectric constant of CVD BN [8]. In Fig. 8 (b), the leakage current density of the 1.6nm BN/1.3nm Al_2O_3 gate dielectric is less than 10^{-12}A/μm^2 at V_g = -1V, which is comparable to SiO_2 with the same EOT.

Typical transfer curves of a back-gate (7.5nm HfO_2) BP transistor without any passivation techniques are shown in Fig. 9. The I-V hysteresis is as large as 2.5V [ΔE_{BP} = 6.0MV/cm; ΔE_{BP} is defined as $(\Delta V_g/EOT)\cdot(3.9/6.1)$;$k_{BP}$=6.1;$k_{SiO2}$=3.9]. Fig. 10 shows the transfer curves of a 500nm L_{ch} BP MOSFET with BN/Al_2O_3 as top gate dielectric, showing hysteresis of 0.25V (ΔE_{BP} = 0.6MV/cm). SS_{min} as low as 70mV/dec is achieved indicating a low-defect interface between BP and BN. The drain current is low because the BN above the S/D region was not etched avoiding the interface degradation due to the dry etching process. The transfer curves of a 200nm L_{ch} BP MOSFET with BN etched are shown in Fig. 11. The hysteresis is as low as 0.1V (ΔE_{BP} = 0.25MV/cm), which is reduced by a factor of 24, compared to the back-gated devices.

Table 1 summarizes different BP passivation techniques in literature [9-11]. Unfortunately, conventional ALD Al_2O_3 is not a viable method to reduce hysteresis since ALD usually needs H_2O as precursor and grows at high temperature. Vacuum annealing is reported to be an effective way to reduce hysteresis but it doesn't completely solve the degradation problem. It is also reported that hysteresis can be completely eliminated by sandwiching BP with thick exfoliated BN, but it cannot achieve the required EOT scaling. In this work, low hysteresis and small EOT can be achieved at the same time by using MOCVD BN and ALD Al_2O_3 bilayer dielectric.

Fig. 12 shows the linear I_d-V_g curve as well as the g_m-V_g curve of a 200nm L_{ch} BP MOSFET with V_{ds} = -0.8V. The peak g_m is about 340μS/μm, which is the highest reported value among all BP transistors. The threshold voltage is ~0.65V extracted by linear extrapolation. The field effect hole mobility is calculated to be 144 cm^2/Vs with C_g = 1.15μF/cm^2. It is known mobility could be under-estimated from short channel devices. The I_{on}/I_{off} is about 10^4 and 10^3 for V_d = -0.1 and -0.8V

The I_d-V_d curves of the same device are shown in Fig. 13. Record high I_{on} = 850μA/μm is achieved at V_d = -1.8V and V_g = -2V. No clear current saturation is observed when the channel current is along the high mobility direction. Fig. 14 shows the I_d-V_d curves of the same device with different back biases (V_{bg} = 0, -20, and -40V). Interestingly, the ON state is nearly independent of V_{bg} although the OFF state is still affected by V_{bg}. This indicates that the drain current flows through the top few layers which are strongly controlled by the top-gate. The contact resistance of top-gated devices doesn't change significantly through electrostatic doping from back gate.

To get a better understanding of the increase of I_{on}, R_c and sheet resistance (R_s) are extracted with a 12nm thick BP TLM structure, as shown in Fig. 15. Record low R_c of 0.58kΩ·μm for BP transistors has been obtained, which is one fifth of the previous reported value of Ni/BP contact at zero gate bias [12]. There are three factors that contribute to the low R_c: (i) protected by BN, no oxides of phosphorus exhibit at the BP/metal interface during the fabrication process; (ii) there is less interlayer resistance due to the top gate structure, which is an important part of R_c for back gate structure; (iii) high work-function metal Pt is used to form a lower Schottky barrier at the BP/metal contact. Fig. 16 shows the transfer curves of two BP MOSFETs with (a) Pt/Ni/Al and (b) Ni/Al as contact metals. The I_{on} of the device with Pt/Ni/Al contact is about 1.6 times higher than that of device with Ni/Al contact.

The anisotropic characteristics of BP is also investigated. Fig. 17 and 18 depict the output and transfer characteristics of a 200nm L_{ch} BP MOSEFT along the zigzag direction. Unlike the armchair devices, the drain current of zigzag device starts to saturate at V_d = -1V due to its lower mobility. The hole mobility is calculated to be 51 cm^2/Vs, which is about one third of the armchair mobility. The I_{on}/I_{off} is as high as 10^5 and 10^4 for V_d = -0.1 and -1V due to the smaller thickness. The time dependent I_d-V_g curves are presented in Fig. 19. The device still works properly after 20 days although minor V_{th} shift is observed. Finally, Table 2 benchmarks the device metrics such as EOT, I_{on}, g_m, R_c, I_{on}/I_{off} of this work with other BP transistor results in literature [12-15].

IV. CONCLUSION

High-performance BP MOSFETs with I_{on} = 850μA/μm, g_m of 340μS/μm, EOT = 3nm, and R_c = 0.58kΩ·μm have been successfully demonstrated in this work. The significant performance improvement is attributed to the BN/Al_2O_3 bilayer dielectric, which served as a top gate dielectric and a passivation layer. I-V hysteresis and SS as low as 0.1V and 70mV/dec have also been demonstrated.

ACKNOWLEDGMENT

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REFERENCES

[1] H. Liu et al., *ACS Nano*, 2014, p. 4033. [2] L. Li et al., *Nature Nano* 2014, p. 372. [3] V. Tran et al., *Phys. Rev. B*, 2014, p. 235319. [4] T. Takahashi et al. *J. Phys. C Solid State Phys*., 1985 18, p. 825. [5] Y. Huang et al. *arXiv:* 1511.09201, 2015. [6] J. D. Wood et al. *Nano Lett.*, 2014, p. 6964. [7] A. Favron et al., *Nature Materials*, 2015, p. 826. [8] S. Kim et al., *Nature Comm.*, 2015, p. 9662. [9] J. Kim et al., *Scientific Reports*, 2015, p. 8989. [10] L. Li et al., *ACS NANO*, 2016, p. 4672. [11] X. Chen et al., *Nature Comm.*, 2015, p. 7315. [12] Y. Du et al., *IEEE EDL*, 2016, p. 429. [13] H. Liu et al.,*IEEE EDL*, 2014, p. 795. [14] N. Haratipour et al., *IEEE EDL*, 2015, p. 411. [15] H. Wang et al., *Nano Lett.*, 2014, p. 6424.

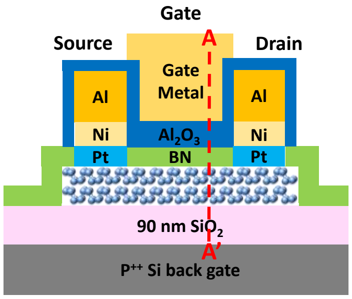

Fig. 1. Schematic diagram of a BP PMOSFET with BN/Al_2O_3 gate dielectric.

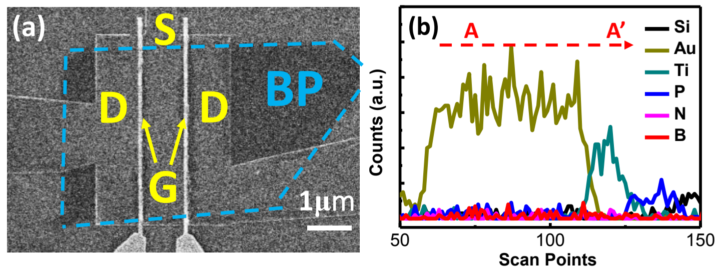

Fig. 2. (a) Top-view SEM image of two BP MOSFETs with BN/Al_2O_3 top gate dielectric. (b) EDS element analysis along the AA' gate direction.

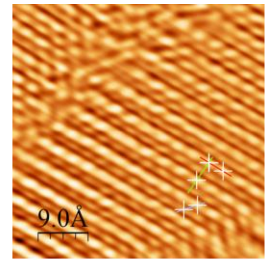

Fig. 3. STM image of a freshly cleaved BP surface showing atomic puckered structures.

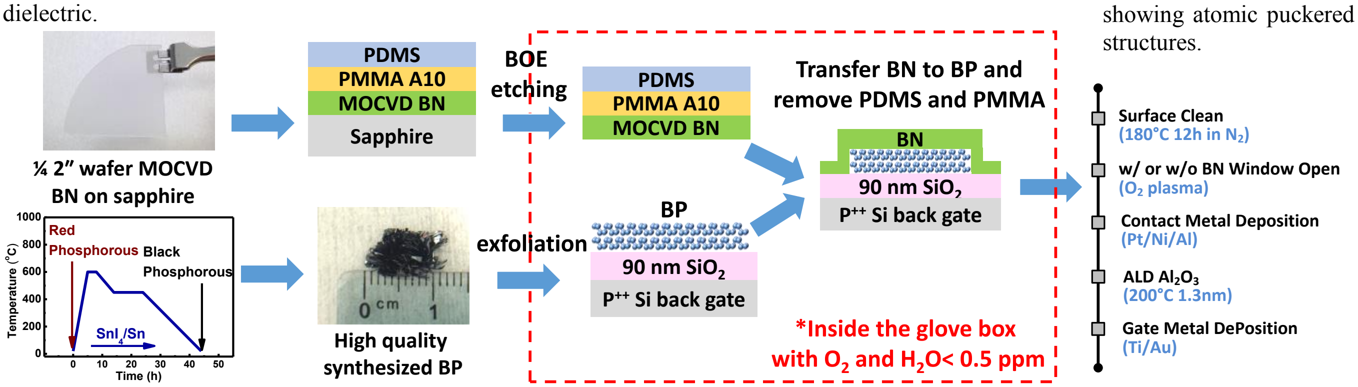

Fig. 4. Fabrication process flow for the BP MOSFET. Key steps include: (i) MOCVD BN; (ii) bulk BP growth; (iii) BP exfoliation; (iv) BN transfer; (v) BN dry etching; (vi) ALD Al_2O_3. BP exfoliation and BN transfer were performed in glovebox filled with high purity Ar.

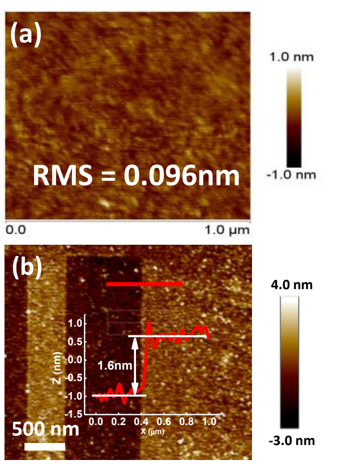

Fig. 5. AFM image of (a) BN on sapphire with RMS = 0.096 nm and (b) BN after dry etching. The thickness of BN is 1.6 nm.

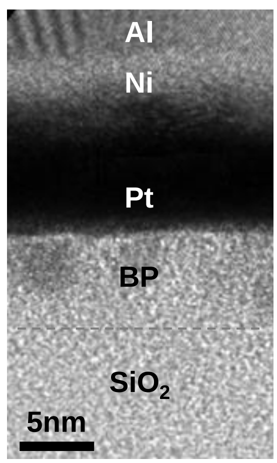

Fig. 6. Cross-sectional TEM image of the Pt/BP contact after BN etching.

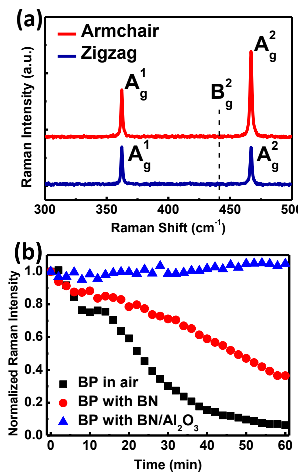

Fig. 7. (a) BP anisotropic Raman. (b) Time dependence of A^1_g Raman intensity of BP w/o BN, w/ BN, and w/ BN and Al_2O_3.

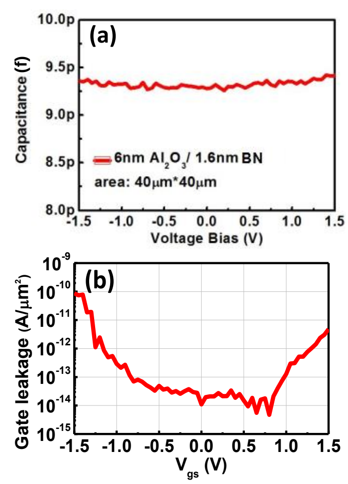

Fig. 8. (a) C-V of a BN/Al_2O_3 capacitor; (b) gate leakage vs. V_g of 1.6nm BN/1.3nm Al_2O_3.

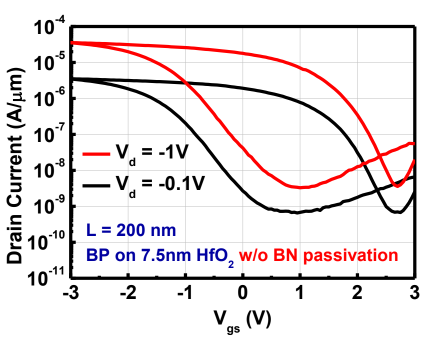

Fig. 9. Typical due sweep I_d-V_g of a 200nm L_{ch} BP MOSFET with 7.5nm HfO_2 as back gate oxide. No passivation technique is used.

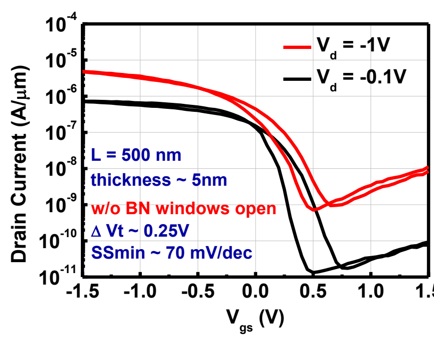

Fig. 10. I_d-V_g of a 500nm L_{ch} BP FET with BN/Al_2O_3 as gate dielectric without source/drain BN etching.

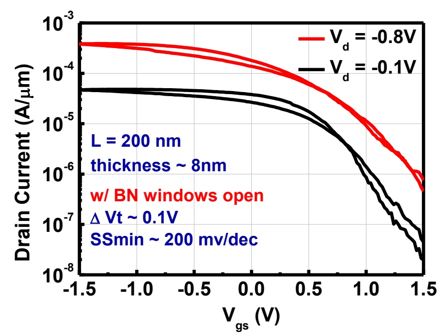

Fig. 11. I_d-V_g of a 200nm L_{ch} BP MOSFET with BN/Al_2O_3 as gate dielectric. The source/drain BN was etched. Hysteresis is as low as 0.1V.

	Gate Oxide/ passivation	ΔV_g	ΔE_{bp}	Remarks
1* without passivation	7.5nm HfO_2 as back gate, no passivation	2.5V	6 MV/cm	Large hysteresis due to oxidation
2* ALD Al_2O_3 only [9]	5nm Al_2O_3 as front gate and passivation layer	2.5V	6 MV/cm	No obvious improvement
3* vacuum annealing [10]	10nm SiO_2 as back gate; annealed in vacuum	0.4V	0.3 MV/cm	Hysteresis is reduced but it requires vacuum
4* BN sandwich + annealing [11]	Exfoliated thick BN as back gate and front passivation layer	0	0	No hysteresis but difficult to scale down
5* this work: BN/Al_2O_3	1.6nm BN/1.3nm Al_2O_3 as front gate and passivation layer	0.1-0.25V	0.25-0.6 MV/cm	low hysteresis and small EOT

Table 1. Comparison of BP passivation techniques: 1) no passivation; 2) ALD Al_2O_3 as top gate; 3) vacuum annealing; 4) sandwiched with top and bottom BN and annealing; 5) this work.

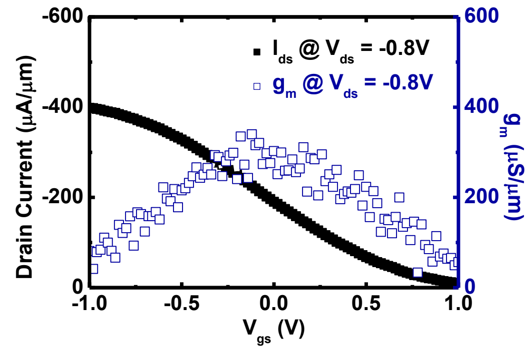

Fig. 12. Linear I_d-V_g and g_m-V_g curve (V_d = -0.8V) of the same device in Fig. 11.

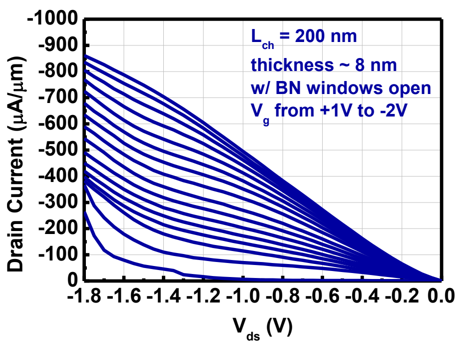

Fig. 13. I_d-V_d of the same device in Fig. 11. I_{on} of 850μA/μm was obtain with V_d= -1.8V and V_g= -2V.

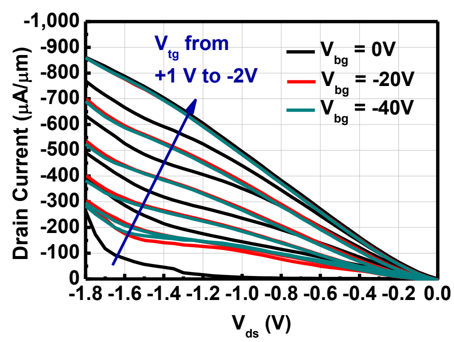

Fig. 14. Back gate bias dependence of I_d-V_d of the same device in Fig. 11. I_{on} is nearly intendent of V_{bg}.

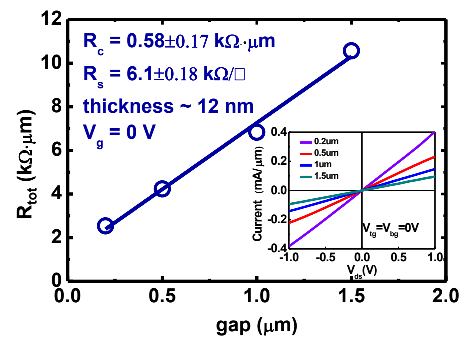

Fig. 15. TLM resistance on BP with Pt/Ni/Al contact. Inset shows the I-V curves between two contacts with different gap length.

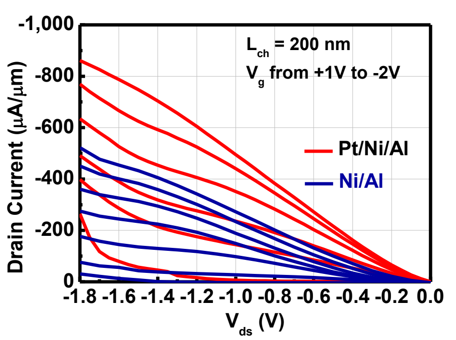

Fig. 16. I_d-V_d of 200nm L_{ch} BP MOSFETs with Pt/Ni/Al and Ni/Al contacts.

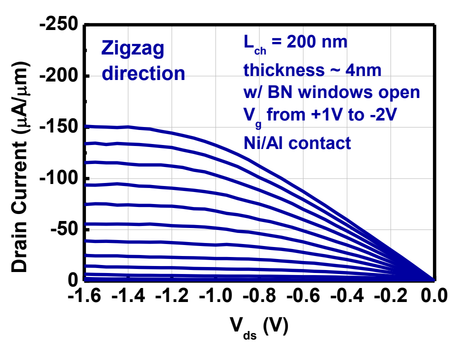

Fig. 17. I_d-V_d of a 200nm L_{ch} BP MOSFET with Ni/Al contact along the zigzag direction.

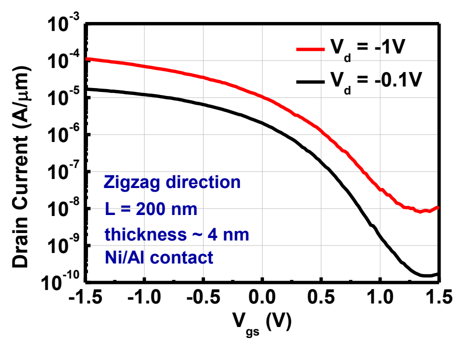

Fig. 18. I_d-V_g of the same device in Fig. 17. I_{on}/I_{off} is about 10^5 and 10^4 at V_{ds} = -0.1 and -1V, respectively.

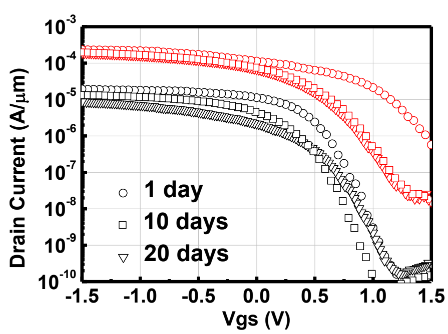

Fig. 19. Time dependence of I_d-V_g of a 200nm L_{ch} BP MOSFET with Ni/Al contact.

	1# Purdue	2# Purdue	3# Uni. of Minnesota	4# USC	5# Stanford	6# This Work
L_{ch}	0.5μm	1.5μm	170nm	300nm	1μm	200nm
Gate Oxide	16nm Al_2O_3	90nm SiO_2	7nm HfO_2	21nm HfO_2	10nm SiO_2	1.6nm BN/1.3nm Al_2O_3
S/D Metal	Ni/Au	Ni	Ti/Au	Ti/Pd/Au	Sc/Au	Pt/Ni/Al
I_{on}	144μA/μm (V_d = -1V)	210μA/μm (V_d = -2V) *w/o doping	300μA/μm (V_d = -2V)	270μA/μm (V_d = -2V)	482μA/μm (V_d = -2V)	850μA/μm (V_d = -1.8V)
g_m	3.3μS/μm (V_d = -0.5V)	NA	250μS/μm (V_d = -2V)	180μS/μm (V_d = -2V)	NA	340μS/μm (V_d = -0.8V)
R_c	NA	1.3kΩ•μm (V_g = -40V)	1.14kΩ•μm (V_g = -1.5V)	NA	NA	0.58kΩ•μm (V_g = 0V)
I_{on}/I_{off}	~10^3 (V_d = -0.1V)	~10^3 (V_d = -0.01V)	~10^3 (V_d = -0.1V)	~$2*10^3$ (V_d = -2V)	~10^3-10^5 (V_d = -0.7V)	~10^3-10^5 (V_d = -0.1V)

Table 2. Benchmark of device metrics of this work with other results in literature [12-15].