Few-Layer Black Phosphorus PMOSFETs with BN/Al₂O₃ Bilayer Gate Dielectric: Achieving $I_{on}=850\mu A/\mu m$, $g_m=340\mu S/\mu m$, and $R_c=0.58k\Omega\cdot\mu m$

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Abstract—In this paper, high-performance few-layer black phosphorus (BP) PMOSFETs have been demonstrated by using MOCVD BN and ALD Al₂O₃ as the top-gate dielectric as well as the passivation layer. Highest $I_{on}$ of $850\mu A/\mu m$ ($V_{ds} = -1.8V$) and $g_m$ of $340\mu S/\mu m$ ($V_{ds} = -0.8V$) have been achieved with the 200nm channel length ($L_{ch}$) devices. Record low contact resistance ($R_c$) of 0.58kΩ·µm has been obtained on BP transistors by contact engineering. The gate leakage of the BN/Al₂O₃ bilayer gate dielectric is less than $10^{-12} A/µm^2$ ($V_g = -1V$) with an EOT of 3nm. SS and hysteresis voltage as low as 70mV/dec and 0.8V have been achieved, indicating a high quality interface between BP and BN.

I. INTRODUCTION

BP is an exceptional two-dimensional (2D) material for high-performance transistor applications due to its excellent transport properties: i) intrinsically high electron and hole mobilities, i.e., hole mobility as high as 300-1000cm²/Vs at room temperature [1,2]; ii) direct bandgap semiconductor with the bandgap of 0.35-2.0eV depending on the number of layers, which can find wide applications in electronics and photonics [3,4]. However, the device performance of BP PMOSFETs such as $I_{on}$, $g_m$, EOT, and $R_c$ in literature are still far below what is expected due to the instability of BP in ambient reacting with $O_2$ and/or $H_2O$ [5,6].

In this work, a bilayer gate dielectric of 1.6nm MOCVD sp²-BN and 1.3nm ALD Al₂O₃ was used to passivate the BP channel from oxidation. Compared with un-passivated devices, the passivated devices showed significant performance improvement. Hysteresis as low as 0.1V and SS as low as 70mV/dec are achieved. Record high $I_{on}$ of $850\mu A/\mu m$ ($V_{ds} = -1.8V$) and $g_m$ of $340\mu S/\mu m$ ($V_{ds} = -0.8V$) have been demonstrated with a 200nm $L_{ch}$ device. The gate leakage is less than $10^{-12} A/µm^2$ ($V_g = -1V$) with an EOT of 3nm. Meanwhile, $R_c$ as low as 0.58 kΩ·µm has also been demonstrated by contact engineering. It is shown that BN/Al₂O₃ is a high quality and scalable gate dielectric as well as an effective passivation layer for BP.

II. EXPERIMENT

Fig. 1 shows the schematic diagram of a BP MOSFET with BN/Al₂O₃ as gate dielectric. A top view SEM image of two connected100nm $L_{ch}$ BP MOSFETs is shown in Fig. 2(a). Fig. 2(b) shows the element analysis along the gate stack direction, namely AA’ in Fig. 1. Fig. 3 illustrates the STM image of a 4.5nm by 4.5nm freshly cleaved BP surface with 0.3V scanning bias showing the puckered structures with atomic resolution. The detail of fabrication is shown in Fig. 4. The sp³-BN was grown by MOCVD at 1050°C on 1/4 2” sapphire wafers. The roughness of BN on sapphire is less than 0.1nm and the film thickness is ~1.6nm measured by AFM, as shown in Fig. 5(a) and (b). Bulk BP was synthesized from red phosphorus using SnI₂/Sn as catalyst in sealed ampoules. Firstly, PMMA A10 and PDMS were coated on BN/sapphire wafers. The sapphire substrate was peeled after a few hours’ soak in BOE. BP flakes (thickness of 4-12 nm) were exfoliated onto a 90nm SiO₂/p⁺ Si substrate. The PDMS/PMMA/BN film was transferred to the substrate after baking at 120°C for 30 minutes. The processes of BP exfoliation and BN transfer were all performed in a glovebox with $H_2O$ and $O_2$ concentration less than 0.5ppm. The sample was baked at 100°C for 30 minutes to improve the adhesion between BP and BN. PMMA and PDMS was removed by solvent cleaning followed by $N_2$ annealing at 180°C. After Source/Drain pattern, an optional low power $O_2/Ar$ plasma etching was used to open the BN windows at the S/D regions. The samples were immediately loaded into a metalization chamber after etching. 5nm Pt/ 8nm Ni/ 30nm Al or 12nm Ni/ 30nm Al was deposited as the contact metals. Fig. 6 shows a cross-sectional TEM image of the S/D region with BN etched. After metal lift-off, 1.3nm Al₂O₃ was deposited with ALD at 200°C. Finally, 10nm Ti/50nm Au was deposited as the top gate metal.

All patterns were defined with a VISTEC VB6 UHR e-beam lithography. Dry etching was performed with a Panasonic E620 high density plasma etcher. A HORIBA LabRAM HR800 Raman spectrometer was used for the Raman measurement with a 632.8nm wavelength He-Ne laser. All the devices were measured with a Keithley 4200 semiconductor parameters analyzer at room temperature.

III. RESULTS AND DISCUSSION

BP has anisotropic hole mobilities as the hole effective mass of armchair direction is 6-8 times larger than that of zigzag direction from DFT calculation [1]. Consequently, the armchair direction is identified with polarized Raman spectra and used as the channel direction for all devices, as shown in Fig. 7(a). Fig. 7(b) shows the time dependence of integrated intensity of $A_s^{1}$ Raman mode of BP samples without BN, with BN, and with...
BN/Al2O3, respectively. Laser illumination is used to accelerate the degradation of BP [7]. Exposed in air, the normalized A1g Raman intensity of the freshly cleaved BP flake decreases exponentially within one hour, indicating its fast degradation in ambient. The degradation speed slows down when it is covered by BN only. Interestingly, no sign of degradation is observed when BP is covered by BN and Al2O3 with EOT of 3nm thick. It is shown that BN/Al2O3 bilayer dielectric can effectively suppresses the degradation of BP in ambient.

Fig. 8 (a) shows the C-V characteristics of 1.6nm BN and 6nm Al2O3. The extracted relative dielectric constant of the MOCVD BN is about 3.0, which is in agreement with the reported dielectric constant of CVD BN [8]. In Fig. 8 (b), the leakage current density of the 1.6nm BN/13nm Al2O3 gate dielectric is less than 10^{-12}A/μm² at Vg = -1V, which is comparable to SiO2 with the same EOT.

Typical transfer curves of a back-gate (7.5nm H2O) BP transistor without any passivation techniques are shown in Fig. 9. The I-V hysteresis is as large as 2.5V [ΔEdrain = 6.0MV/cm, ΔEdrain is defined as (ΔVf/ΔEOT)-3(9.6/1.1)kBT=6.1/kBT=3.9]. Fig. 10 shows the transfer curves of a 500nm Lch BP MOSFET with BN/Al2O3 as top gate dielectric, showing hysteresis of 0.25V (ΔEdrain = 0.6MV/cm). SSmn as low as 70mV/dec is achieved indicating a low-defect interface between BP and BN. The drain current is low because the BN above the S/D region was not etched avoiding the interface degradation due to the dry etching process. The transfer curves of a 200nm Lch BP MOSFET with BN etched are shown in Fig. 11. The hysteresis is as low as 0.1V (ΔEdrain = 0.25MV/cm), which is reduced by a factor of 24, compared to the back-gated devices.

Table 1 summarizes different BP passivation techniques in literature [9-11]. Unfortunately, conventional ALD Al2O3 is not a viable method to reduce hysteresis since ALD usually needs H2O as precursor and grows at high temperature. Vacuum annealing is reported to be an effective way to reduce hysteresis but it doesn‘t completely solve the degradation problem. It is also reported that hysteresis can be completely eliminated by sandwiching BP with thick exfoliated BN, but it cannot achieve the required EOT scaling. In this work, low hysteresis and small EOT can be achieved at the same time by using MOCVD BN and ALD Al2O3 bilayer dielectric.

Fig. 12 shows the linear Ioff-Vg curve as well as the g_m-Vg curve of a 200nm Lch BP MOSFET with Vth = -0.8V. The peak g_m is about 340μS/μm, which is the highest reported value among all BP transistors. The threshold voltage is -0.65V extracted by linear extrapolation. The field effect hole mobility is calculated to be 440cm²/Vs with Cg = 1.15μF/cm². It is known mobility could be under-estimated from short channel devices. The Ioff/Ion is about 10⁴ and 10³ for Vg = -0.1 and -0.8V.

The Ioff-Vg curves of the same device are shown in Fig. 13. Record high Ion = 850μA/μm is achieved at Vg = -1.8V and Vg = -2V. No clear current saturation is observed when the channel current is along the high mobility direction. Fig. 14 shows the Ioff-Vg curves of the same device with different back biases (Vbg = 0, -20, and -40V). Interestingly, the ON state is nearly independent of Vbg although the OFF state is still affected by Vbg. This indicates that the drain current flows through the top few layers which are strongly controlled by the top-gate. The contact resistance of top-gated devices doesn’t change significantly through electrostatic doping from back gate.

To get a better understanding of the increase of Ion, Roff and sheet resistance (R_s) are extracted with a 12nm thick BP TLM structure, as shown in Fig. 15. Record low Roff of 0.85kΩ for BP transistor has been obtained, which is one fifth of the previous reported value of Ni/BP contact at zero gate bias [12]. There are three factors that contribute to the low Roff: (i) protected by BN, no oxides of phosphorus exhibit at the BP/metal interface during the fabrication process; (ii) there is less interlayer resistance due to the top gate structure, which is an important part of Roff for back gate structure; (iii) high work-function metal Pt is used to form a lower Schottky barrier at the BP/metal contact. Fig. 16 shows the transfer curves of two BP MOSFETs with (a) Pt/Ni/Al and (b) Ni/Al as contact metals. The Ion of the device with Pt/Ni/Al contact is about 1.6 times higher than that of device with Ni/Al contact.

The anisotropic characteristics of BP is also investigated. Fig. 17 and 18 depict the output and transfer characteristics of a 200nm Lch BP MOSFET along the zigzag direction. Unlike the armchair devices, the drain current of zigzag device starts to saturate at Vd = -1V due to its lower mobility. The hole mobility is calculated to be 51cm²/Vs, which is about one third of the armchair mobility. The Ion/Ioff is as high as 10⁴ and 10⁴ for Vg = -0.1 and -1V due to the smaller thickness. The time dependent Ioff-Vg curves are presented in Fig. 19. The device still works properly after 20 days although minor Vth shift is observed. Finally, Table 2 benchmarks the device metrics such as EOT, Ion, g_m, Roff, Ion/Ioff of this work with other BP transistor results in literature [12-15].

IV. CONCLUSION

High-performance BP MOSFETs with Ion = 850μA/μm, g_m of 340μS/μm, EOT = 3nm, and R_s = 0.85kΩ have been successfully demonstrated in this work. The significant performance improvement is attributed to the BN/Al2O3 bilayer dielectric, which served as a top gate dielectric and a passivation layer. I-V hysteresis and SS as low as 0.1V and 70mV/dec have also been demonstrated.

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REFERENCES

Fig. 1. Schematic diagram of a BP PMOSFET with BN/Al2O3 gate dielectric.

Fig. 2. (a) Top-view SEM image of two BP MOSFETs with BN/Al2O3 top gate dielectric. (b) EDS element analysis along the AA’ gate direction.

Fig. 3. STM image of a freshly cleaved BP surface showing atomic puckered structures.

Fig. 4. Fabrication process flow for the BP MOSFET. Key steps include: (i) MOCVD BN; (ii) bulk BP growth; (iii) BP exfoliation; (iv) BN transfer; (v) BN dry etching; (vi) ALD Al2O3. BP exfoliation and BN transfer were performed in glovebox filled with high purity Ar.

Fig. 5. AFM image of (a) BN on sapphire with RMS = 0.096 nm and (b) BN after dry etching. The thickness of BN is 1.6 nm.

Fig. 6. Cross-sectional TEM image of the Pt/BP contact after BN etching.

Fig. 7. (a) BP anisotropic Raman. (b) Time dependence of A1g Raman intensity of BP w/o BN, w/ BN, and w/ BN and Al2O3.

Fig. 8. (a) C-V of a BN/Al2O3 capacitor; (b) gate leakage vs. Vg of 1.6nm BN/1.3nm Al2O3.

Fig. 9. Typical due sweep Ld-Vg of a 200nm Lch BP MOSFET with 7.5nm H2O2 as back gate oxide. No passivation technique is used.

Fig. 10. Ld-Vg of a 500nm Lch BP FET with BN/Al2O3 as gate dielectric without source/drain BN etching.

Fig. 11. Ld-Vg of a 200nm Lch BP MOSFET with BN/Al2O3 as gate dielectric. The source/drain BN was etched. Hysteresis is as low as 0.1V.
Table 1. Comparison of BP passivation techniques: 1) no passivation; 2) ALD Al₂O₃ as top gate; 3) vacuum annealing; 4) sandwiched with top and bottom BN and annealing; 5) this work.

<table>
<thead>
<tr>
<th>Gate Oxide/ passivation</th>
<th>ΔV₉</th>
<th>ΔEₜₚ</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1° without passivation</td>
<td>7.5nm HfO₂ as back gate, no passivation</td>
<td>2.5V</td>
<td>Large hysteresis due to oxidation</td>
</tr>
<tr>
<td>2° ALD Al₂O₃ only [9]</td>
<td>5nm Al₂O₃ as front gate and passivation layer</td>
<td>2.5V</td>
<td>No obvious improvement</td>
</tr>
<tr>
<td>3° vacuum annealing [10]</td>
<td>10nm SiO₂ as back gate; annealed in vacuum</td>
<td>0.4V</td>
<td>Hysteresis is reduced but it requires vacuum</td>
</tr>
<tr>
<td>4° BN sandwich + annealing [11]</td>
<td>Exfoliated thick BN as back gate and front passivation layer</td>
<td>0</td>
<td>No hysteresis but difficult to scale down</td>
</tr>
<tr>
<td>5° this work: BN/Al₂O₃</td>
<td>1.6nm BN/1.3nm Al₂O₃ as front gate and passivation layer</td>
<td>0.1-0.25V</td>
<td>low hysteresis and small EOT</td>
</tr>
</tbody>
</table>

Fig. 13. Iₘₜ-Vₙ of the same device in Fig. 11. Iₘₜ of 850μA/μm was obtain with Vₙ= -1.8V and Vₙ= -2V.

Fig. 14. Back gate bias dependence of Iₘₜ-Vₙ of the same device in Fig. 11. Iₘₜ is nearly intendent of Vₙ.

Fig. 15. TLM resistance on BP with Pt/Ni/Al contact. Inset shows the I-V curves between two contacts with different gap length.

Table 2. Benchmark of device metrics of this work with other results in literature [12-15].

<table>
<thead>
<tr>
<th>Remarks</th>
<th>1° Purdue</th>
<th>2° Purdue</th>
<th>3° Uni. of Minnesota</th>
<th>4° USC</th>
<th>5° Stanford</th>
<th>6° This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>lₘₜ</td>
<td>0.5µm</td>
<td>1.5µm</td>
<td>170nm</td>
<td>300nm</td>
<td>1µm</td>
<td>200nm</td>
</tr>
<tr>
<td>Gate Oxide</td>
<td>16nm Al₂O₃</td>
<td>90nm SiO₂</td>
<td>7nm HfO₂</td>
<td>21nm HfO₂</td>
<td>10nm SiO₂</td>
<td>1.6nm BN/1.3nm Al₂O₃</td>
</tr>
<tr>
<td>S/D Metal</td>
<td>Ni/Au</td>
<td>Ni</td>
<td>Ti/Au</td>
<td>Ti/Pd/Au</td>
<td>Sc/Au</td>
<td>Pt/Ni/Al</td>
</tr>
<tr>
<td>lₘ</td>
<td>144µA/µm (Vₙ = -1V)</td>
<td>210µA/µm (Vₙ = -2V)</td>
<td>300µA/µm (Vₙ = -2V)</td>
<td>270µA/µm (Vₙ = -2V)</td>
<td>482µA/µm (Vₙ = -2V)</td>
<td>850µA/µm (Vₙ = -1.8V)</td>
</tr>
<tr>
<td>rₘ</td>
<td>3.3µS/µm (Vₙ = -0.5V)</td>
<td>NA</td>
<td>250µS/µm (Vₙ = -2V)</td>
<td>180µS/µm (Vₙ = -2V)</td>
<td>NA</td>
<td>340µS/µm (Vₙ = -0.8V)</td>
</tr>
<tr>
<td>Rₗ</td>
<td>NA</td>
<td>1.3kΩ/µm (Vₙ = -40V)</td>
<td>1.14kΩ/µm (Vₙ = -1.5V)</td>
<td>NA</td>
<td>NA</td>
<td>0.58kΩ/µm (Vₙ = 0V)</td>
</tr>
<tr>
<td>Iₘₜ/Iₘₜ</td>
<td>~10³ (Vₙ = -0.1V)</td>
<td>~10³ (Vₙ = -0.01V)</td>
<td>~10³ (Vₙ = -0.1V)</td>
<td>~2*10³ (Vₙ = -2V)</td>
<td>~10¹-10³ (Vₙ = -0.7V)</td>
<td>~10¹-10³ (Vₙ = -0.1V)</td>
</tr>
</tbody>
</table>

Fig. 16. Iₘₜ-Vₙ of 200nm Lₘₜ BP MOSFETs with Pt/Ni/Al and Ni/Al contacts.

Fig. 17. Iₘₜ-Vₙ of a 200nm Lₘₜ BP MOSFET with Ni/Al contact along the zigzag direction.

Fig. 18. Iₘₜ-Vₙ of the same device in Fig. 17. Iₘₜ/Iₘₜ is about 10³ and 10⁴ at Vₙ = -0.1 and -1V, respectively.

Fig. 19. Time dependence of Iₘₜ-Vₙ of a 200nm Lₘₜ BP MOSFET with Ni/Al contact.