Monolithic 3D Integration of Vertically Stacked CMOS Devices and Circuits with High-Mobility Atomic-Layer-Deposited In_2O_3 n-FET and Polycrystalline Si p-FET: Achieving Large Noise Margin and High Voltage Gain of 134 V/V

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***Abstract*—**In this work, we demonstrate the monolithic 3D integration (M3D) of vertically stacked p-type low-temperature polycrystalline silicon (LTPS) top-gate transistor and n-type back-gate oxide semiconductor transistor, similar to a complementary field-effect transistor (CFET) structure, for complementary metal-oxide-semiconductor (CMOS) logic applications, with a low thermal budget of 450 °C. High-performance logic devices and circuits (inverter, NAND, NOR) are demonstrated with a high voltage gain of 134.3 V/V and a large noise margin of 0.84 V at V_{DD} of 2 V, which are among the best values in reported CMOS inverters by oxide semiconductor n-FET and LTPS p-FET. These devices are enabled by a high electron mobility atomic-layer-deposited (ALD) In_2O_3 as n-channel to balance the high hole mobility of LTPS. The fabricated ALD In_2O_3 n-FETs exhibit high electron mobility > 100 $cm^2/V{\cdot}s$ on SiO_2/Si substrate and mobility of 23.8 $cm^2/V{\cdot}s$ in the n-FET of the M3D CMOS inverter, which is the highest number in reported CMOS inverters with oxide semiconductor n-FETs and LTPS p-FETs.

I. Introduction

Oxide semiconductors such as indium oxide (In_2O_3) [1-4], indium gallium zinc oxide (IGZO) [5-8], indium tungsten oxide (IWO) [9], indium tin oxide (ITO) [10] are considered as promising n-type channel materials for back-end-of-line (BEOL) compatible devices for monolithic 3D integration (M3D) [11], due to their low-temperature process, high electron mobility and low off-leakage current. However, a p-type device with low thermal budget is required for complementary metal-oxide-semiconductor (CMOS) applications. Low-temperature polycrystalline silicon (LTPS) is a potentially suitable candidate for p-FET channel because of the high hole mobility and low-temperature fabrication process at about 400-450 °C [12-16]. Considering the low off-leakage current of oxide semiconductor transistors, the M3D of oxide semiconductor n-FET and LTPS p-FET could not only furtherly improve the area efficiency of CMOS logic circuits with potential on BEOL compatibility, but also be capable for dynamic random-access memory (DRAM) application, particularly for the 2T0C architecture [7, 17-21], taking advantage of the wide bandgap nature of oxide semiconductors for long retention time.

In this work, we report the experimental demonstration of the M3D of vertically stacked ALD In_2O_3 n-FET and LTPS p-FET for CMOS logic applications. The fabricated ALD In_2O_3 n-FETs exhibit high electron mobility > 100 $cm^2/V{\cdot}s$ on SiO_2/Si and mobility of 23.8 $cm^2/V{\cdot}s$ in the n-FET of the M3D CMOS inverter, which is the highest electron mobility reported in CMOS inverter with oxide semiconductor n-FET and LTPS p-FET. A high inverter gain > 134.3 V/V and a large noise margin of 0.84 V at V_{DD} of 2 V are achieved, indicating high-performance CMOS logic is achieved through the M3D of ALD In_2O_3 n-FET and LTPS p-FET. The M3D integration process of ALD In_2O_3 n-FET and LTPS p-FET with a low thermal budget of 450 °C provides a promising route toward 3D CMOS logic and embedded memory applications.

II. Experiments

Fig. 1 shows a schematic diagram of an M3D CMOS inverter with vertically stacked ALD In_2O_3 n-FET and LTPS p-FET, similar to a complementary field-effect transistor (CFET) structure. Top-gate structure is used for LTPS p-FET while back-gate structure is used for ALD In_2O_3 n-FET, so that the gate electrode can be shared by both n-FET and p-FET. Such structure can be directly applied to CMOS logic such as inverter, NAND, NOR, etc. Fig. 2 and Fig. 3 show the fabrication process flow. The fabrication process started with the plasma-enhanced chemical vapor deposition (PECVD) deposition of 47.5 nm thick a-Si on a glass substrate with SiO_2 and SiN_x buffer layer, followed by dehydrogenation and excimer-laser annealing (ELA) at or below 450 °C to form the poly-Si channel. A 140 nm thick SiN_x/SiO_2 layer was deposited as the gate insulator (GI) by PECVD at 360 °C after channel isolation. Then, a Mo layer of 300 nm was deposited by physical vapor deposition (PVD) and patterned to form the gate electrode. At the S/D region of LPTS p-FET, p+ implantation was performed, followed by annealing at 380 °C for dopant activation. Subsequently, an interlayer dielectric (ILD) of SiO_2/SiN_x stack was deposited, followed by via hole (VIA-1) opening for S/D contacts (Ti/Al/Ti). A planarization layer (PLN) was then formed with via hole (VIA-2) defined for interconnection. A 50 nm thick ITO layer was deposited as the contact electrode and also as the gate electrode for ALD In_2O_3 n-FET. 12 nm Al_2O_3 as gate insulator and In_2O_3 as n-type channel were then deposited by ALD at 200 °C, with $(CH_3)_3Al$ (TMA), $(CH_3)_3In$ (TMIn) and H_2O as Al, In and O precursors. Channel isolation was performed by wet etching using diluted hydrochloric acid. Ni S/D electrodes were then evaporated, which were patterned by photolithography. The thermal budget of the M3D fabrication process in this work is about 450 °C so that it has the potential to be compatible with back-end-of-line (BEOL) process of Si CMOS. ALD In_2O_3 transistors were also fabricated on SiO_2/Si substrate using a similar fabrication process with 5 nm HfO_2 as gate insulator, as developed in ref. [3], as control group for comparison with the M3D process.

III. Results and Discussion

Fig. 4(a) shows a cross-sectional SEM image of an M3D CMOS inverter, capturing the vertically stacked LTPS p-FET and

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ALD In_2O_3 n-FET. The LTPS p-FET at the bottom layer has a top-gate structure with Mo as gate electrode and ALD In_2O_3 n-FET has a back-gate structure with ITO as gate electrode. The vias connecting the gate electrodes and S/D electrodes of LTPS p-FET and ALD In_2O_3 n-FET are absent in the cross-section image because these vias are not located at the plane of focused ion beam (FIB) cut. Fig. 4(b) presents the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image and the corresponding energy dispersive spectroscopy (EDS) mapping of the ITO/Al_2O_3/In_2O_3/Ni gate stack of the ALD In_2O_3 n-FET, capturing the ITO gate electrode, Al_2O_3 gate insulator, ultrathin In_2O_3 channel, and Ni S/D contacts. Fig. 4(c) presents the bright-field (BF) STEM image and the corresponding EDS mapping of the poly-Si/SiO_2/SiN_X/Mo gate stack of the LTPS p-FET. Fig. 5 shows the top-view photo image of fabricated CMOS inverter, NAND, and NOR logic gates. The effective layout area can be significantly reduced due to the vertically stacked n-FET and p-FET by the M3D process.

Fig. 6 shows the transfer characteristics of two typical long channel ALD In_2O_3 transistors with 5 nm HfO_2 as gate dielectrics, with different channel thickness (T_{ch}), fabricated on a SiO_2/Si substrate. The device fabrication process on SiO_2/Si substrate was developed in our previous work with mobility > 100 $cm^2/V{\cdot}s$, where threshold voltage (V_T) can be tuned by thickness and thermal engineering [3]. Fig. 7 presents the field-effect mobility (μ_{FE}) extracted from the transconductance (g_m) at low V_{DS} of the two devices in Fig. 6. Device with T_{ch} of 2.2 nm has a threshold voltage (V_T) of -1.15 V exhibiting a high μ_{FE} of 106.9 $cm^2/V{\cdot}s$ while device with T_{ch} of 1.5 nm has a V_T of 0.02 V (enhancement-mode) with μ_{FE} of 90.7 $cm^2/V{\cdot}s$. These mobilities match well with LTPS p-FET for CMOS logic. Fig. 8 and Fig. 9 show the transfer and output characteristics of a short channel ALD In_2O_3 transistor with channel length (L_{ch}) of 0.1 μm, T_{ch} of 2.2 nm and with 5 nm HfO_2 as gate dielectrics. A high drive current over 2 mA/μm is achieved, also indicating a low contact resistance.

To fully utilize the high mobility property of ALD In_2O_3, ALD In_2O_3 n-FETs with 12 nm Al_2O_3 as gate dielectrics are used to match the voltage range with LTPS p-FET. Fig. 10 and Fig. 11 show the transfer and output characteristics of a typical LTPS p-FET in a vertically stacked M3D CMOS inverter with L_{ch} of 5 μm. Fig. 12 presents the μ_{FE} versus V_{GS} characteristics of the same device, exhibiting a high hole mobility of 96.9 $cm^2/V{\cdot}s$. Fig. 13 shows the transfer characteristics of a typical ALD In_2O_3 n-FET in the M3D CMOS inverter with L_{ch} of 10 μm. Fig. 14 presents the μ_{FE} versus V_{GS} characteristics of the same device, with an electron mobility of 23.8 $cm^2/V{\cdot}s$. μ_{FE} of ALD In_2O_3 in the M3D CMOS inverter is lower than that of ALD In_2O_3 transistors fabricated on the SiO_2/Si substrate, as shown in Fig. 7, most likely due to the surface roughness caused by the 3D integration process. But this μ_{FE} is still a record on n-FETs among CMOS devices and circuits using oxide semiconductor n-FET and LTPS p-FET, as discussed latter. Further process optimization on the 3D stack and fabrication process can further improve the electron mobility of ALD In_2O_3.

Fig. 15 shows the voltage transfer characteristics of an M3D CMOS inverter with ALD In_2O_3 n-FET with L_{ch} of 10 μm and LTPS p-FET with L_{ch} of 20 μm at V_{DD} from 2 V to 6 V, exhibiting a full swing on output from V_{DD} to zero. The midpoint voltage is tuned by threshold voltage engineering, based on thickness engineering and thermal engineering approaches as in ref. 3, to enhance the noise margin (NM). The inverter gain is presented in Fig. 16, where a high gain of 134.3 V/V is achieved, which is among the best reported values in CMOS inverters by oxide semiconductor n-FET and LTPS p-FET. Fig. 17 shows the NM of the same M3D CMOS inverter as in Fig. 15 at V_{DD} of 2 V. A high noise margin of 0.84 V at V_{DD} of 2 V is achieved. NM here is extracted by the largest possible square method, which is the largest noise margin reported normalized by V_{DD}. The high inverter voltage gain and large noise margin indicate high-performance CMOS logic is achieved by the M3D of ALD In_2O_3 n-FET and LTPS p-FET.

Fig. 18 and Fig. 19 present the V_{OUT} and V_{IN} versus time characteristics at V_{DD} of 4 V of M3D CMOS NAND/NOR logic gates by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET. Four combinations of input states '00', '01', '10', and '11', and corresponding output results are highlighted, demonstrating functional NAND/NOR operation with a full swing across zero to V_{DD}.

Table I summarizes the reported state-of-the-art CMOS devices and circuits by oxide semiconductor n-FET and p-FET with LTPS and SnO as channel materials. In this work, we use ALD In_2O_3 as n-FET channel to achieve the highest electron mobility in these CMOS devices. Meanwhile, we have demonstrated 3D vertically stacked CMOS logic gates such as inverter, NAND, NOR gates, using an M3D fabrication process, achieving largest noise margin (normalized by V_{DD}) and highest voltage gain among these devices.

IV. Conclusion

In conclusion, the monolithic 3D integration CMOS devices and circuits with vertically stacked top-gate LTPS p-FET and back-gate ALD In_2O_3 n-FET are demonstrated with a low thermal budget of 450 °C. High-performance CMOS logic gates with a high inverter gain > 134.3 V/V and a large noise margin of 0.84 V at V_{DD} of 2 V are achieved, enabled by the high-mobility ALD In_2O_3 as n-channel to balance the high hole mobility of LTPS. The above M3D integration process provides a promising route toward 3D CMOS logic and embedded memory applications.

Acknowledgments

The authors gratefully acknowledge funding support through the National Key R&D Program of China (Grant No. 2019YFA0706100), Innovation 2030 Program of China (Grant No. 2022ZD0210600), and the Multi-Glass Project (MPG) Platform from Tianma Microelectronics Co., Ltd. The work is also partly supported by SRC JUMP ASCENT Center and nCore IMPACT Center.

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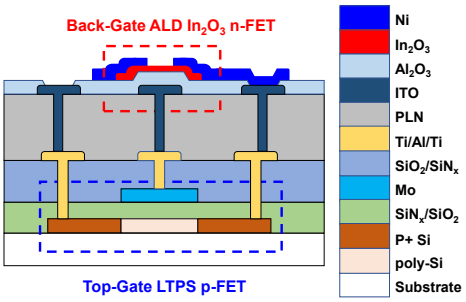

Fig. 1. Schematic diagram of a M3D CMOS inverter by ALD In_2O_3 n-FET and LTPS p-FET.

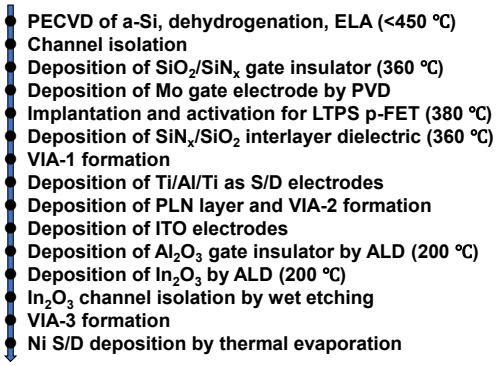

Fig. 2. Fabrication process flow of the M3D of vertically stacked ALD In_2O_3 n-FET and LTPS p-FET.

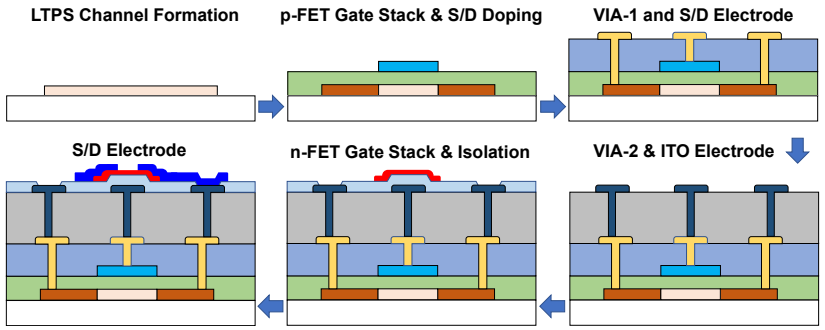

Fig. 3. Illustration of the M3D fabrication process of vertically stacked ALD In_2O_3 n-FET and LTPS p-FET.

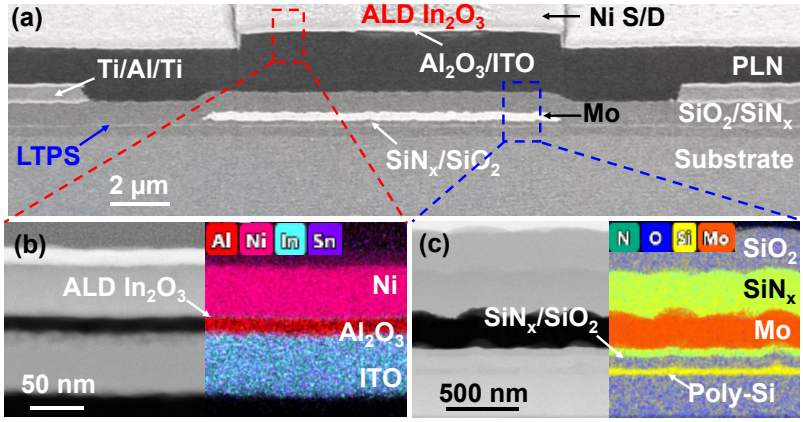

Fig. 4. (a) SEM cross-section image of a CMOS inverter by the M3D process using vertically stacked ALD In_2O_3 n-FET and LTPS p-FET. TEM and EDS cross-section images of gate stack of (b) ALD In_2O_3 n-FET and (c) LTPS p-FET.

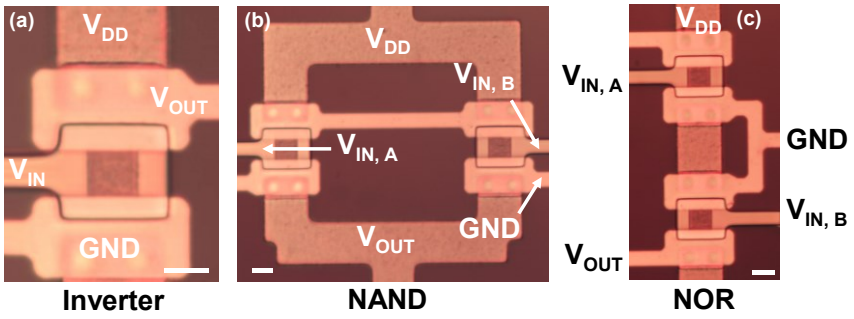

Fig. 5. Top-view photo image of (a) inverter, (b) NAND, and (c) NOR circuits fabricated using M3D process by stacked ALD In_2O_3 n-FETs and LTPS p-FETs. The scale bar in each figure is 10 μm. ALD In_2O_3 n-FETs (bottom) and LTPS p-FETs (top) are vertically stacked on top of each other similar to a CFET structure.

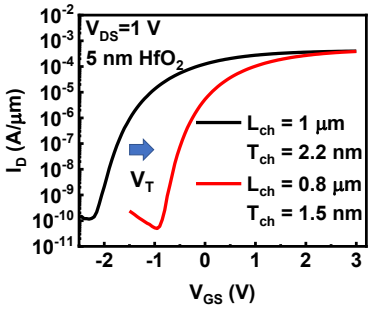

Fig. 6. Comparison of I_D-V_{GS} of back-gate ALD In_2O_3 n-FETs with different T_{ch} and with 5 nm HfO_2 as gate dielectrics fabricated on a SiO_2/Si substrate. The device fabrication process of was developed in our previous work [3].

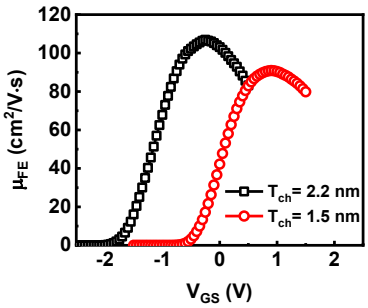

Fig. 7. μ_{FE}-V_{GS} at low V_{DS} of the same device as in Fig. 6.

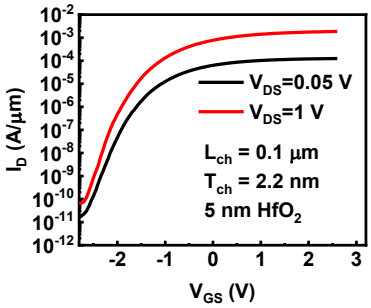

Fig. 8. I_D-V_{GS} of a back-gate ALD In_2O_3 n-FET with L_{ch} of 0.1 μm and T_{ch} of 2.2 nm, and with 5 nm HfO_2 as gate dielectrics fabricated on a SiO_2/Si substrate. The device fabrication process was developed in our previous work [3].

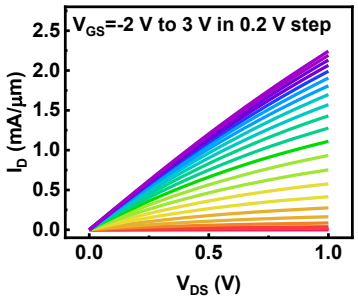

Fig. 9. I_D-V_{DS} of the same device as in Fig. 8. Maximum drain current > 2 mA/μm is achieved.

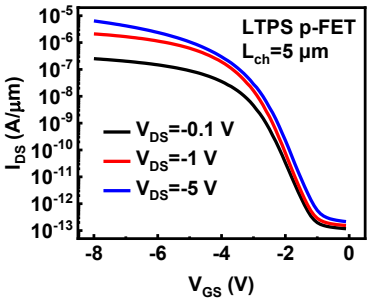

Fig. 10. I_D-V_{GS} of a representative top-gate LTPS p-FET with L_{ch} of 5 μm, in a M3D CMOS inverter by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET.

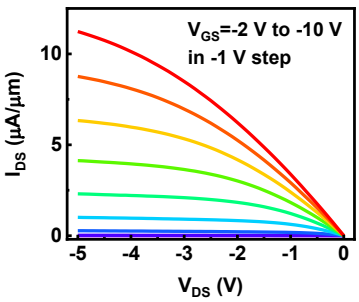

Fig. 11. I_D-V_{DS} of the same device as in Fig. 10.

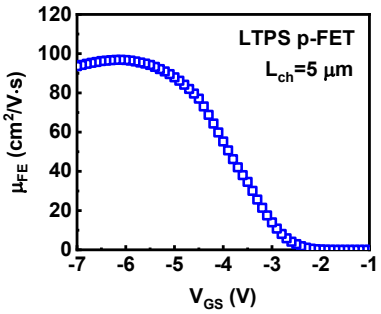

Fig. 12. μ_{FE}-V_{GS} at low V_{DS} of the same device as in Fig. 10.

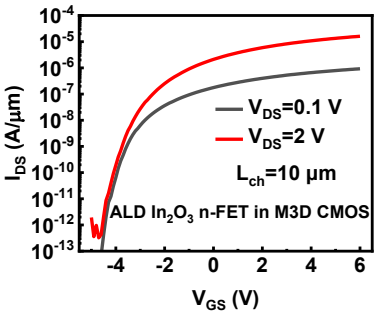

Fig. 13. I_D-V_{GS} of a representative back-gate ALD In_2O_3 n-FET with L_{ch} of 10 μm, in a M3D CMOS inverter by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET.

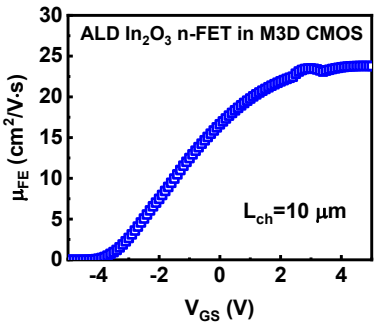

Fig. 14. μ_{FE}-V_{GS} at low V_{DS} of a back-gate ALD In_2O_3 n-FET with L_{ch} of 10 μm, in a M3D CMOS inverter by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET.

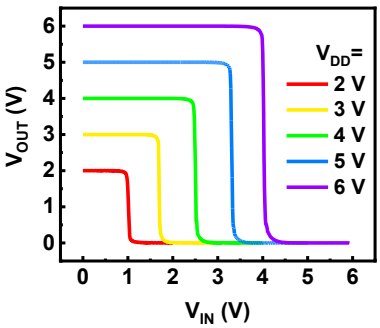

Fig. 15. V_{OUT} versus V_{IN} characteristics of a M3D CMOS inverter by vertically stacked ALD In_2O_3 n-FET (L_{ch}=10 μm) and LTPS p-FET (L_{ch}=20 μm).

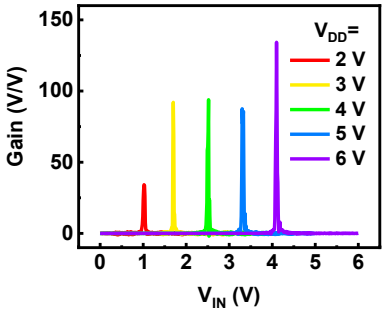

Fig. 16. Voltage gain of the same M3D CMOS inverter as in Fig. 15.

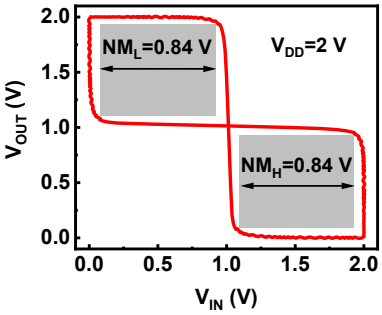

Fig. 17. Noise margin of the same M3D CMOS inverter as in Fig. 15 at V_{DD} of 2 V.

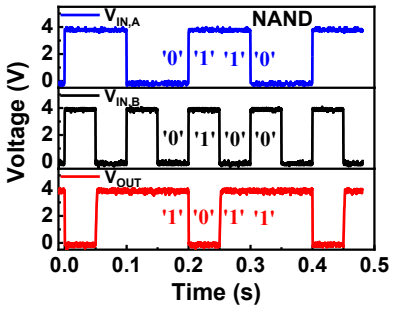

Fig. 18. V_{OUT} and V_{IN} versus time characteristics of a M3D CMOS NAND logic gate by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET, demonstrating the NAND logic.

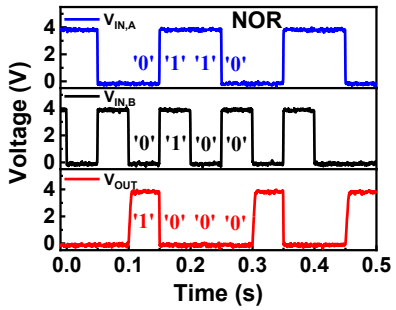

Fig. 19. V_{OUT} and V_{IN} versus time characteristics of a M3D CMOS NOR logic gate by vertically stacked ALD In_2O_3 n-FET and LTPS p-FET, demonstrating the NOR logic.

Table I. Comparison of State-of-the-Art 3D Stacked CMOS Technology by Bottom-Up Fabrication

		This work	[16]	[15]	[12]	[13]	[14]
n-FET		In_2O_3	IGZO	IGZO	IGZO	IGZO	IGZO
p-FET		Poly-Si	Poly-Si	Poly-Si	Poly-Si	Poly-Si	SnO
Channel Stacked		Y	Y	N	N	N	N
n-Channel Mobility (cm^2/V·s)		106.9 (n-FET only)/ 23.8 (M3D)	-	13.52	16.3	10.1	10.05
p-Channel Mobility (cm^2/V·s)		96.9	-	81.76	69.0	78.3	1.19
Gain (V/V)		134.3	18	114.28	-	68.3	112
Noise Margin	NM_H (V) / V_{DD} (V)	0.84 / 2	0.60* / 2	4.5 / 8	-	4.1 / 10	5.22 / 10
	NM_L (V) / V_{DD} (V)	0.84 / 2	0.62* / 2	2.8 / 8	-	4.5 / 10	3.54 / 10
n-Channel Process		ALD	Sputter	Sputter	Sputter	Sputter	Sputter
p-Channel Process		PECVD	PECVD	PECVD	PECVD	PECVD	Sputter

* NM here is calculated based on the voltage transfer curve from ref. [16]