Deep Sub-100 nm Ge CMOS Devices on Si with the Recessed S/D and Channel

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Abstract

We report on comprehensive studies of Ge CMOS devices with the recessed channel and S/D fabricated on a Ge-on-insulator (GeOI) substrate. Both nFETs and pFETs with channel lengths (L_{ch}) from 500 to 20 nm, channel thicknesses (T_{ch}) from 90 to 15 nm, EOTs from 5 to 3 nm, and gate stacks with and without the post oxidation (PO) are investigated. Benefiting from the fully depleted ultra-thin body (FD-UTB) channel with a reasonable interface, a low sub-threshold slope (SS) of 95 mV/dec is obtained in a 60 nm L_{ch} nFET and a record high I_{ON}/I_{OFF} ratio of 10^6 is realized in a 300 nm L_{ch} nFET. The recessed contact strongly dependents on the recessed depth and optimized recessed depth significantly improves the Ge contacts.

Introduction

Ge is considered as a promising channel material in the post Si CMOS era, due to its higher and near symmetrical carrier mobilities for both electrons and holes, large density of states, and Si-compatible low temperature process. Recently, many important progresses have been achieved [1-7]. In our previous report [8], a novel recessed channel and S/D technique is used to improve the Ge n-contact and the gate electrostatic control. In this paper, we carried out a comprehensive study of the device performance dependence on $L_{ch,}$ $T_{ch,}$ EOT and the interface passivation of both nFETs and pFETs with the recessed channel and S/D. The post oxidation process improves the $Al_2O_3/GeO_x/Ge$ interface. Determined by ion implantation profiles, the characteristics of nFETs are much more sensitive to T_{ch} than those of pFETs. To better understand the temperature-dependent device OFF- and ON-state characteristics, the OFF-state band-to-band-tunneling (BTBT) generation rate and the ON-state injection velocity are simulated by TCAD.

Experiment

Fig. 1 shows the experiment process flows for both Ge nFETs and pFETs. The device cross section at each main step is given in Fig. 2 and a brief summary on experimental splits is also included. The near-Gaussian distribution of the implanted ions in the Ge is plotted as the color-map shown in the cross section.

The starting material is a GeOI wafer with 180 nm lightly Sb-doped (100) Ge and 400 nm SiO_2 on (100) Si from Soitec (**step 1** in Fig. 2). An over-etched testing recess channel structure is given in Fig. 3, showing the layers of the substrate. The pFETs and nFETs were fabricated in parallel for better comparison. After cleaning and mesa isolation using SF_6 based inductively coupled plasma (ICP) dry etching, ion implantation (**step 2** in Fig. 2) was carried out for nFETs and pFETs using P and BF_2 respectively, which were then separately activated by rapid thermal anneal (RTA) in different conditions. Then, the channel was formed by a SF_6 ICP dry etching (**step 3** in Fig. 2). For the recessed channels, depending on the etching time, T_{ch} of 15, 25, 60 and 90 nm are realized, as shown in Fig. 3 (b-d). Next, the samples were cyclically rinsed in 2% HF for 3 times as the surface wet clean. For the gate dielectrics, three conditions: 5 nm Al_2O_3 gate dielectric with the Ge post oxidation (PO) (*condition I*, EOT = 3 nm), 8 nm Al_2O_3 gate dielectric with the Ge PO (*condition II*, EOT = 4.5 nm) and 8 nm Al_2O_3 gate dielectric without the Ge PO (*condition III*, EOT = 5 nm), are studied. After the gate dielectric formation, the oxide in the S/D was first etched away and then a BCl_3/Ar ICP dry etching was conducted to partially remove the top doped Ge layer as the recessed S/D etch. The etch rate is calibrated to be 15 nm/min. Determined by etching time, different recess depths were studied to optimize the quality of metal contacts on Ge, as shown in Fig. 4(a-b). Next, 100 nm Ni was deposited as the metal contacts for both nFETs and pFETs (**step 4** in Fig. 2), followed by an Ohmic annealing by RTA. Finally, the gate metal was defined by 40/60 nm Ti/Au for the pFETs and 40/60 nm Ni/Au for the nFETs (**step 5** in Fig. 2). All of the split conditions are applied to both nFETs and pFETs.

Results and Discussion

Fig 4(c) shows the n-Ge TLM results with varying recess etching time (recess depths). The inserted figure depicts the contact resistance (R_c) versus the etching time, demonstrating that R_c first decreases and then increases quickly with the etching time (recess depth). This is resulted from the near-Gaussian distribution profile of doping ions: with extended etching time, the doping concentration at the newly formed surface first increases and then decreases rapidly, hence, there is an optimized recess etching time or depth for low-resistivity Ohmic contacts on ion-implanted Ge. Fig. 5(a) shows the best TLM results, where the low R_c of 0.32 and 0.15 Ω·mm and sheet resistance (R_{sh}) of 80 and 140 Ω/□ are achieved on n- and p-type Ge contacts, respectively. The difference of R_{sh} between n- and p-type contacts is mainly attributed to the difference of mobility between holes and electrons in Ge. Fig. 5(b-c) provide the ON-resistance (R_{ON}) versus L_{ch} of pFETs and nFETs in *condition III* at $|V_{gs}-V_{TH}| = 2$ V, $|V_{ds}| = 0.05$ V at different temperatures. The source/drain series resistance (R_{sd}) is extracted to be 0.7 and 1.1 Ω·mm for nFETs and pFETs. Although the R_c of p-type Ge contact is smaller than that of n-type Ge contact, R_{sd} of pFETs is larger than that of nFETs because of a factor of 2 larger R_{sh}. The R_{sd} shows negligible dependence on temperature, indicating the dominance of the tunneling current in the Ohmic contacts.

Fig. 6(a) provides the titled SEM image of a fabricated device. The device gate area is enlarged in Fig. 6(b). The recessed channel can be clearly seen in the testing device without the gate metal in Fig. 6(c). Fig. 7(a) shows the transfer curves of a 400 nm L_{ch} pFET in *condition III* at V_{gs} from 1 V to -3V and V_{ds} = -0.05, -0.5 and -1 V. The device has a reasonable SS of 151 mV/dec and a high I_{ON}/I_{OFF} ratio of 5×10^5, both at V_{ds} = -0.5 V. The g_m-V_{gs} curves of the same device are given in Fig. 7(b). For comparison, a 300 nm L_{ch} nFET in the same condition is given in Fig. 8, showing a decent SS of 139 mV/dec and a record high I_{ON}/I_{OFF} ratio of 10^6,

both at V_{ds} = 0.5 V. By further improving the MOS interface using the PO technique, SS as low as 95 mV/dec is achieved in a 60 nm L_{ch} nFET in *condition II* at V_{ds} = 0.05 V as shown in Fig. 9(a). SS could to be further reduced by EOT scaling and interface optimization. The g_m-V_{gs} curves of the same device are given in Fig. 9(b). Fig. 9(c) provides the output characteristics of the same device with V_{ds} from 0 V to 1.5 V and V_{gs} from -1 V to 1.5 V in 0.2 V steps.

Fig. 10 provides the V_{TH} scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III*. The V_{TH} roll-off resulted from the short channel effects (SCEs) is suppressed in thinner channel devices due to better gate electrostatic control of the channels. Compared with devices in *condition III* with a larger EOT and no PO, devices in *condition I* show slightly better SCE immunity. Figs. 11-12 provide the drain current (I_d) and maximum trans-conductance (g_{max}) scaling metrics of the same set of nFETs in Fig. 10 at V_{ds} = 0.5 and 1 V. Better interface after the PO process and smaller EOT provide better ON-state performance. However, smaller T_{ch} greatly reduces I_d and g_{max}, mainly due to the degraded electron mobility [9] and reduced cross-sectional area of current conduction. Fig. 13 shows the SS scaling metrics of the same set of nFETs in Fig. 10. SS increases with decreasing L_{ch}. Smaller T_{ch} and EOT and better interface offer better SS. The I_{ON}/I_{OFF} ratio scaling metrics at V_{ds} = 0.5 V in Fig. 14 show the similar trend as SS due to the SCEs.

Fig. 15(a-b) give the transfer curves of pFETs and nFETs with the same L_{ch} of 500 nm but different T_{ch} of 25, 60 and 90 nm, respectively. The nFETs are much more sensitive to T_{ch} than pFETs, as proved by the fast degradation in I_{ON}/I_{OFF} ratio with increasing $T_{ch.}$ This is could be due to that the doping profile is different for n and p Ge ion implantation: the P ion is much more diffusive than BF_2 in Ge [10] and it has a much larger density gradient than that of BF_2 ions [11] in the channel region. The concentration of P ions decreases much faster than BF_2 ions in Ge, resulting in a worse gate control in nFETs than pFETs when T_{ch} increases. Figs. 16-17 show the g_m-V_{gs} and output curves of the same set of devices in Fig. 15. On the condition of same T_{ch} and L_{ch}, nFETs shows better ON-state performance because of a larger electron mobility than hole mobility. For pFETs, the 90 nm T_{ch} device has the largest g_{max} of 100 mS/mm at V_{ds} = -1 V. However, for nFETs, the g_{max} of the 90 nm T_{ch} is smaller than that of the 60 nm T_{ch} device which has a g_{max} of 230 mS/mm at V_{ds} = 1 V. This can be partly explained by 1) larger OFF-state leakage in thicker channel 2) the fact that the P ion concentration in the upper part of the 90 nm T_{ch} channel is much higher than that of the 60 nm T_{ch} channel and more Coulomb scattering lowers electron mobility.

Fig. 18 provides the V_{TH} scaling metrics of pFETs with T_{ch} of 25, 60 and 90 nm in *condition I* and T_{ch} of 25 nm in *condition III*, showing a similar trend as nFETs. The more negative V_{TH} of the pFETs in *condition III* could be due to more fixed charge in the Ge-oxide without the PO process. Fig. 19-20 show the I_d and g_{max} scaling metrics of the same set of pFETs in Fig. 18 at V_{ds} = -1 V. The I_d and g_{max} increase with decreasing L_{ch} as expected. Moreover, their relationship with T_{ch} show similar behaviors as in the nFETs shown in Figs. 11-12 because of the dependence of mobility on T_{ch}. Better interface quality by the post oxidation is confirmed by the improved I_d and g_{max} of the devices in *condition I* compared with the devices in *condition III* with the same T_{ch} of 25 nm. Fig. 21 shows the SS versus L_{ch} relationships of the same set of pFETs in Fig. 18. SS increases with lower L_{ch} and better immunity from SCEs are obtained with reduced T_{ch} and EOT, and higher interface quality. The I_{ON}/I_{OFF} ratio scaling metrics of the same set of pFETs are given in Fig. 22, showing similar trend like that of SS. The I_{ON} increase accounts for the ratio increase when L_{ch} > 150 nm and the I_{OFF} increase accounts for the ratio decrease when L_{ch} < 150 nm.

Figs. 23-24 show the transfer curves of a 50 nm L_{ch} pFET and a 60 nm L_{ch} nFET in *condition III* at temperatures from 300 K to 400 K at $|V_{ds}|$ = 0.5 and 1 V, respectively. The I_{OFF} and SS increases at higher temperatures because of the temperature dependence of the diffusion current in OFF-state and sub-threshold region. Since the change of contact resistance at different temperatures is negligible as proved in Fig. 5, the reduced I_{ON} with the increase of temperature indicates the phonon scattering dominance in carrier motilities at room temperature.

All the error bars in the scaling metrics plots are based on the measurements over average 20 devices at each data point, indicating good device uniformity.

To better understand the device behavior, TCAD simulation is carried out on the recessed channel Ge nFET by Sentaurus. Fig. 25(a-b) shows the simulated electron density in a 50 nm L_{ch} and 15 nm T_{ch} nFET in the OFF and ON-state at V_{ds} = 0.5 V, respectively. The black lines in Fig. 25(a) mark the boundary of the depletion region with a full-depleted channel. In the ON-state, a layer with high density accumulation carriers is formed close to the interface between Ge and oxide, as shown in the inserted figure in Fig. 25(b). Fig. 26(a-c) show the BTBT generation rate in the same simulated device with different gate biases at 300 K, explaining the GIDL in the OFF-state. With increasing negative gate bias, the electrical field from drain to channel raises, increasing the band-bending, thus, the BTBT current becomes larger. Fig. 26(d) depicts simulated band-diagram of Ge along the BTBT current path marked by the dashed arrow in Fig. 26(c). Fig. 26(e-f) describe the electron velocity near the source side in device ON-state with different temperatures of 200, 300 and 400 K, showing much larger injection velocity at lower temperatures. Fig. 26(g) provides the simulated I_d-V_{gs} at different temperatures, in consistent with the results in Figs. 23-24.

Conclusion

We present comprehensive studies of the Ge nFETs and pFETs with the recessed channel and S/D on GeOI, fabricated for Ge CMOS applications. With further EOT scaling and interface optimization, the device process developed here is promising for ultimate low-power high-speed CMOS beyond Si.

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Reference

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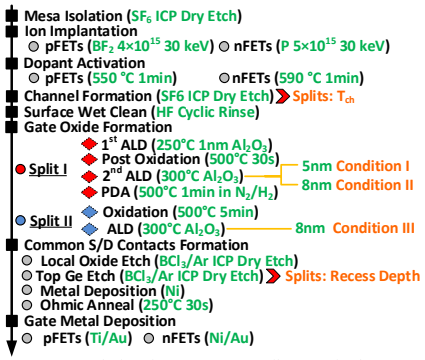


Fig. 1 Fabrication process flow of the Ge recessed channel and S/D MOSFETs. Different gate stacks / T_{ch} / recess depths are studied.

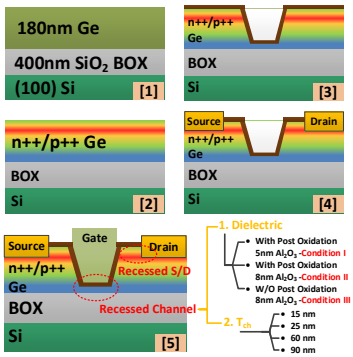


Fig. 2 Device cross sections at different fabrication steps. Experiment splits of gate dielectric and T_{ch} are listed.

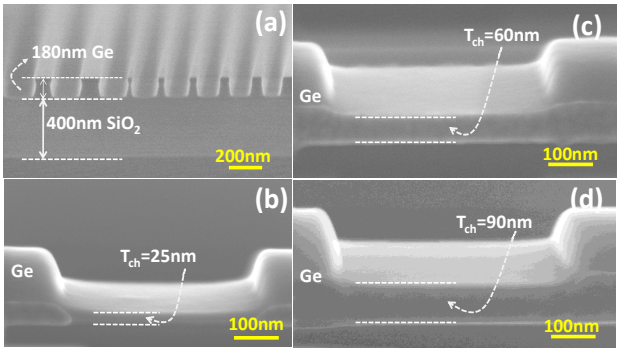
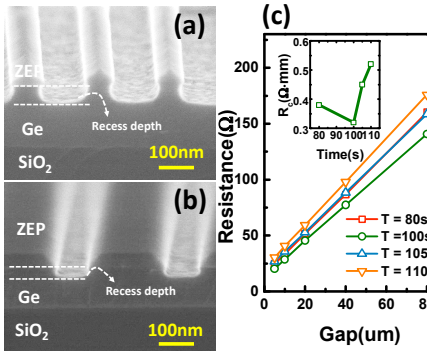


Fig. 3 (a) Cross section of testing recessed channel. A substrate with 180 nm Ge on 400 nm SiO_2 was used. (b-d) Cross sections of recessed channels with T_{ch} of 25, 60 and 90 nm, respectively.



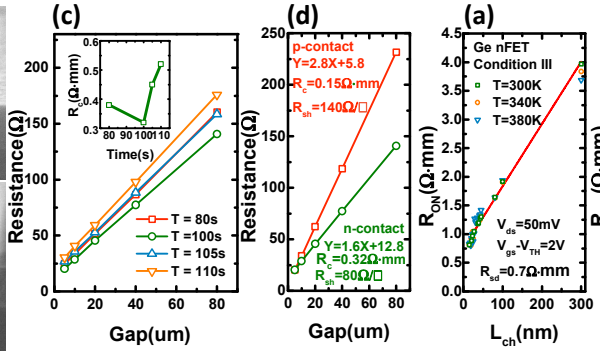


Fig. 4 (a-b) Testing recessed S/D structures with different recess depths. (c) TLM results of recessed contacts on n-Ge with different recess depths (etching time). The inserted figure shows the dependence of R_c on the etching time. (d) Best TLM results on n and p type contacts.

Fig. 5 On-resistance dependence on L_{ch} of nFETs (a) and pFETs (b) in *condition III* at different temperatures. The R_{sd} is extracted.

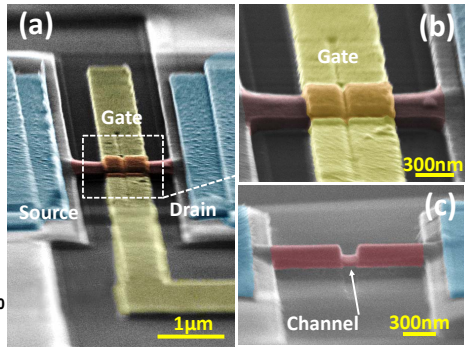


Fig. 6 (a) Tilted view of a fabricated device. (b) Zoom-in image of the gate area of the device in (a). (c) Tilted view of a testing device without the gate metal. The recessed channel can be clearly observed.

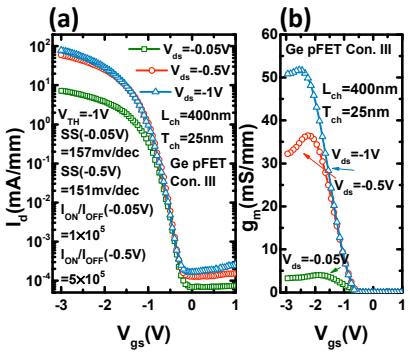


Fig. 7 I_d-V_{gs} curves of a 400 nm L_{ch} pFET in *condition III* with a high I_{ON}/I_{OFF}. (b) The g_m-V_{gs} curves of the device in (a).

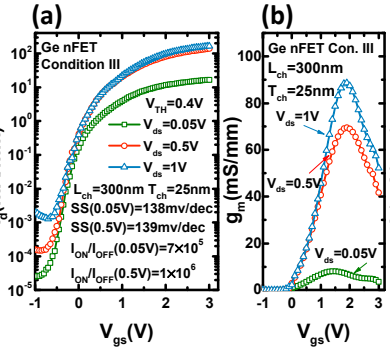


Fig. 8 I_d-V_{gs} curves of a 300 nm L_{ch} nFET in *condition III* with a record high I_{ON}/I_{OFF}. (b) The g_m-V_{gs} curves of the device in (a).

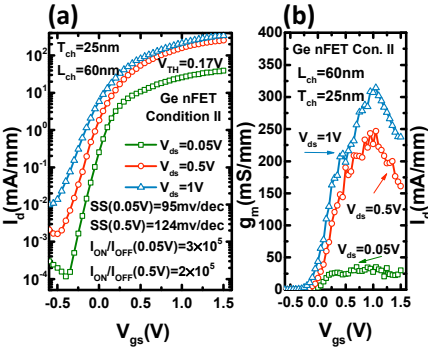


Fig. 9 (a) I_d-V_{gs} curves of a 60 nm L_{ch} nFETs in *condition II*. A low SS of 95 mV/dec is obtained. (b) The g_m vs. V_{gs} relationship of the same device in (a). (c) Output curves of the same device in (a).

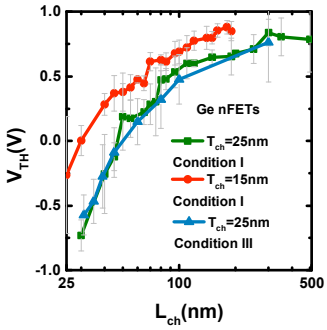


Fig. 10 V_{TH} scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III*.

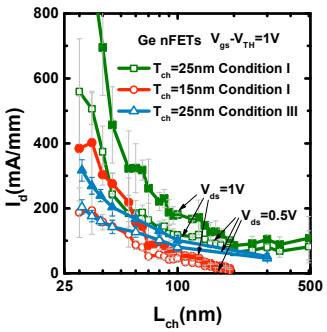


Fig. 11 I_d scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{gs} -V_{TH} = 1 V and V_{ds} of 0.5 and 1 V.

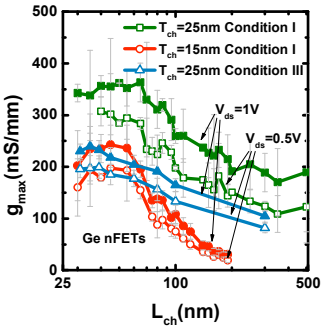


Fig. 12 g_{max} scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of 0.5 and 1 V.

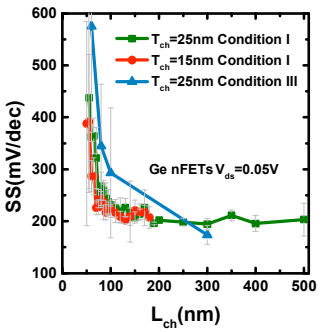


Fig. 13 SS scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of 0.05 V.

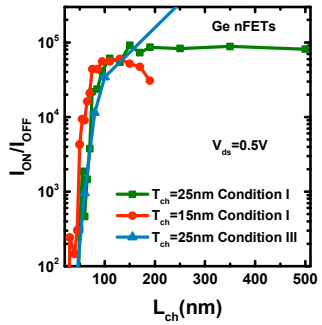


Fig. 14 I_{ON}/I_{OFF} ratio scaling metrics of nFETs with T_{ch} of 15/25 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of 0.5 V.

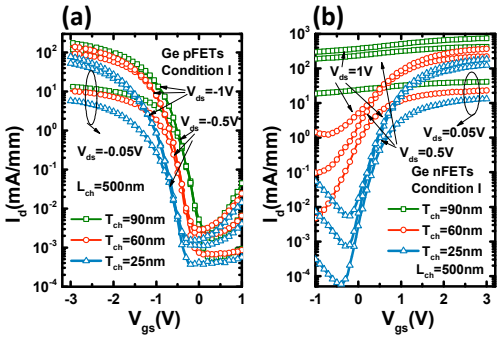


Fig. 15 (a) Transfer curves of pFETs with T_{ch} of 25, 60 and 90 nm in *condition I*. (b) Transfer curves of nFETs with T_{ch} of 25, 60 and 90 nm in *condition I*.

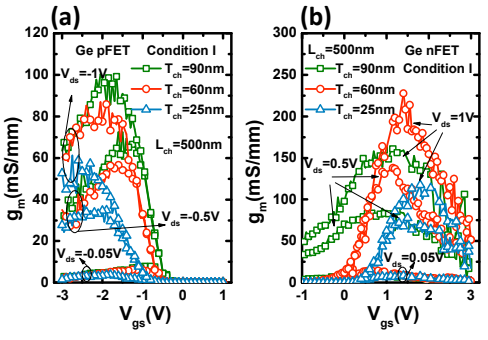


Fig. 16 (a) g_m v.s. V_{gs} curves of pFETs with T_{ch} of 25, 60 and 90 nm in *condition I*. (b) g_m v.s. V_{gs} curves of nFETs with T_{ch} of 25, 60 and 90 nm in *condition I*.

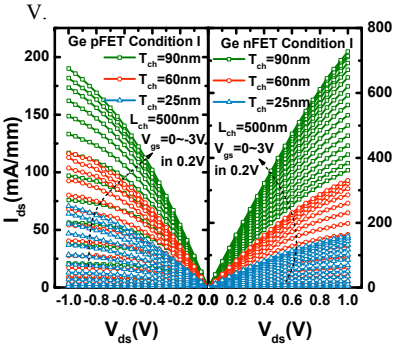


Fig. 17 left: Output curves of the same 3 pFETs in Fig. 15(a). Right: Output curves of the same 3 nFETs in Fig. 15(b).

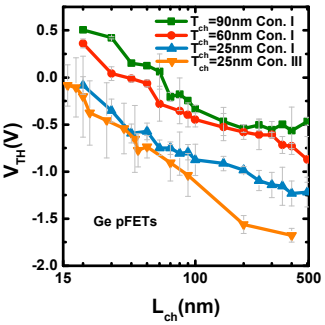


Fig. 18 V_{TH} scaling metrics of pFETs with T_{ch} of 25/60/90 nm in *condition I* and T_{ch} of 25 nm in *condition III*.

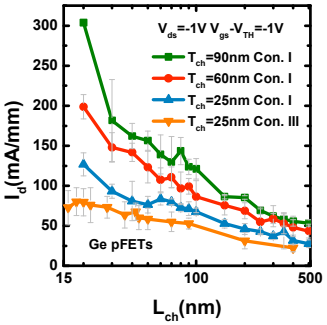


Fig. 19 I_d scaling metrics of pFETs with T_{ch} of 25/60/90 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{gs} -V_{TH} = -1 V and V_{ds} of -1 V.

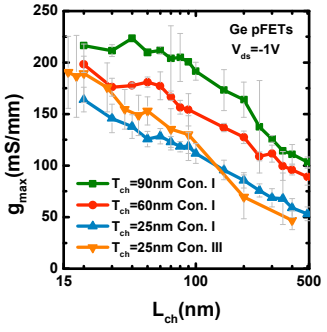


Fig. 20 g_{max} scaling metrics of pFETs with T_{ch} of 25/60/90 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of -1 V.

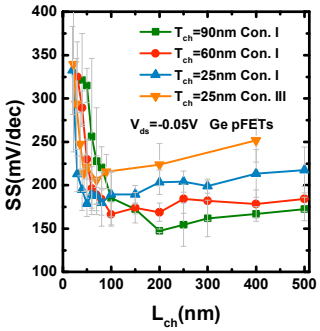


Fig. 21 SS scaling metrics of pFETs with T_{ch} of 25/60/90 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of -0.05 V.

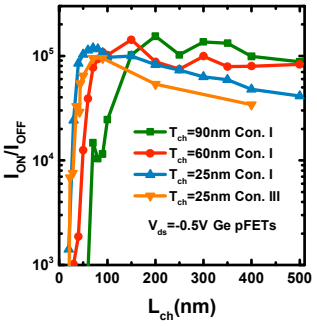


Fig. 22 I_{ON}/I_{OFF} ratio scaling metrics of pFETs with T_{ch} of 25/60/90 nm in *condition I* and T_{ch} of 25 nm in *condition III* at V_{ds} of -0.5 V.

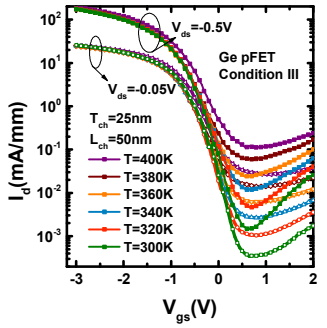


Fig. 23 Transfer curves of a 50 nm L_{ch} pFET in *condition III* at different temperatures from 300 to 400 K.

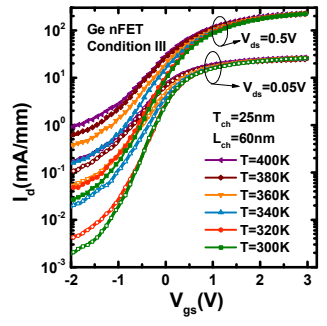


Fig. 24 Transfer curves of a 60 nm L_{ch} nFET in *condition III* at different temperatures from 300 to 400 K.

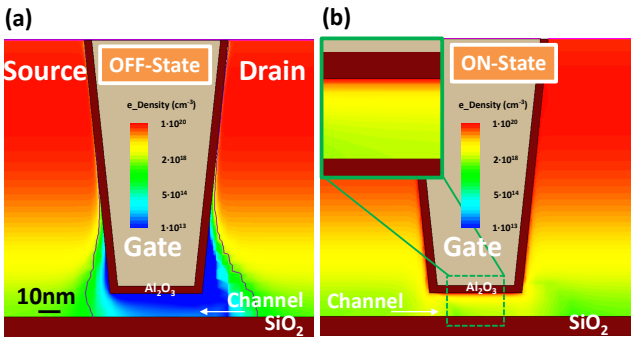


Fig. 25 (a) OFF-state simulation result of electron distribution of a 50nm L_{ch} recessed channel nFET by TCAD. The black lines mark the boundary of the depletion region. (b) ON-state simulation result of electron density of the device in (a). Inserted figure shows the enlarged channel area.

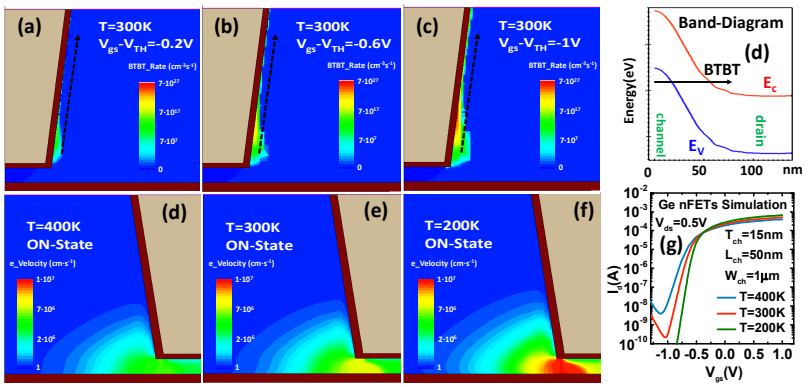


Fig. 26. (a-c) OFF-state BTBT generation rate ($cm^{-3}s^{-1}$) contours of the device in Fig. 25 with V_{gs}-V_{TH} = -0.2, -0.6 and -1 V at 300 K. (d) Simulated band-Structure along the tunneling path marked by the dashed arrow in (c). (d-f) ON-state electron velocity ($cm{\cdot}s^{-1}$) contours of the same device at T of 400, 300 and 200 K. (f) Simulated transfer curves at different temperatures.