InGaAs 3D MOSFETs with Drastically Different Shapes Formed by Anisotropic Wet Etching

J. Zhang,[1] M. Si,[1] X. B. Lou,[2] W. Wu,[1] R. G. Gordon,[2] and P. D. Ye[1]

[1] School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.
[2] Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.
Tel: 1-765-494-7611, Fax: 1-765-496-7443, E-mail: yep@purdue.edu

Abstract

In this work, we report on a 3D device fabrication technology achieved by applying a novel anisotropic wet etching method. By aligning channel structures along different crystal orientations, high performance 3D InGaAs devices with different channel shapes such as fins, nanowires and waves have been demonstrated. With further optimizing off-state leakage path by barrier engineering, a record high I_{ON}/I_{OFF} over 10^8 and minimum I_{OFF}~3pA/μm have been obtained from InGaAs FinFET device. Scaling metrics for InGaAs GAA MOSFETs and FinFETs are systematically studied with L_{ch} from 800 nm down to 50 nm and W_{Fin}/W_{NW} from 100 nm down to 20 nm which shows an excellent immunity to short channel effects.

Introduction

InGaAs 3D MOSFETs such as FinFETs and gate-all-around (GAA) MOSFETs have been demonstrated to offer large drive current and excellent immunity to short channel effects (SCEs) down to deep sub-100 nm channel length [1-23]. Although on-state performance of In(Ga)As MOSFETs are comparable or even higher to Silicon MOSFETs, In(Ga)As MOSFET technology is still not ready for high-speed low-power applications because of its high off-state leakage current (I_{OFF}) [18]. Meanwhile, InGaAs dry etching FinFETs suffer from a large fin bottom which prevents the further scaling of InGaAs FinFETs [5-8]. In this work, we *(i) report on a novel anisotropic wet etching based process technology for 3D InGaAs MOSFETs fabrication by simply aligning the structures along different crystal orientations to realize drastically different 3D devices including FinFETs with nearly vertical sidewalls, (ii) demonstrate InGaAs FinFETs with record I_{ON}/I_{OFF} over 10^8 and minimum I_{OFF}~3pA/μm through barrier engineering on off-state leakage path, (iii) systematically studied the scaling metrics and device performance of these 3D devices with three differently shaped channels down to 50 nm channel length (L_{ch}).*

Experiments

Figs. 1-3 show (a) the schematic diagram and (b) cross-sectional view of three different 3D InGaAs MOSFETs fabricated based on a simple wet etching process just with the fin or wire along three different crystal orientations. The 3D structure changes dramatically from inverted triangle nanowire to atomic shape waveform, and even nearly perfect vertical fin. The device fabrication process flow is shown in Fig. 4. The InGaAs devices are fabricated on two substrates with different doping level as shown in Fig. 5. The InAlAs and InGaAs layers were epitaxially grown on P++ (100) InP substrates as starting material. The crystal orientation of the substrates is EJ standard, as shown in Fig. 6(a). After solvent clean and $(NH_4)_2S$ pretreatment, 10 nm Al_2O_3 was grown by ALD as an encapsulation layer. Source/drain Si implantation was then performed at 20KeV with a dose of $1\times10^{14}/cm^2$. After dopant activation at 600°C for 15s in N_2, the 10 nm Al_2O_3 was removed by buffered oxide etch (BOE). Then, 10 nm Titanium (Ti) was deposited as wet etching mask and followed by a lift-off process. Then, a citric acid and H_2O_2 based wet etching (citric acid/H_2O_2/H_2O=15 g/10 ml/70 ml) was performed. The direction of patterned Ti mask is critical, and pattern angle "α" is defined in Fig. 6(a) and 6(b). Fig. 6(b) illustrates how Ti mask was patterned on the substrate surface. In this work, the effect of α is studied. It is found if α=0°, InGaAs nanowire with inverted triangle shape is obtained. If α=90°, triangle shape InGaAs waveform structure is obtained. More interestingly, in between a triangle and an inverted triangle, InGaAs fin structure with nearly vertical sidewalls on top is achieved if α=45°. A perfect vertical fin structure is a challenge to realize by dry etching technique in III-V as shown in Fig.9(c) and Ref.[6]. Surprisingly, it can be realized in such a simple wet etching process by fully using the anisotropic properties of III-V. The detailed etching results are shown in Figs. 7-9 and will be discussed further in this paper. After the removal of Ti mask by BOE and 10min $(NH_4)_2S$ passivation, 10 nm Al_2O_3 was grown by ALD as gate dielectric. ALD Tungsten Nitride (WN) was grown in-situ after Al_2O_3 as gate metal. Then, Ni/Au was deposited to define the gate and it also served as etching mask for WN. After WN etching process, Au/Ge/Ni Ohmic contacts were formed and followed by a RTA at 350°C in N_2 for 15s. Pt/Ti/Au body contact and Ni/Au test pads were deposited as the final process. All devices discussed in the following part are on substrate A unless otherwise specified.

Results and Discussion

Figs. 7-9 show the SEM images of the anisotropic wet etching process in this work. If Ti mask is patterned with α=0°, the InGaAs cross-section is an inverted triangle, as shown in Fig. 7(a), because the wet etching in III-V is anisotropic. If the performed wet etching time is long enough, the inverted

triangle shape InGaAs can be suspended and the nanowire is realized as shown in Fig. 7(b). The top view of fabricated InGaAs nanowires by the anisotropic wet etching, having nanowire width (W_{NW}) as thin as 10 nm and nanowire length (L_{NW}) as long as 1 μm, is illustrated in Fig.7(c). If Ti mask is patterned with $\alpha=90^o$, the InGaAs cross-section is a triangle, as shown in Fig. 8(a) and (b). The top view of a fabricated InGaAs waveform structure is shown in Fig. 8(c). By combining the triangle and inverted triangle to choose in between $\alpha=45^o$, the InGaAs fin structure with nearly vertical sidewalls on top is obtained, as shown in Fig. 9(a). This wet etching process can be applied to fabricate FinFET with W_{Fin} down to sub-10 nm, as shown in Fig. 9(b), and with fin height up to several hundred nanometers. Compared to InGaAs fins fabricated by Cl-based dry etching (Fig. 9(c)), the wet etched fins are almost vertical and ideal. Figs. 10-11 show a typical transfer and output characteristics of an L_{ch}=50 nm, W_{Fin}=20 nm and H_{Fin}=50 nm FinFET. This device shows normalized on-current ($I_{ON/N}$) of 104 μA/μm at V_{gs}-V_T=0.5 V and V_{ds}=0.5 V, transconductance (g_m) of 386 μS/μm, subthreshold swing (SS) of 143 mV/dec at V_{ds}=0.5 V, drain induced barrier lowering (DIBL) of 40 mV/V and threshold voltage (V_T) of -0.18 V from linear extrapolation at V_{ds}=0.05 V. Due to the junction leakage current, the source current (I_s) is used to obtain the intrinsic current in the channel. Figs. 12-13 show a typical transfer and output characteristics of an L_{ch}=50 nm, W_{NW}=30 nm InGaAs GAA MOSFET. This device shows $I_{ON/N}$ of 48 μA/μm at V_{gs}-V_T=0.5 V and V_{ds}=0.5 V, g_m of 160 μS/μm, SS of 154 mV/dec at V_{ds}=0.5 V, DIBL of 27 mV/V and V_T of 0.0 V. Fig. 14 shows a typical transfer characteristics of a L_{ch}=100 nm InGaAs WaveFET [24]. This device shows $I_{ON/N}$ of 167 μA/μm at V_{gs}-V_T=0.5 V and V_{ds}=0.5 V, g_m of 374 μS/μm, SS of 314 mV/dec at V_{ds}=0.5 V, DIBL of 214 mV/V and V_T of -1.0 V. The relatively negative V_T, large SS and DIBL of an InGaAs WaveFET is because it has a wide fin bottom. GAA and FinFET structures have better immunity to SCEs over WaveFETs. Fig. 15 shows the H_{Fin} extraction using InGaAs FinFETs with various W_{Fin}. As on current (I_{ON}) = $I_{ON/N}\times(W_{Fin}+2H_{Fin})$, with I_{ON} at V_{DD}=0.5V at various W_{Fin}, $I_{ON/N}$ and H_{Fin} can be extracted from the slope and intersection. $I_{ON/N}$ for L_{ch}=100 nm devices is extracted as 130 μA/μm and effective H_{Fin} is estimated as 50 nm. Figs. 16-17 show the W_{Fin} dependence of SS (V_{ds}=0.5V) and DIBL and at various L_{ch} on InGaAs FinFETs. The InGaAs FinFETs formed by wet etching technique show excellent immunity to SCEs with W_{Fin} less than 40nm down to L_{ch}=50 nm, demonstrating the advantage of forming nearly vertical fin structures versus triangle shape waveform structures. Figs. 18-20 show SS (V_{ds}=0.5V), DIBL and V_T roll off scaling metrics for InGaAs FinFETs and GAA MOSFETs with inverted triangle structures at L_{ch} from 800 nm down to 50 nm. Both InGaAs FinFETs and GAA MOSFETs demonstrate good immunity to SCEs with scaled W_{Fin} or W_{NW}. As the 3D InGaAs devices were fabricated on bulk InGaAs, body contact can be formed directly on InGaAs layers. Fig. 21 shows the transfer characteristics versus body voltage (V_B) where a clear V_B modulation can be observed, suggesting body contact is effective and can be used for charge pumping measurements. Fig. 22 shows a well-behaved device with a record I_{ON}/I_{OFF} exceeding 10^8 and I_{OFF}~3pA/μm at L_{ch}=200 nm fabricated on substrate A. This high I_{ON}/I_{OFF} is achieved through barrier engineering of the InGaAs devices. Fig. 23 summaries the band diagrams for leakage paths on InGaAs devices fabricated in this work. If InGaAs FinFETs are fabricated on substrate A, electrons go through n++ source region, $1\times10^{17}/cm^3$ p-doped region and $4\times10^{17}/cm^3$ p-doped region for off-state leakage, called leakage path A. If InGaAs FinFETs are fabricated on substrate B, electrons go through n++ source region, $4\times10^{17}/cm^3$ p-doped region and $1\times10^{18}/cm^3$ p-doped region, called leakage path B. If InGaAs devices are fabricated on substrate A without mesa isolation, electrons go through n++ source region, $1\times10^{17}/cm^3$ p-doped region, called leakage path C. Fig. 24 shows the I_{ON}/I_{OFF} comparison among devices with leakage paths A, B and C. Leakage path A shows the best I_{ON}/I_{OFF} because A has less BTBT than B and a larger barrier than C.

Conclusion

InGaAs GAA MOSFETs, FinFETs with nearly vertical sidewall, WaveFETs are demonstrated through a novel anisotropic wet etching process. InGaAs FinFETs and GAA MOSFETs are systematically studied with L_{ch} from 800 nm down to 50nm and W_{Fin} or W_{NW} from 100 nm down to 20 nm, showing excellent immunity to SCEs. InGaAs FinFETs with record I_{ON}/I_{OFF} over 10^8 and minimum I_{OFF}~3pA/μm are achieved through barrier engineering on off-state leakage path.

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Reference

[1] J. A. del Alamo, *Nature* 2011, p. 317. [2] J. J. Gu et al., *IEDM* 2012, p. 633. [3] M. Si et al., *APL* 2013, p. 093505. [4] M. Radosavljevic et al., *IEDM* 2009, p. 319. [5] M. Radosavljevic et al., *IEDM* 2011, p. 765. [6] Y. Q. Wu, *IEDM* 2009, p. 323 [7] V. T. Arun et al., *VLSIT* 2014, p. 72. [8] T. W. Kim et al., *IEEE EDL* 2015, p. 223. [9] C. B. Zota et al., *IEEE EDL* 2014, p. 342. [10] N. Waldron et al., *IEEE EDL* 2014, p. 1097. [11] T. Maeda, et al., *VLSIT* 2011, p. 62. [12] K. Tomioka, et al., *IEDM* 2011, p. 773. [13] L. Czornomaz, et al., *IEDM* 2012, p. 517. [14] Y. Sun, et al., *IEDM* 2014, p. 582. [15] A. Alian et al., *IEDM* 2013, p. 437. [16] J. Lin, et al., *IEDM* 2012, p. 757. [17] J. Lin, et al., *IEEE EDL* 2014, p. 440. [18] C. Y. Huang, et al., *IEDM* 2014, p. 586. [19] A. Ali, et al., *IEDM* 2010, p. 134. [20] T. W. Kim, et al., *IEDM* 2012, p. 765. [21] S. H. Kim, et al., *IEDM* 2013, p. 429. [22] S. H. Kim, et al., *VLSI* 2011, p. 58. [23] A. V. Thathachary, et al., *Nano Lett.* 2014, p. 626. [24] J.Y. Zhang et al. *APL* 2014, p.073506.

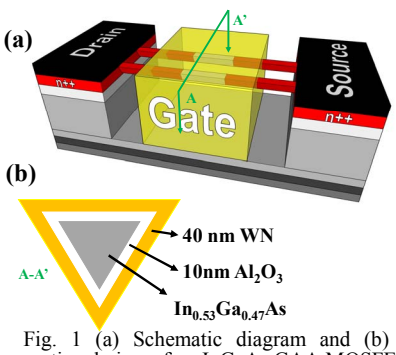

Fig. 1 (a) Schematic diagram and (b) cross-sectional view of an InGaAs GAA MOSFET with an inverted triangle shape formed by a simple wet etching process.

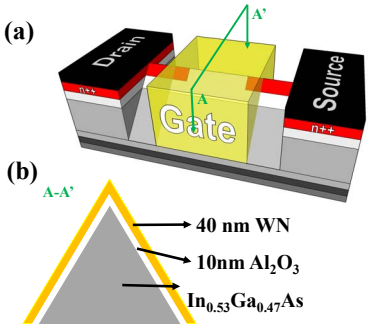

Fig. 2 (a) Schematic diagram and (b) cross-sectional view of an InGaAs MOSFET with a triangle shape. An array of triangles looks like a wave so that we call the device WaveFET.[24]

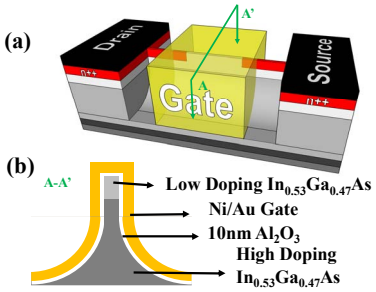

Fig. 3 (a) Schematic diagram and (b) cross-sectional view of an InGaAs FinFET with vertical sidewalls on top formed by a simple wet etching process. This device is the focus of this work.

- MBE Growth
- S/D Implantation (20keV $1\times10^{14}/cm^2$)
- Dopant Activation (600°C 15s in N_2)
- Ti Wet Etching Mask Deposition
  - 0° Nanowire
  - 45° Fin
  - 90° Wave
- Citric Acid/H_2O_2 Based Wet Etching
  - Citric Acid:H_2O_2:H_2O=15g:10ml:70ml
- ALD Al_2O_3 Dielectric Deposition
- Gate Metal Deposition
  - ALD WN for GAA FETs and WaveFETs
  - Ni/Au Ebeam Evaporation for FinFETs
- Au/Ge/Ni Ohmic Contact
- Pt/Ti/Au Body Contact
- Ni/Au Test Pads

Fig. 4 Fabrication process flow for the InGaAs GAA MOSFETs, FinFETs and WaveFETs by a novel wet etching based process.

Substrate A

100nm P-$In_{0.53}Ga_{0.47}As$ $1\times10^{17}/cm^3$
700nm P-$In_{0.53}Ga_{0.47}As$ $4\times10^{17}/cm^3$
300nm P-InAlAs $4\times10^{17}/cm^3$
P++ InP Substrate

Substrate B

100nm P-$In_{0.53}Ga_{0.47}As$ $4\times10^{17}/cm^3$
700nm P-$In_{0.53}Ga_{0.47}As$ $1\times10^{18}/cm^3$
300nm P-InAlAs $1\times10^{18}/cm^3$
P++ InP Substrate

Fig. 5 Substrate structures grown by MBE used in this work.

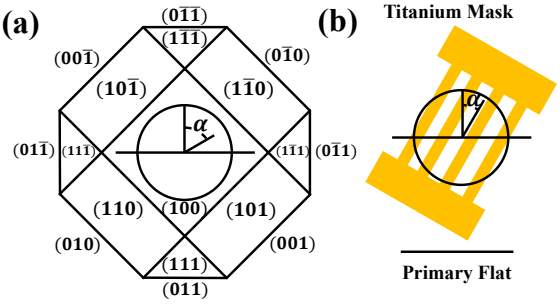

Fig. 6 (a) Crystal orientations of substrates used in this work (EJ standard). (b) Titanium mask pattern direction with respect to (a).

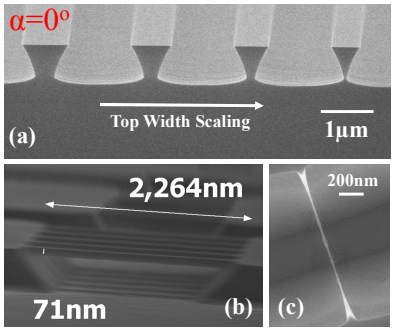

Fig. 7 (b) SEM cross-sectional view of nanowire formation by Ti mask width scaling. An inverted triangular InGaAs structure is formed due to the anisotropic wet etching. (b) The bird eye view and (c) top view of fabricated InGaAs nanowires. InGaAs nanowires can be scaled down to W_{NW}=10 nm and L_{NW}=1 μm, as shown in (c).

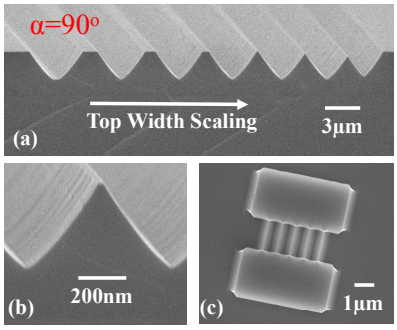

Fig. 8 (a) and (b) SEM cross-sectional illustration of wave structure formation by Ti mask width scaling. A triangular InGaAs structure is formed due to the anisotropic wet etching. (c) The top view of a fabricated InGaAs wave structure by the wet etching technology.

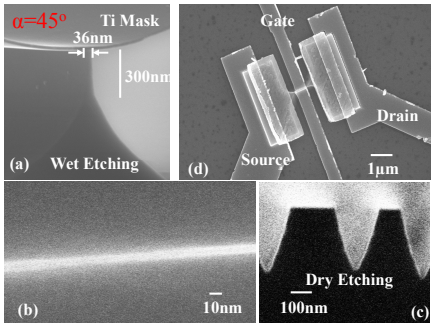

Fig. 9 (a) SEM cross-sectional view of the fin structure. Nearly vertical sidewalls are formed. Fin width is 36 nm and fin height is around 300 nm. (b) The top view of fabricated an InGaAs fin with fin width down to sub-10 nm. (c) InGaAs fins fabricated by Cl-based dry etching where vertical sidewalls are difficult to realize. (d) SEM top view of a fabricated InGaAs FinFET device.

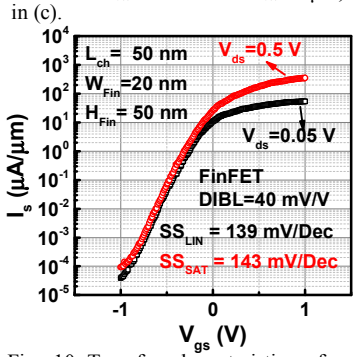

Fig. 10 Transfer characteristics of an InGaAs FinFET with L_{ch}=50nm, W_{Fin}=20nm, H_{Fin}=50nm and 10nm Al_2O_3 as dielectric.

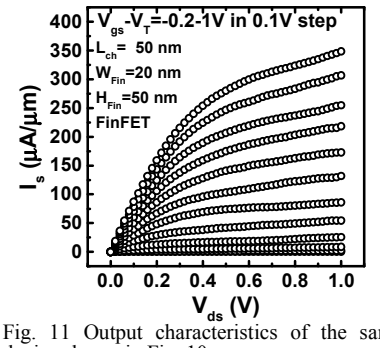

Fig. 11 Output characteristics of the same device shown in Fig. 10.

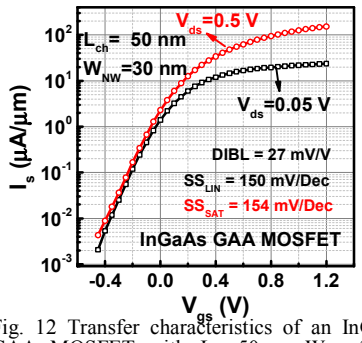

Fig. 12 Transfer characteristics of an InGaAs GAA MOSFET with L_{ch}=50nm, W_{NW}=30nm and 10 nm Al_2O_3 as gate dielectric.

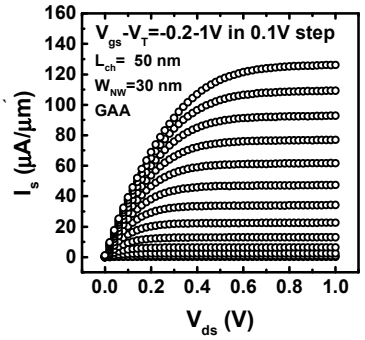

Fig. 13 Output characteristics of the same device shown in Fig. 12.

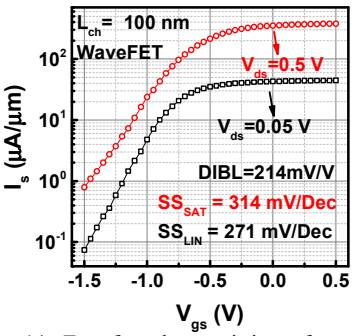

Fig. 14 Transfer characteristics of an InGaAs WaveFET with L_{ch}=100nm, 10 nm Al_2O_3 as dielectric, where SCEs become severe.

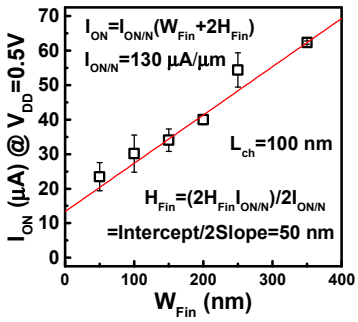

Fig. 15 Extraction of effective Fin height (H_{Fin}) by linear fitting of I_{ON} at V_{DD}=0.5V versus W_{Fin}. H_{Fin} is extracted equals to 50nm determined by the depth of ion implantation. Normalized I_{ON} at V_{DD}=0.5V for L_{ch}=100nm devices is extracted as 130μA/μm.

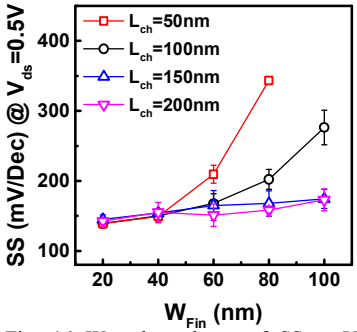

Fig. 16 W_{Fin} dependence of SS at V_{ds}=0.5V and at various L_{ch} on InGaAs FinFETs. The InGaAs FinFET devices by wet etching technique show excellent immunity to SCEs down to 50nm with W_{Fin} less than 40nm, demonstrating nearly vertical sidewall fin structure is critical to be immune to SCEs.

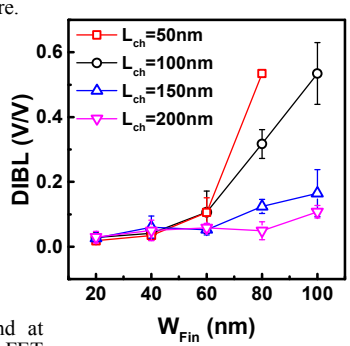

Fig. 17 W_{Fin} dependence of DIBL at various L_{ch} of InGaAs FinFETs.

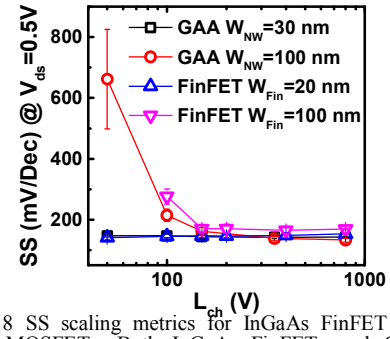

Fig. 18 SS scaling metrics for InGaAs FinFET and GAA MOSFETs. Both InGaAs FinFETs and GAA MOSFETs demonstrate good immunity to SCEs with scaled W_{Fin} or W_{NW}.

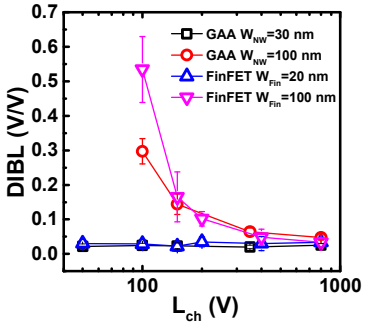

Fig. 19 DIBL scaling metrics for InGaAs FinFETs and GAA MOSFETs. Both InGaAs FinFETs and GAA MOSFETs demonstrate good immunity to SCEs with scaled W_{Fin} or W_{NW}.

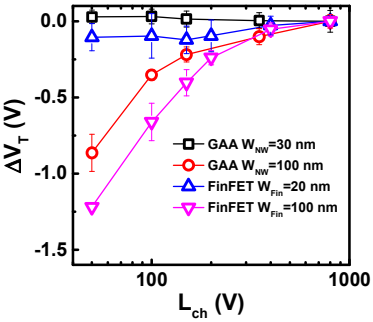

Fig. 20 V_T roll off versus L_{ch} for InGaAs FinFETs and GAA MOSFETs. Both InGaAs FinFETs and GAA MOSFETs demonstrate good immunity to SCEs with scaled W_{Fin} or W_{NW}.

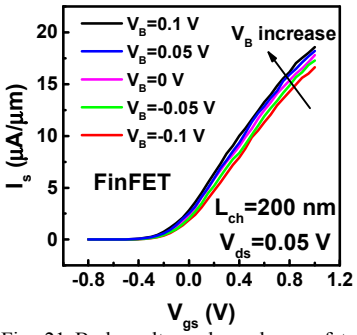

Fig. 21 Body voltage dependence of transfer characteristics at V_{ds}=0.05V on an InGaAs FinFET with L_{ch}=200nm.

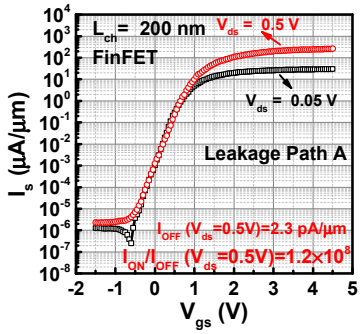

Fig. 22 Transfer characteristics of an InGaAs FinFET on bulk InGaAs with L_{ch}=200nm and record I_{ON}/I_{OFF}=1.2×10^8. The high I_{ON}/I_{OFF} is obtained by barrier engineering on the off–state leakage path.

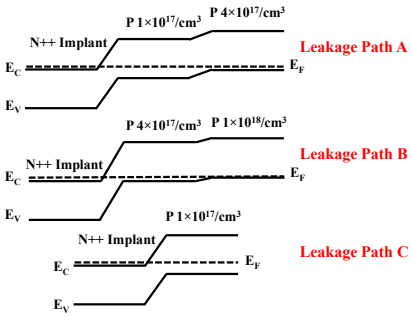

Fig. 23 Summary of energy barriers for possible off-state leakage paths of devices in this work. Leakage Path A is for InGaAs FinFET devices fabricated on substrate A. Leakage Path B is for InGaAs FinFET devices fabricated on substrate B. Leakage Path C is for InGaAs devices fabricated on substrate A but without mesa isolation.

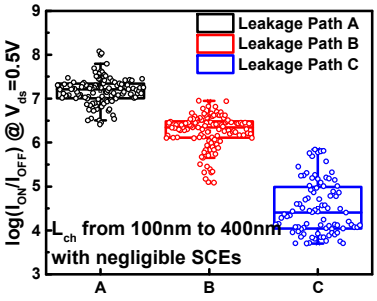

Fig. 24 I_{ON}/I_{OFF} comparison among devices with leakage path A, B and C.