Sub-60 mV/dec Ferroelectric HZO MoS_2 Negative Capacitance Field-effect Transistor with Internal Metal Gate: the Role of Parasitic Capacitance

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***Abstract*—**Steep-slope MoS_2 NC-FETs with ferroelectric HZO and internal metal gate in the gate dielectric stack are demonstrated. SS less than 50 mV/dec is obtained for both forward and reverse gate voltage sweeps, with minimum SS_{For}=37.6 mV/dec and minimum SS_{Rev}=42.2 mV/dec. A second minimum of SS_{Rev} as low as 8.3 mV/dec can be measured as the result of dynamic switching at high speed in ferroelectric HZO. The impact of parasitic capacitance on SS and dynamic hysteresis is systematically studied by both experiment and dynamic simulation.

I. Introduction

Negative capacitance field-effect transistor (NC-FET) is one of the promising solutions to overcome the fundamental thermionic limit of subthreshold slope (SS) of a metal-oxide-semiconductor field-effect transistor (MOSFET), which is about 60 mV/dec at room temperature [1-10]. Meanwhile, 2-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have the potential for ultra-scaled transistor technology beyond 10 nm technology node because of their atomically thin layered channel and low dielectric constant, which offers strong electrostatic control. Junctionless MoS_2 FETs exhibit high on/off ratio and strong immunity to short channel effects for transistor applications with channel length (L_{ch}) down to sub-5 nm [11, 12].

In this work, we demonstrate steep-slope MoS_2 NC-FETs with ferroelectric hafnium zirconium oxide (HZO) and internal metal gate (IMG) in the gate stack. SS less than 50 mV/dec is obtained for both forward and reverse gate voltage sweeps, with minimum SS_{For}=37.6 mV/dec and minimum SS_{Rev}=42.2 mV/dec. A second minimum of SS_{Rev} as low as 8.3 mV/dec can be measured as the result of dynamic switching at high speed in ferroelectric HZO. The impact of parasitic capacitance (C_f) between drain electrode and IMG on SS and hysteresis is systematically studied by both experiment and dynamic simulation. It is found that the parasitic capacitance contributes to the reduction of SS but leads to a larger dynamic hysteresis. Therefore, the balance of SS and switching speed need to be considered in real device applications.

II. Experimental

Fig. 1(a) and 1(b) show the schematic diagram of MoS_2 NC-FETs with and without internal metal gate. 20 nm Ni as IMG and 10 nm HfO_2 as gate dielectric for internal MoS_2 FET are inserted into the structure of Fig. 1(a) to fabricate MoS_2 NC-FETs with IMG as shown in Fig. 1(b). The MoS_2 NC-FETs with IMG consist of few-layer MoS_2 as channel, 20 nm polycrystalline HZO layer, 3 nm amorphous aluminum oxide (Al_2O_3) layer, 20 nm Ni layer and 10 nm HfO_2 as the gate dielectric, heavily doped silicon substrate as the gate electrode and nickel as the source/drain contacts. Fig. 2 show the top-view SEM images of MoS_2 NC-FETs with and without IMG, corresponding to the structures in Fig. 1(a). Fig. 3 shows a cross-sectional TEM image of a MoS_2 NC-FET without IMG.

The detailed fabrication process of MoS_2 NC-FETs without IMG can be found in [1]. The device fabrication process of MoS_2 NC-FETs with IMG is discussed as following. $Hf_{0.5}Zr_{0.5}O_2$ film was deposited by atomic layer deposition (ALD) at 250 °C on a heavily doped low resistivity silicon substrate after standard RCA cleaning, diluted HF dip and deionized water rinse. $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), and H_2O were used as the Hf precursor, Zr precursor, and oxygen precursor, respectively. The $Hf_{1-x}Zr_xO_2$ film with x = 0.5 was achieved by controlling HfO_2:ZrO_2 cycle ratio of 1:1. Another 3 nm Al_2O_3 was subsequently *in-situ* deposited using $Al(CH_3)_3$ (TMA) and H_2O also at 250 °C. An amorphous Al_2O_3 layer was applied for capacitance matching and gate leakage current reduction through polycrystalline HZO. Then, the IMG pattern was defined by electron-beam lithography, followed by 20 nm Ni electron-beam evaporation and lift-off process. Another 10 nm HfO_2 was deposited by ALD at 250 °C using TDMAHf and H_2O as precursors. The annealing process was then performed by rapid thermal annealing (RTA) in nitrogen ambient for 1 minute at 400 °C. MoS_2 flakes were transferred to the substrate by scotch-tape based mechanical exfoliation. 100 nm nickel electrodes as electrical source/drain contacts were fabricated using electron-beam lithography, electron-beam evaporation and lift-off process.

III. Results and Discussion

Fig. 4 shows the DFT calculation on the ferroelectricity of HZO/Al_2O_3 gate stack. Fig. 4(a) shows the electron difference density of HZO/Al_2O_3 with ion displacement in HZO. Fig. 4(b) and 4(c) show the calculated P-E and C-E curves simulated by DFT calculations based on the structure in Fig. 4(a). The HZO/Al_2O_3 is implemented by ATK2016 (DFT calculation) with CI-Nudged elastic band method [8]. According to the simulation, negative capacitance behavior of the HZO/Al_2O_3 gate stack can be achieved as shown in the S-shaped P-E curve, which is also evidenced in the extracted C-E curves. Experimentally, the polarization vs. voltage (V_{total}) are directly measured at three different voltage range by a Radiant Precision LC II test system, as shown in Fig. 5 and Fig. 6 at two different RTA temperatures. Clear ferroelectricity enhancement by RTA at 450 °C can be observed comparing with no RTA sample. V_{total} here is defined as the voltage across the entire capacitor and it equals to the sum of voltage across the Al_2O_3 layer (V_{AlO}) and voltage across the HZO layer (V_{HZO}), as shown in eqn. (1) in Fig. 8. V_{AlO} can be calculated as eqn. (2) in Fig. 8, because Al_2O_3 layer offers a linear capacitance. Therefore, by subtracting V_{AlO} from V_{total}, V_{HZO} can be obtained, as eqn. (3) in Fig. 8. Thus, polarization vs. voltage and electric field across the HZO layer can be obtained, as shown in Fig. 9, showing a negative slope. In addition, as dP/dV

can be seen as the dynamic capacitance during the measurement, the maximum dP/dV reflects the maximum capacitance during the measurement. The maximum capacitances (dP/dV) measured are 2.69 μF/cm^2, 4.28 μF/cm^2 and 5.95 μF/cm^2, corresponding to 6 V, 8 V and 10 V voltage measurement ranges, as shown in Fig. 7. The equivalent oxide thicknesses (EOT) are calculated to be 1.3 nm, 0.8 nm and 0.6 nm. As the EOT of 3 nm Al_2O_3 layer is about 1.3 nm, suggesting the capacitance of HZO layer is negative to obtain EOT less than 1.3 nm [13]. The physical origin of the negative slope obtained in Fig. 9 and its impact by the measured low leakage current and interface traps are still under investigation.

Fig. 10 shows the I_D-V_{GS} characteristics of a MoS_2 NC-FET with IMG and with 0.5 μm channel length (L_{ch}) and 8 nm channel thickness (T_{ch}). Fig. 11 shows the I_D-V_{GS} characteristics of the internal MoS_2 FET of the same device as in Fig. 10. Fig. 12 shows a representative MoS_2 NC-FET without IMG (Gate stack annealed at same 400 ºC). Fig. 13 shows SS vs. I_D in the off-state of the same devices as in Fig. 10 and Fig.11, to compare MoS_2 NC-FET with IMG and the internal MoS_2 FET with 10 nm HfO_2 only as gate dielectric. A plateau and a minimum characterize the sub-60 mV/dec SS (vs I_D) during reverse sweep for MoS_2 NC-FETs. These features ($SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$) are observed among almost all fabricated devices. The second local minimum of SS is the result of the switching between two polarization states of the ferroelectric oxide, associated with loss of capacitance matching at high speed. All the device I_D-V_{GS} characterization are kept at the same measurement speed (at about 0.05 V/s). The MoS_2 NC-FET with IMG exhibits SS_{For}=37.6 mV/dec, $SS_{Rev,min\#1}$=42.2 mV/dec, and $SS_{Rev,min\#2}$=8.3 mV/dec but with a negative 0.33 V hysteresis at I_D=1 nA/μm, comparing to a negative 0.1 V hysteresis in MoS_2 NC-FET without IMG. This suggests the enhanced C_f lead to a larger hysteresis and smaller SS [1]. The SS of the MoS_2 NC-FET with IMG is much smaller than the SS measured from the internal MoS_2 FET, indicating the exist of internal amplification of the 20 nm HZO/3 nm Al_2O_3 stack. Fig. 14 shows the gate leakage current measured from the gate stack of Fig. 1(b). The calculated the gate leakage current is less than 100 fA/μm within ±2 V so that the gate leakage current is negligible to device I-V characteristics. Fig. 15 shows the comparison of I_D-V_{GS} characteristics measured at V_{DS}=0.1 V between the MoS_2 NC-FET with IMG and the internal MoS_2 FET. The improved drain current suggesting the reduction of contact resistance by the internal amplification of negative capacitance gate stack. Fig. 16 and Fig. 17 show the internal amplification measured from MoS_2 NC-FET (V_G) and the internal MoS_2 FET (V_{int}), where the internal amplification is defined as dV_{int}/dV_G. Internal amplification greater than 2 is achieved for both forward and reverse gate voltage sweeps.

To further understand the impact of parasitic capacitance (C_f) on the SS and hysteresis of MoS_2 NC-FETs, both steady-state and dynamic simulation are performed. The hysteresis of MoS_2 NC-FETs origins from two reasons. One reason is total gate capacitance (C_{device}+C_{FE}) is negative and the entire system is unstable. This reason can't explain the hysteresis of MoS_2 NC-FET in this work since the hysteresis will disappear if the measurement sweep speed is very slow [1]. However, the steady-state model is ideal while the actual measurement process is dynamic because the rise time of the gate voltage cannot be infinite so that V_{mos} cannot follow the change speed of V_{GS}, which leads to the hysteresis as the second origin [14]. The dynamic effect can be modeled by adding a dumping resistor in series with the ferroelectric capacitor, as shown in Fig. 18. The simulation methodology is described in detail in [1]. Fig. 19 and Fig. 20 show the dynamic and steady-state simulation of MoS_2 NC-FET with 20 nm HZO and 2 nm Al_2O_3 gate stack at various parasitic capacitance. No hysteresis can be observed in the steady-state simulation of Fig. 19, indicating the hysteresis measured in this work is a dynamic effect of measurement. As shown in the dynamic simulation of MoS_2 NC-FET in Fig. 18, by increasing the parasitic capacitance, SS reduces while the hysteresis is increasing. Fig. 21 shows SS versus C_f for both dynamic and steady-state simulation. SS extracted from both forward and reverse gate voltage sweep reduces with C_f while SS_{For} is close to the SS in steady-state simulation. Therefore, the steep slope of SS measured from reverse gate voltage sweep most likely comes from the dynamic effect of the measurement. Fig. 22 and Fig. 23 shows the threshold voltage (V_T) and hysteresis as a function of C_f. Hysteresis is found to increase with the increase of parasitic capacitance. Thus, high parasitic capacitance prevents the NC-FETs to work at high speed so that the optimization of parasitic capacitance to balance between SS and working speed in NC-FETs is required.

ACKNOWLEDGMENT

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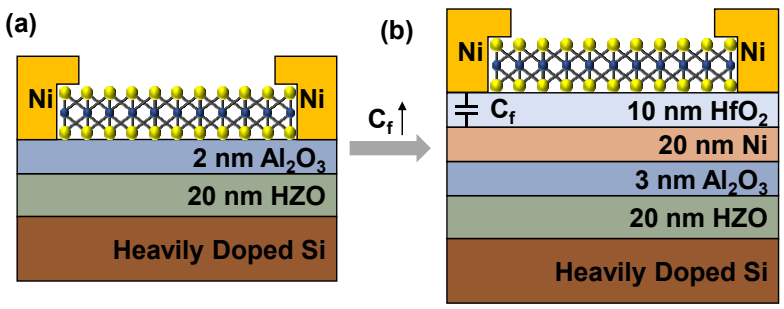


Fig. 1. Schematic of MoS_2 NC-FETs (a) without and (b) with internal metal gate.

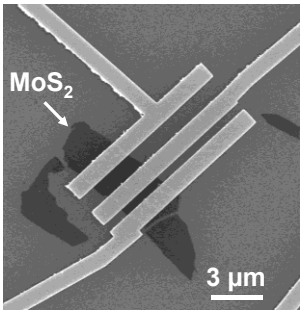


Fig. 2. Top-view SEM image of MoS_2 NC-FETs.

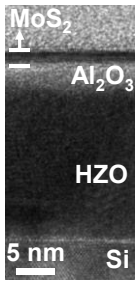


Fig. 3. TEM cross-sectional image of a MoS_2 NC-FET as in Fig.

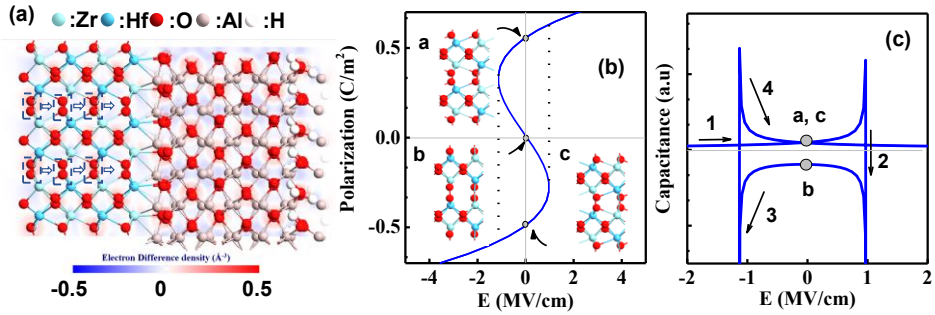


Fig. 4 (a) Electron density difference of the HZO (polarization direction [001]) on α-Al_2O_3. (b) P-E and (c) C-E curves of FE-HZO/Al_2O_3 simulated by DFT calculations. S-shaped P-E indicates negative capacitance behavior can be achieved in the HZO/Al_2O_3 gate stack.

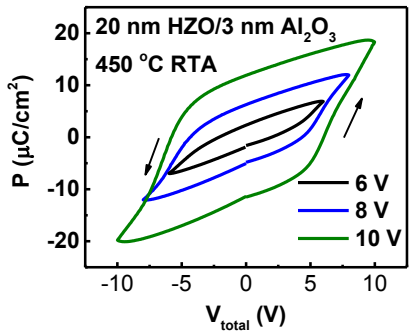


Fig. 5. Hysteresis loop of polarization vs. voltage for 20 nm HZO/3 nm Al_2O_3 annealed at 450 °C at various voltage sweep ranges.

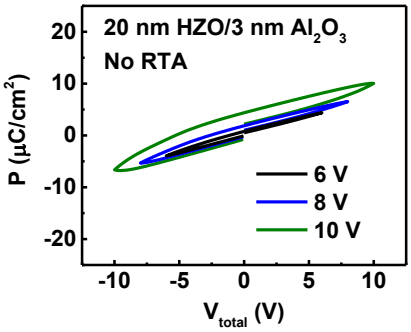


Fig. 6. Hysteresis loop of polarization vs. voltage for 20 nm HZO/3 nm Al_2O_3 without RTA at various voltage sweep ranges.

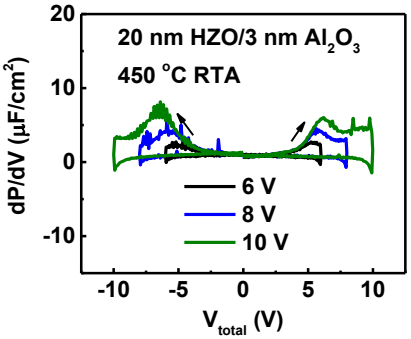
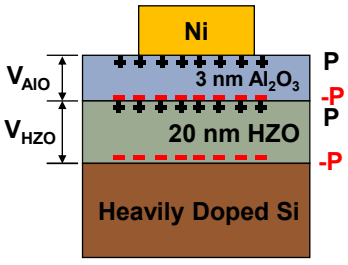


Fig. 7. dP/dV of polarization vs. voltage characteristics in Fig. 5.



$$V_{total} = V_{AlO} + V_{HZO} \quad (1)$$

$$V_{AlO} = \frac{P}{C_{AlO}} \quad (2)$$

$$V_{HZO} = V_{total} - \frac{P}{C_{AlO}} \quad (3)$$

Fig. 8. Illustration and calculation of voltage across the HZO layer during polarization vs. voltage measurement.

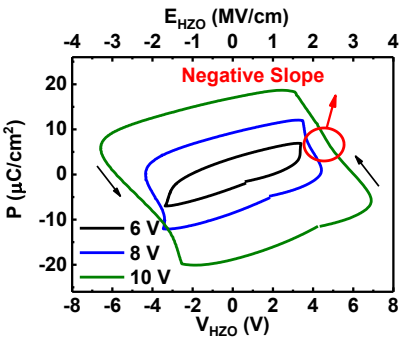


Fig. 9. Hysteresis loop of polarization vs. voltage for 20 nm HZO only annealed at 450 °C at various voltage sweep ranges, calculated based on Fig. 8.

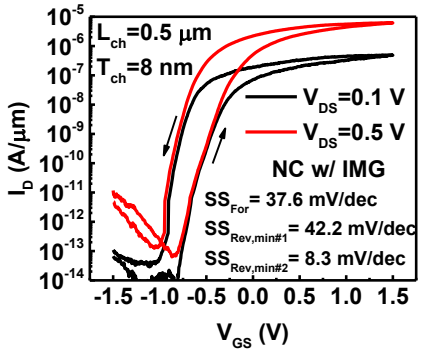


Fig. 10. I_D-V_{GS} characteristics of MoS_2 NC-FET with IMG measured at room temperature, same structure as Fig. 1(b).

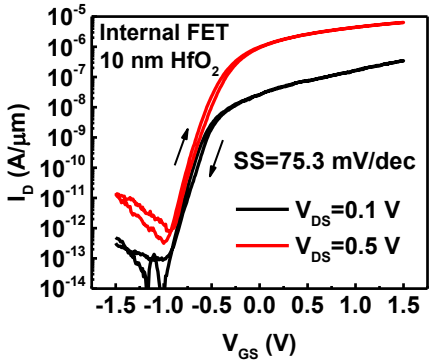


Fig. 11. I_D-V_{GS} characteristics of internal MoS_2 FET of the same device as Fig. 10 but has 10 nm HfO_2 as gate dielectric.

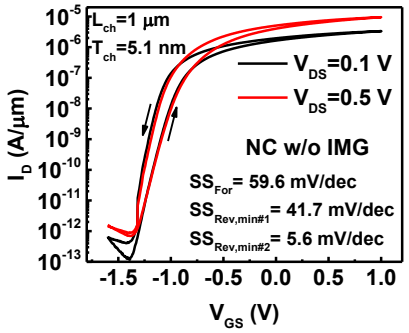


Fig. 12. I_D-V_{GS} characteristics of MoS_2 NC-FET without IMG measured at room temperature, same structure as Fig. 1(a).

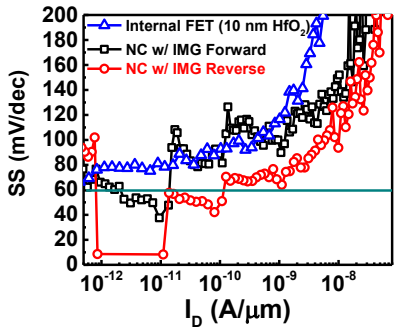


Fig. 13. SS vs. I_D characteristics of MoS_2 NC-FET with IMG and internal MoS_2 FET of the same device.

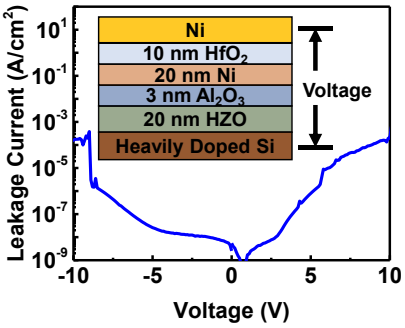


Fig. 14. Leakage current vs. voltage measured using the gate stack in Fig. 1(b). The leakage current is negligible in all the I-V characteristics.

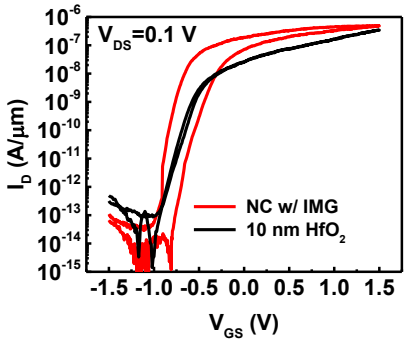


Fig. 15. I_D-V_{GS} characteristics comparison between MoS_2 NC-FET with IMG and the internal MoS_2 FET of the same device.

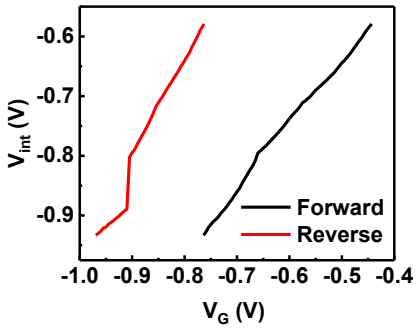


Fig. 16. V_{int} vs. V_G for MoS_2 NC-FET with IMG calculated based on internal MoS_2 FET as in Fig. 15.

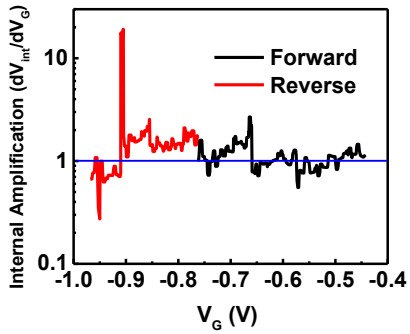


Fig. 17. Internal amplification calculated based on dV_{int}/dV_G in Fig. 16.

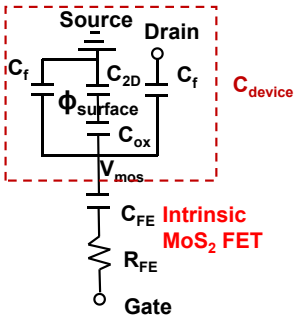


Fig. 18. Simplified small-signal capacitance representation of a MoS_2 NC-FET for steady-state and dynamic simulation.

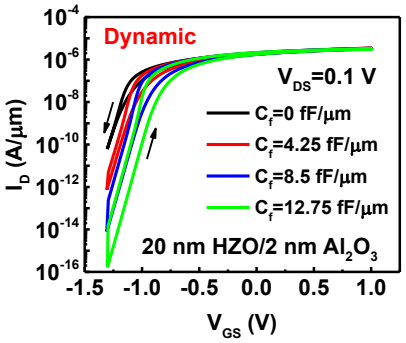


Fig. 19. Dynamic simulation of I_D-V_{GS} characteristics of MoS_2 NC-FET with various parasitic capacitance.

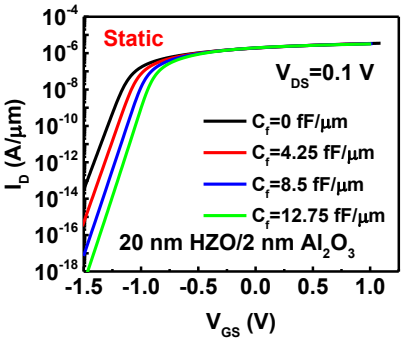


Fig. 20. Steady-state simulation of I_D-V_{GS} characteristics of MoS_2 NC-FET with various parasitic capacitance.

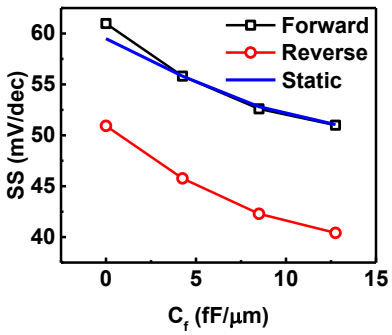


Fig. 21. The impact of parasitic capacitance on SS in dynamic and steady-state simulation.

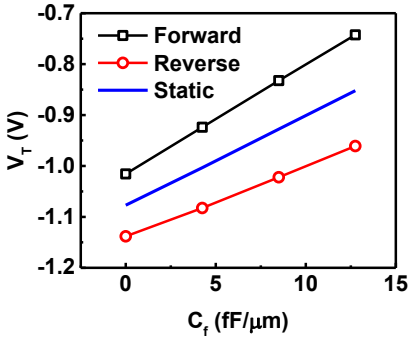


Fig. 22. The impact of parasitic capacitance on V_T in dynamic and steady-state simulation.

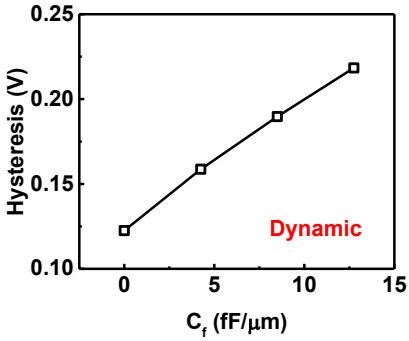


Fig. 23. The impact of parasitic capacitance on hysteresis in dynamic simulation.