First Demonstration of BEOL-Compatible Ultrathin Atomic-Layer-Deposited InZnO Transistors with GHz Operation and Record High Bias-Stress Stability

D. Zheng[1], A. Charnas[1], J. Anderson[1], H. Dou[2], Z. Hu[2], Z. Lin[1], Z. Zhang[1], J. Zhang[1], P.-Y. Liao[1], M. Si[1], H. Wang[2], D. Weinstein[1] and P. D. Ye[1,*]

[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA, *Email: yep@purdue.edu

[2]School of Materials Engineering, Purdue University, West Lafayette, IN, USA

Abstract — This work reports for the first time ultrathin atomic-layer-deposited (ALD) InZnO as a novel back-end-of-line (BEOL) channel material for monolithic 3D integration. By tuning the ratio of In to Zn with ALD cycles, InZnO transistors with 3.5 nm channel thickness can achieve excellent subthreshold swings (SS) as low as 65 mV/dec, high on-off current ratio up to 10^{11}, and sizeable on-current density (I_{ON}) up to 1.33 A/mm for In-rich channels at 100 nm channel length with drain voltage (V_{DS}) of 1 V. A surprising high degree of stability under large positive gate bias stress (statistically measured threshold voltage shift ΔV_T of -16 mV after 1500 s stress with gate voltage bias (V_{Bias}) of 3.5 V) is observed in the In:Zn=1:1 case. ALD process resolves the long-time concern on the stability of sputtered InZnO films as the channels without Ga doping. A charge-neutrality-level (CNL) alignment and trap generation model is proposed to explain this unique phenomenon of negligible V_T shift under positive gate bias stress (PBS). Finally, ground-signal-ground (GSG) structures are also fabricated to investigate the RF performance of these BEOL-compatible transistors with GHz operation frequencies.

I. Introduction

Oxide semiconductors such as pure In_2O_3 [1], Sn-doped and W-doped In_2O_3 (ITO and IWO) [2,3], and indium-gallium-zinc-oxide (IGZO) [4] are regarded as promising candidates for next-generation BEOL-compatible transistors towards monolithic 3D integration. Recently, tremendous efforts have been spent on the systematic investigation of ALD atomically thin In_2O_3 due to its high carrier density, high mobility, and ultra-low contact resistivity from its unique CNL band alignment and intrinsic high electron band velocity at high electron density [5]. Despite its excellent transport properties, the stability of In_2O_3 remains a concern. From the large amount of work on sputtered IGZO films for display applications, Sn, Ga, W, and other elements have been reported as effective dopants as carrier suppressors and strong oxygen binders to improve the stability of bulk In_2O_3 in the past. We want to emphasize here that ALD In_2O_3-based films could be very different from the sputtered ones and they have never been systematically studied at a few nanometers thickness before.

In this work, we demonstrate high-performance ALD InZnO thin-film-transistors (TFTs) with near-ideal SS down to 65 mV/dec, high on-off ratio of 10^{11}, relatively large I_{on} of 0.55-1.3 A/mm, and record-high stability ΔV_T of -16 mV after 1500s PBS. The negligible V_T shift under PBS can be explained by the special band-alignment of In_2O_3, which is the key to deeply understand all characteristics of In_2O_3-based oxide semiconductors including InZnO [6,7]. Fig. 1 shows the band-alignment of related oxides with CNL level for metal/semiconductor interfaces and sometimes called trap neutral level (TNL) for dielectric/semiconductor interfaces. E_{CNL} or E_{TNL} is deeply inside the conduction band for In_2O_3 and it can be shifted towards conduction band edge in InZnO. This is the fundamental reason for ultra-low contact resistivity and surface accumulation of electrons in In_2O_3 and also InZnO.

II. Experiments

ALD growth, device schematic, and process flow for the fabrication are illustrated in Figs. 2-4. After the standard cleaning process, a 10 nm Al_2O_3 layer was grown by ALD using TMA and H_2O at 175°C on top of 90 nm thermally grown SiO_2 on p+ Si substrate to obtain a smooth surface. A bilayer photoresist lithography process was used to form a 40 nm Ni bottom gate with sharp edges by e-beam evaporation, followed by a 6 nm HfO_2 by ALD at 200 °C with TDMAHf and H_2O as Hf and O precursors. InZnO channel was realized by ALD at 225 °C with TMIn, DEZn, and H_2O as In, Zn, and O precursors. A complete cycle of ALD growth of InZnO started with one cycle of ZnO with DEZn and H_2O, followed by N cycles of In_2O_3 with TMIn and H_2O (N is set to be 5, 3, and 1 to change the In and Zn concentrations as desired). Note that 7 ALD cycles lead to one atomic layer so that the InZnO films are indeed mixed amorphous ones instead of nanolaminates. The thickness of ALD InZnO film (3.5 nm) was determined by an ellipsometer (Gaertner L116A) calibrated by HRTEM and AFM [1]. O_2 annealing at 250 °C for 60 s is applied here to improve the interface quality and lower the carrier density by filling the oxygen vacancies. The thermal budget of the process is below 250 °C. In this paper, In:Zn=5:1, 3:1, and 1:1 indicate the ALD cycle ratios of In and Zn, which could be moderately different from the real atomic content ratio of In and Zn.

Electrical characterization was conducted with the Keysight B1500 system in ambient. RF characteristics were measured using a Keysight N5225A vector network analyzer (VNA) from 30 MHz to 20 GHz. DC bias was provided by Keithley 2400 SMUs connected to the VNA bias tees and synchronized programmatically. On-wafer short and open device structures were employed to de-embed pad parasitic effect.

III. Results and Discussion

Figure 5 presents a SEM image of a single device from the as-fabricated InZnO transistor array with a TEM image and EDS mapping of In, Zn and Hf shown in Fig. 6. Figs. 7-8 represent the output and transfer characteristics of a long channel as-fabricated InZnO (In:Zn=1:1) transistors showing all well-behaved on-state and off-state performance. Characteristics of a 100 nm short-channel InZnO device are presented in Figs. 9-10 with improved I_{on} to 550 mA/mm at V_{DS}=1.0V. Figs. 11-14 show the detailed performances of InZnO transistors with different In:Zn ratios after O_2 annealing for 60s at 250°C. At least 5 devices were measured for the average extraction. Negligible hysteresis and DIBL indicate low interface trap density and immunity to the short channel effects along with the significantly improved SS to 65 mV/dec and high on-off ratio to 10^{11} (In:Zn=1:1) due to the wide bandgap of ~3.0 eV for InZnO. After annealing, V_T shift to right and the device is operated in enhancement-mode. I_{on} of 550 mA/mm is still achieved by higher V_{GS} and V_{DS} as shown in Figs. 11-12. Higher I_{on} of 1.18 A/mm and 1.33 A/mm can be achieved with increased In:Zn ratio of 3:1 and 5:1 without scarifying too much SS and I_{on}/I_{off} ratio as shown in Figs. 13 and 14. Increased Zn ratio leads to E_{TNL} approaching conduction band edge, lower carrier density and larger bandgap, resulting in a better current saturation characteristic.

Statistical analysis of V_T and field-effect mobility μ_{FE} is illustrated in Fig. 15, where at least five devices are measured at each point. Zn serves as the scattering center that reduces the mobility from 45 to 22 $cm^2/V\cdot s$ and no obvious V_T rolling off indicates a high short channel effect immunity in the ultrathin channel regime; positively shifted V_T is able to be tuned from depletion-mode to enhancement mode by In:Zn ratio due to the E_{CNL} or E_{TNL} described above.

PBS instability test is the most important reliability test for n-channel devices. The n-type InZnO channel was measured with V_{Bias} fixed as V_T + 3 V for at least 1500 sec, and the linear extrapolation method is used to evaluate the V_T degradation. V_{DS}, channel length and width are fixed as 0.05 V,100 nm and 1 µm to avoid geometry dependence for a fair comparison in different In:Zn ratio channels during the reliability measurements. Fig. 16 illustrates extremely small, almost negligible V_T degradation in InZnO (In: Zn=1:1) TFT transfer curves. This is an extraordinary reliability data for any In_2O_3 based devices since it is widely reported that sputtered In_2O_3 or InZnO have serious PBS instability. Here, we propose a physics model considering E_{TNL} and trap generation in Fig. 19 to explain this surprising observation. As the band alignment is shown in Fig. 1, E_{CNL} or E_{TNL} of ZnO lies inside the bandgap and close to the conduction edge. E_{TNL} of InZnO with In:Zn=1:1 could be located very near to E_C where both acceptor-like and donor-like traps compensate each other, locate at the lowest valley of two types of traps as shown in Fig. 19 and is less sensitive to trap states in general. E_F at V_T should be located inside bandgap but very near E_C since the device is enhancement-mode as shown in Figs. 11 and 12. Under PBS, E_F moves up through E_{TNL} but generates the smallest donor-like traps and leads to negligible negative V_T shift in In:Zn=1:1 case. With the increase of In:Zn ratio, E_{TNL} moves up inside the conduction band and locates itself at more donor-like trap states. After PBS, much more donor-like trap states are generated as positive charges and V_T shifts negatively and become sensitive at PBS as shown in Fig. 18 in comparison of PBS on 3.5 nm InZnO and In_2O_3 TFTs. It is noticeable that higher Zn improves ΔV_T from -349 mV (In_2O_3), -219 mV (In:Zn=5:1), -162 mV (In:Zn=3:1), to -16 mV (In:Zn=1:1) after 1500s positive bias stress in the statistical measurement. The outstanding stability of PBS on ALD InZnO (In:Zn=1:1) and the proposed model are the main experimental observation and understanding of this work.

By leveraging the improved saturation DC performance, a ground-signal-ground (GSG) structure was fabricated with the schematic and optical image shown in Fig. 20, where an optimized Ti/Au/Ni as the metal gate and Ni/Au as the contacts. L_{OV} and L_G are also carefully designed to reduce the parasitic capacitance in the RF measurement. Fig. 21 shows the RF transistor with an effective channel length of 350 nm including L_{OV} of 100 nm and L_G of 150 nm. V_{DS} and V_{GS} can be biased at 1.2 V and 5 V, respectively, due to the improved output saturation. Transit frequency (f_T) and maximum frequency of power gain (f_{max}) were extracted from the de-embedded S-parameter measurements as 3.8 GHz and 5 GHz, respectively. Fig. 22 shows the off-state breakdown V_{DS} of ~6V limited by 6 nm HfO_2 and depleted 3.5nm InZnO. InZnO itself has a measured breakdown field of 0.45 MV/cm if a 90 nm thick SiO_2 dielectric is applied. Channel dependence of f_T and f_{max} is also investigated based on the long-channel InZnO transistors, where a near-exponentially increasing trend can be observed as the channel length is scaled, as shown in Fig. 23. As InZnO is highly scalable and stable, there is a significant room for further improving the performance of InZnO RF transistors by deeper channel length scaling. We would emphasize the achieved f_T and f_{max} are among the high values reported for BEOL oxide semiconductor devices. Table 1 presents a benchmark InZnO TFTs in this work with other state-of-the-art back-gate amorphous oxide semiconductors [3,8-11]. Beyond the benefits of high carrier concentration and mobility, a large bandgap and high-quality oxide/oxide interface, InZnO TFTs outperform all oxide semiconductors in terms of PBS stability due to its unique band-alignment as described above.

IV. Conclusion

In conclusion, BEOL-compatible ALD InZnO FETs with remarkable DC and reliability performance are demonstrated. Negligible negative V_T shift under PBS for InZnO (In:Zn=1:1) can be understood by the model of E_{TNL} near the conduction band edge which becomes less sensitive to trap generations. This work provides a new route to engineer novel BEOL oxide semiconductor channels by tailoring their band-alignments. The work is supported by SRC nCore IMPACT Center, AFOSR, and DARPA/SRC JUMP ASCENT Center.

References

[1] M. Si *et al.*, Nat. Electron., vol. 5, p. 164, 2022. [2] S. Li *et al*, Nat. Mater., vol. 18, p.1091, 2019. [3] W. Chakraborty *et al.*, IEEE TED, vol. 67, p. 5336, 2020. [4] J. Guo *et al*, IEDM, 2021. [5] Z. Lin, *et al*. arXiv, 2205.00360, 2022. [6] M. Si *et al.*, Nano Lett., vol. 21, p. 500, 2021. [7] J. Robertson *et al.*, PRB, vol. 83, p. 075205, 2011. [8] E. Chong *et al.*, Semicond. Sci. Technol., vol. 27, p. 012001, 2011. [9] H. C. Wu *et al.*, ECS J. Solid State Sci. Technol., vol. 3, p. Q24, 2013. [10] Q. Kong *et al.*, VLSI-TSA, p. 1-2, 2022 [11] Q. Li *et al.*, Membranes, vol. 11, p. 929, 2021.

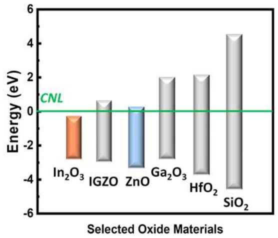

Fig. 1. CNL alignments with conductance band and valence band of selected oxide semiconductors and insulators.

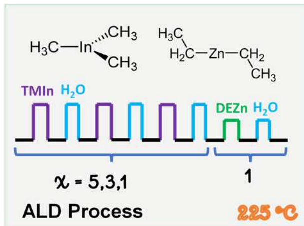

Fig. 2. Illustration of InZnO ALD growth by tuning the growth cycle ratio of In and Zn as 5:1, 3:1 and 1:1, respectively at 225 °C.

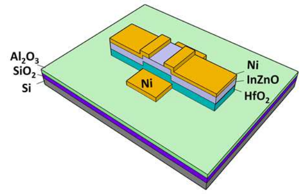

Fig. 3. Schematic diagram of buried gate BEOL InZnO transistor with HfO_2 as the gate dielectric and Ni as S/D contacts.

- ❑ SiO_2/Si substrate solvent cleaning
- ❑ ALD growth of 10nm Al_2O_3 at 175°C
- ❑ E-beam evaporation of 40nm Ni as buried gate
- ❑ ALD growth of 6 nm HfO_2 at 200°C as dielectric
- ❑ ALD growth of 3.5 nm InZnO with growth cycles ratio as 5:1, 3:1 and 1:1 at 225°C
- ❑ Isolation through Ar/SF_6 dry etch
- ❑ E-beam evaporation of 40nm Ni as Source/Drain
- ❑ 250°C O_2 annealing for 60s

Fig. 4. Fabrication process flow of InZnO MOSFETs

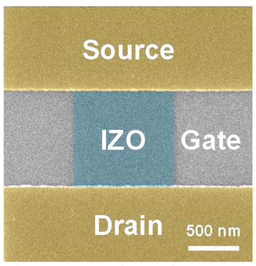

Fig. 5. False-color SEM image of single device.

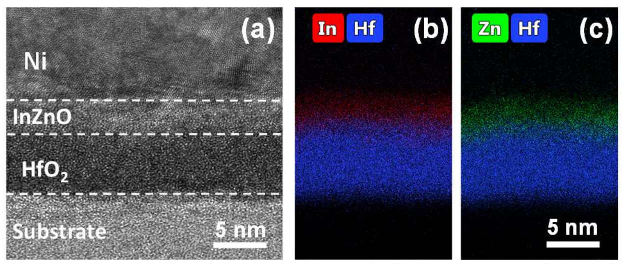

Fig. 6. Cross-sectional TEM image and (b)(c) EDS mapping under HAADF STEM of In, Zn and Hf.

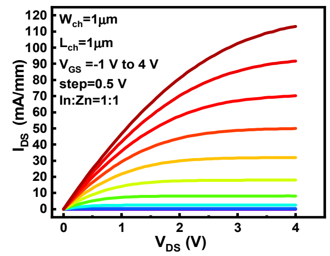

Fig. 7. Output curves of a long-channel InZnO (1:1) transistors with L_{ch}=1 μm and W_{ch}=1 μm before O_2 annealing showing well-behaved DC characteristics and current saturation at high V_{DS}.

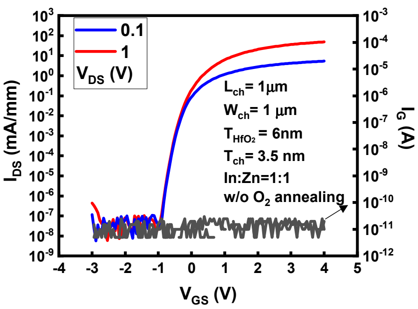

Fig. 8. Transfer curves of the same device in Fig. 7, showing low gate leakage current and also well-controlled off-state performance.

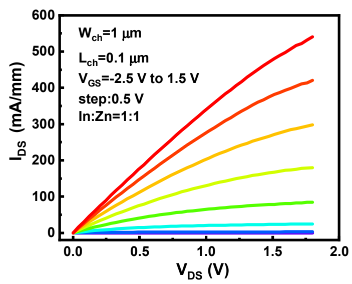

Fig. 9. I_{DS}-V_{DS} output curves of a short-channel InZnO (1:1) transistor with L_{ch}=0.1 μm and W_{ch} =1 μm before O_2 annealing.

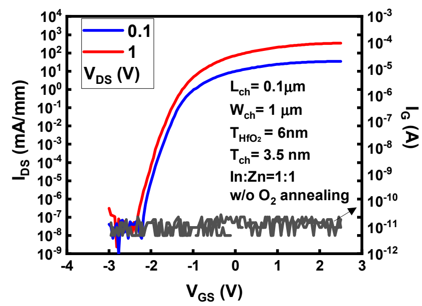

Fig. 10. I_{DS}-V_{GS} transfer curves of the same device as in Fig. 9.

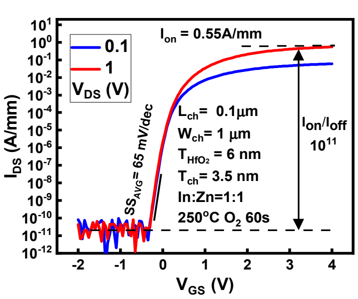

Fig. 11. I_{DS}-V_{GS} transfer characteristics of an annealed InZnO (In: Zn=1:1) transistor of Figs. 9-10, exhibiting better SS of 65 mV/dec and I_{on}/I_{off} ratio, and similar 0.55 A/mm as on-current I_{on}.

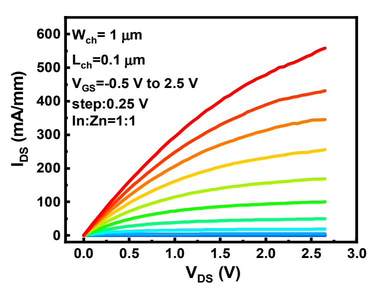

Fig. 12. I_{DS}-V_{DS} output characteristics of the same device in Fig.11 after O_2 annealing. Similar I_{on} can be achieved at higher V_{GS} and V_{DS}.

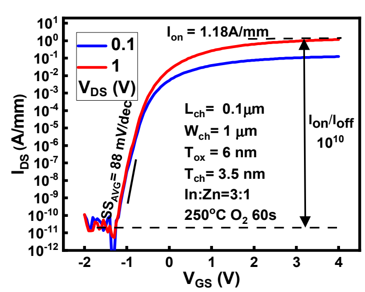

Fig. 13. I_{DS}-V_{GS} transfer characteristics of an annealed InZnO (In: Zn=3:1), exhibiting SS of 88 mV/dec, and 1.18 A/mm on-current.

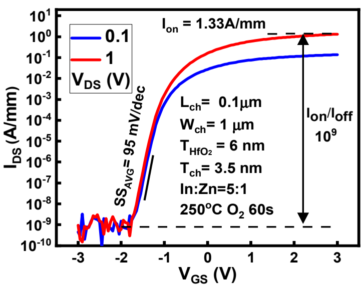

Fig. 14. I_{DS}-V_{GS} transfer characteristics of an annealed InZnO (In: Zn=5:1), exhibiting SS of 95 mV/dec, and 1.33 A/mm on-current.

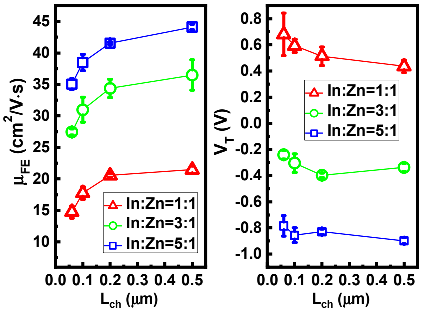

Fig. 15. Statistic results of channel-length dependent field-effect mobility and threshold voltage with different In:Zn ratios (each data point represents the average of at least five devices).

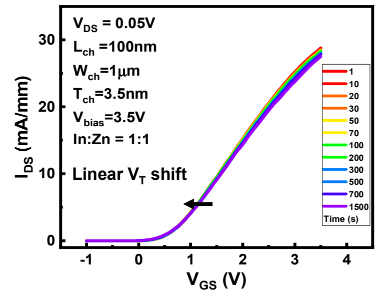

Fig. 16. I_{DS} vs. V_{GS} relationship with stress time up to 1500 s for a large positive gate bias stress.

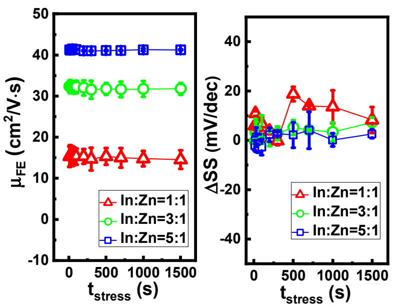

Fig. 17. μ_{FE} and ΔSS dependence on stress time with gate biased at V_T +3V. Each data point represents the average of at least five devices.

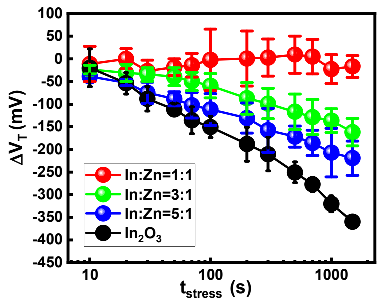

Fig. 18. V_T shifts negatively with stress time increasing in different In:Zn ratios in the statistical measurement, with gate biased at V_T +3V. Negligible V_T shift is obtained for 1:1 InZnO. Each data point represents the average of at least five devices.

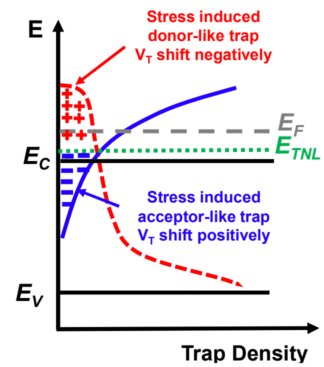

Fig. 19. Model of V_T shifts under PBS on InZnO FETs. This is the key understanding of this work.

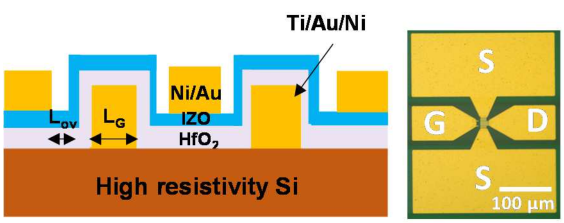

Fig. 20. Schematic and optical microscope image of RF circuits with GSG (ground-signal-ground) structure. In:Zn=5:1 film is employed for better contact and higher g_m. Highly resistive intrinsic silicon (>10 kΩ/□) is selected to reduce the substrate parasitics.

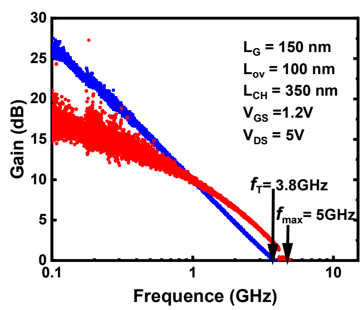

Fig. 21. Unilateral gain and h_{21} from a 0.35μm channel length InZnO RF transistor (In: Zn=5:1).

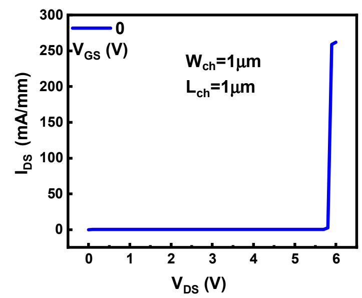

Fig. 22. Off-state breakdown measurement of InZnO transistor (In: Zn=1:1) limited by the ultrathin dielectric and the depleted InZnO layer.

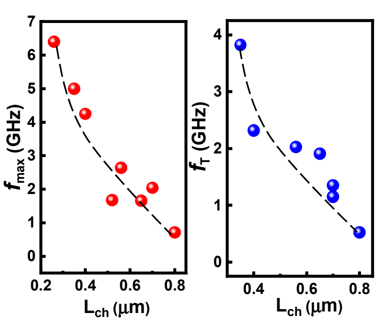

Fig. 23. Channel-length dependence of f_T and f_{max}.

	Thickness (nm)	Passivation Dielectric	Thermal Budget(°C)	Growth Method	L_{ch} (μm)	On-current (μA/μm)	V_{DS} (V)	SS (mV/dec)	On-off ratio	$\lvert V_{Bias}\rvert$ (V)	t_{stress} (s)	$\lvert\Delta V_T\rvert$ (mV)
In:Zn=1:1	3.5	No/6nm HfO_2	250	ALD	0.1	550	1	65	10^{11}	V_{TH}+3	1500	16
In:Zn=3:1	3.5	No/6nm HfO_2	250	ALD	0.1	1180	1	88	10^{10}	V_{TH}+3	1500	162
In:Zn=5:1	3.5	No/6nm HfO_2	250	ALD	0.1	1330	1	95	10^9	V_{TH}+3	1500	219
In_2O_3	3.5	No/3nm HfO_2	250	ALD	0.1	998	0.5	471*	10^3	V_{TH}+3	1500	349
IWO	7	Yes/5nm HfO_2	250	Sputter	0.1	195	1	105	10^9	V_{TH}+1.5	1000	770**
ITO	6	No/10nmAl_2O_3 +30nm HfO_2	100	Sputter	10	1.1	10	167	10^7	V_{TH}+6.3	1000	463
IGZO	15	No/12nm HfO_2	350	Sputter	10	10	1	125	10^8	V_{TH}+6	1500	400
Hf:IZO	40	Yes/200nm SiO_2	300	Sputter	50	1.2	5	1450	10^7	V_{TH}+20	7500	300
Mg:IGZO	30	No/200nm SiO_x	300	Sputter	50	0.4	20	461	10^8	V_{TH}+20	3600	6100

Table 1. Benchmark with state-of-the-art BEOL oxide semiconductor *back-gate* transistors in terms of channel thickness, channel length, thermal budget, on-current, drain voltage, SS, on-off ratio, and bias stability. *V_T of this device is very negative to lead to a large SS for a depletion-mode device. ** Negative bias stress is measured on a back-gate device. It improves to 100 mV on a dual-gate device.