Transient Thermal and Electrical Co-Optimization of BEOL Top-Gated ALD In_2O_3 FETs on Various Thermally Conductive Substrates Including Diamond

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***Abstract*—** In this work, we co-optimize the transient thermal and electrical characteristics of top-gated (TG), ultrathin, atomic-layer-deposited (ALD), back-end-of-line (BEOL) compatible indium oxide (In_2O_3) transistors on various thermally conductive substrates by visualization of the self-heating effect (SHE) utilizing an ultrafast high-resolution (HR) thermo-reflectance (TR) imaging system and overcome the thermal challenges through substrate thermal management and short-pulse measurement. At the steady-state, the temperature increase (ΔT) of the devices on highly resistive silicon (HR Si) and diamond substrates are roughly 6 and 13 times lower than that on SiO_2/Si substrate, due to the higher thermal conductivities (κ) of HR Si and diamond. Consequently, ultrahigh drain current (I_D) of 3.7 mA/μm at drain voltage (V_{DS}) of 1.4 V with direct current (DC) measurement is achieved with TG ALD In_2O_3 FETs on diamond substrate. Furthermore, transient thermal study shows that it takes roughly 350 and 300 ns for the devices to heat-up and cool-down to the steady-states, being independent on the substrate. The extracted time constants of heat-up (τ_h) and cool-down (τ_c) processes are 137 and 109 ns, respectively. By employing electrical short-pulse measurement with pulse width (t_{pulse}) shorter than τ_h, the SHE can be significantly reduced. Accordingly, a higher I_D of 4.3 mA/μm is realized with a 1.9-nm-thick In_2O_3 FET on HR Si substrate after co-optimization.

I. Introduction

Despite of the wide application in display industry [1], oxide semiconductors attract more interests recently as BEOL-compatible channel materials for monolithic 3-D integration [2–15]. Among them, ALD In_2O_3 is of great interest due to its outstanding properties such as wafer-scale uniformity, high carrier mobility, BEOL compatibility, ambient stability, angstrom-scale thickness control, atomically smooth surface, capability of conducting ultrahigh current, and conformality on 3-D surface structures [2–8]. Nevertheless, although TG devices are particularly desired for practical applications, the explorations of In_2O_3 FETs mostly focus on back-gated structure due to the challenges of defect induction during the formation of the high-k TG dielectric and severe SHE with high power density (PD) [7, 8]. The former fortunately can be partly resolved by low temperature ALD of the TG dielectric followed by a rapid thermal annealing (RTA) treatment in O_2 environment [5, 8] while the latter remains as a bottleneck.

In this work, an ultrafast high-resolution thermo-reflectance imaging system is introduced to visualize the transient and steady-state characteristic ΔT of TG In_2O_3 devices on different substrates to address the thermal issues. At the steady-states, the SHE is mitigated by a factor of 6 and 13 with HR Si and diamond substrate, respectively, compared to SiO_2/Si substrate. For the transient process, the extracted time constants τ_h and τ_c are roughly 137 and 109 ns, respectively. By resolving SHE, an ultra-high I_D of 3.7 mA/μm is realized with 2.5-nm-thick In_2O_3 devices on diamond substrate under DC measurement, and even higher I_D of 4.3 mA/μm is achieved with 1.9-nm-thick In_2O_3 transistors on HR Si substrate under pulse measurement.

II. Device Fabrication and Performance

Fig. 1 exhibits the schematic diagram of TG ALD In_2O_3 FETs. Different κ-value substrates including SiO_2/Si, sapphire, HR Si, and diamond from 1.5 to 2200 $W \cdot m^{-1} \cdot K^{-1}$, are used. After solvent cleaning, 1.6–2.5 nm In_2O_3 layer was grown by ALD at 225 °C, followed by an Ar/BCl_3 dry-etching step for device isolation. Next, 45 nm Ni was deposited as source/drain (S/D) contacts, and 7 nm HfO_2 top dielectric layer was formed by ALD at 120 °C. Finally, top-gate metal of 30/20 nm Au/Ni was deposited, followed by an RTA treatment at 250–300 °C in O_2 environment for 2–4 minutes. The overall thermal budget is as low as 300 °C.

Fig. 2 presents the electrical characteristics of a TG ALD In_2O_3 FET with channel length (L_{ch}) of 600 nm and thin channel thickness (T_{ch}) of 1.6 nm on SiO_2/Si substrate operated at enhancement-mode. The extracted threshold voltage (V_T) and subthreshold swing (SS) are 0.08 V and 150 mV/dec, respectively. ON/OFF ratio of 12 orders of magnitude is obtained due to the 3.0 eV wide bandgap of In_2O_3. Fig. 3 shows the I_D–V_{DS} curves of a similar device with a shorter L_{ch} of 80 nm, exhibiting a maximum I_D of 1 mA/μm at V_{DS} of 1 V. However, as the applied V_{DS} increases to 1.6 V as shown in Fig. 4, serious SHE happens due to low-κ of SiO_2, and the device becomes unstable. This is the thermal bottleneck for high I_D In_2O_3 FETs.

III. Steady-State Characterization

The ultrafast HR TR imaging equipment employed to systematically investigate and resolve the SHE is illustrated in Fig. 5. During the measurement, the device under test is applied by periodic V_{DS} pulses, high-speed LED pulses, and a constant V_{GS} bias. Besides, a synchronized charge coupled device (CCD) camera is equipped to capture the surface reflectance. Fig. 6 demonstrates its working mechanism. As V_{DS} pulses start/end, the device is turned ON/OFF and accordingly self-heat-up/cool-down, and TR signals are captured as active/passive images after the steady-state is reached. This process is repeated numerous times, and the

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difference between the active and passive images is averaged consequently and transformed into a temperature scale through dividing by the calibrated thermal coefficient of the surface material ($C_{TH} = -2.5\times10^{-4}$ K^{-1} [16]–[18]) to obtain the final HR ΔT distribution image at the steady-state as shown in Fig. 7.

Fig. 8 presents the observed ΔT distribution of the TG In_2O_3 transistors with identical structure and dimensions but different substrates around the channel region. Clearly, the one on SiO_2/Si substrate is the most self-heated while the one on diamond substrate is the least. The cross-sections of the ΔT along the channel width (W_{ch}) direction normalized by PD is demonstrated in Fig. 9 where the PD is calculated by ($I_D\times V_{DS}$) / ($L_{ch}\times W_{ch}$). The maximum ΔT of the devices with individual substrate and different PD is plotted in Fig. 10 where a linear relationship is obtained despite of the substrate. The inversed slopes of the regression lines indicate the capability of the substrate to dissipate the generated Joule heat in the channel. As implied in Fig. 11, the higher κ of the substrate is, the lower the maximum normalized ΔT will be. Sapphire (κ = 40 $W\cdot m^{-1}\cdot K^{-1}$ [19]), HR Si (κ = 140 $W\cdot m^{-1}\cdot K^{-1}$ [20]), and diamond (κ = 2200 $W\cdot m^{-1}\cdot K^{-1}$ [21]) substrates have ΔT reduction by factors of 2.5, 6, and 13, respectively, compared with SiO_2/Si substrate with thick SiO_2 (κ = 1.5 $W\cdot m^{-1}\cdot K^{-1}$ [22]).

Moreover, heat transfer simulation with a finite-element method is also carried out through COMSOL. Fig. 12 shows the model and mesh build-up where the same structure and dimensions are designed as the tested devices, and the outcome is presented in Fig. 13. For clearer comparison, Fig. 8(a) is re-plotted as Fig. 14 with similar fashion and scale to Fig. 13, and a false-color image of a fabricated TG In_2O_3 transistor around the channel region is illustrated in Fig. 15 for a better SHE visualization. Noticeably, the simulation and TR measurement results are in great agreement as illustrated in Fig. 16. Thermal studies motivate to build up an In_2O_3 transistor with T_{ch} of 2.5 nm and L_{ch} of 100 nm on diamond substrate to alleviate SHE. Fig. 17 presents its DC output and transfer characteristics where an ultrahigh I_D of 3.7 mA/μm is realized at V_{DS} of 1.4V without observable SHE even with high PD, in great contrast to Fig. 4. The extracted field-effect mobility (μ_{FE}) and SS are 55.6 $cm^2\cdot V^{-1}\cdot s^{-1}$ and 185 mV/dec, respectively.

IV. Transient Characterization

Although diamond with ultrahigh κ is an excellent heat sinker, it is not economically affordable for mass production. TG transistors on Si substrate are much more practical. To further mitigate the SHE on Si substrate, detailed transient thermal characteristics are studied. Fig. 18 illustrates the working mechanism for transient thermal characteristics. Similar to steady-state measurements, an active and a passive image are captured by the synchronized CCD camera in each period. By setting the active image to be captured at a specific timing, the ΔT distribution of that moment can be obtained through the same process shown in Fig. 7. To experimentally observe the time-resolved self-heat-up and cool-down processes, the V_{DS} pulses are set to start at 0 ns and end at 600 ns. From 0 ns to 1200 ns, TR images are taken every 50 ns as presented in Fig. 19. The maximum ΔT of each moment of the devices with SiO_2/Si and HR Si substrates are summarized in Fig. 20. It takes roughly 350 and 300 ns to reach steady-states for heat-up and cool-down, independent on the substrate. Fig. 21 exhibits the time constant extraction where 137 and 109 ns are acquired for heat-up (τ_h) and cool-down (τ_c), respectively. τ_h and τ_c are related to intrinsic thermal properties of In_2O_3.

With the understanding of its transient thermal characteristics, short-pulse electrical co-optimization is proposed to alleviate SHE. As shown in Fig. 22, in each period, the transistors under test will only be turned ON for t_{pulse} of time in which the first t_{delay} of time is used for bias stabilization, and the following t_{meas} of time is used for current measurement. Fig. 23 exhibits the I_D–V_{DS} curves of a TG In_2O_3 FET with T_{ch} of 1.9 nm and L_{ch} of 80 nm on HR Si substrate. The empty and solid symbols represent DC and pulse measurement results, and an ultrahigh I_D of 4.3 mA/μm is achieved at high V_{DS} of 3.2 V. In great contrast to Fig. 4, even with such high PD on atomically thin channel, there is no observable SHE since the t_{pulse} of 120 ns is even shorter than τ_h. The key fact is that the electrical response is much faster than the thermal response. As τ_h and τ_c are independent of the heating amplitude [23], ΔT over time during the pulse measurement can be calculated. Fig. 24 illustrates the transient ΔT of the device under the highest PD of DC and pulse measurement in Fig. 23. The maximum ΔT of pulse measurement (blue curve) is lower than 120 K even though its steady-state is higher than 200 K. Short-pulse electrical measurement can significantly reduce SHE and probe the potential of the material and device performance.

V. Conclusion

In summary, transient thermal and electrical properties of TG ALD In_2O_3 FETs on various thermally conductive substrates are co-optimized employing an ultrafast HR TR imaging technique to unveil the problematic SHE. By using HR Si substrate and electrical short-pulse measurement, ultra-high I_D of 4.3 mA/μm is achieved on atomically thin In_2O_3 devices without observable SHE. This work demonstrates that the understanding of both thermal and electrical transient dynamics is of importance to resolve thermal bottleneck on atomically thin oxide semiconductor devices.

Acknowledgment

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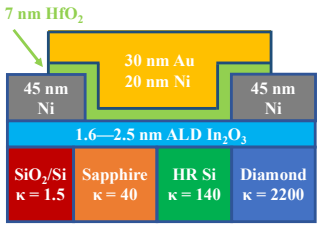

Fig. 1. Device schematic of a TG ALD In_2O_3 FET with various thermally conductive substrates. The unit of thermal conductivity (κ) is $W{\cdot}m^{-1}{\cdot}K^{-1}$.

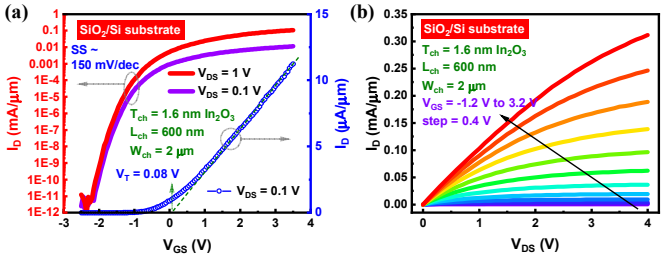

Fig. 2. (a) Transfer and (b) output characteristics of a TG ALD In_2O_3 FET with long L_{ch} of 600 nm and thin T_{ch} of 1.6 nm on a SiO_2/Si substrate operated at enhancement-mode (E-mode).

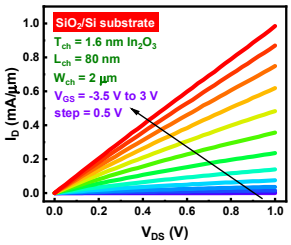

Fig. 3. Output characteristics of a TG ALD In_2O_3 FET with short L_{ch} of 80 nm on a SiO_2/Si substrate.

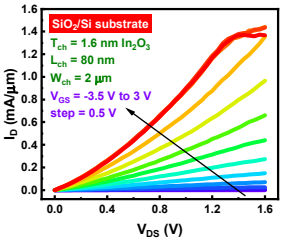

Fig. 4. Severe SHE deteriorates the device performance of a TG ALD In_2O_3 FET with high PD.

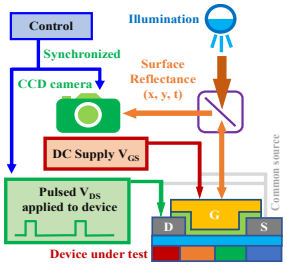

Fig. 5. Schematic illustration of the ultrafast high-resolution TR imaging system setup.

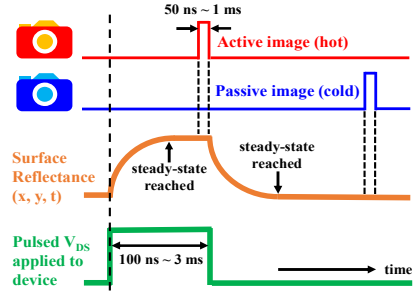

Fig. 6. Working mechanism of the ultrafast high-resolution TR imaging equipment in time domain.

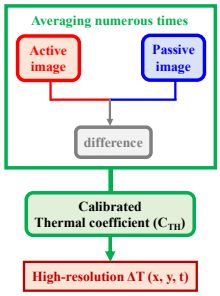

Fig. 7. Transformation from TR signal to a temperature scale.

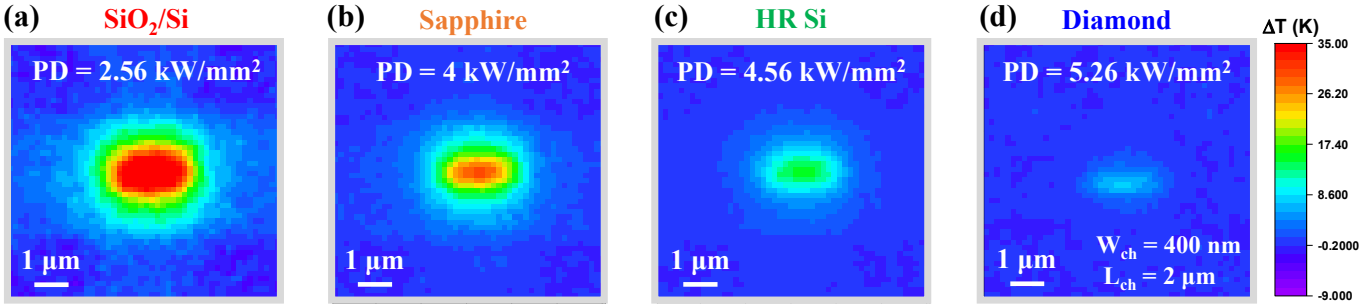

Fig. 8. SHE visualization of In_2O_3 FETs in experiments with substrates of (a) SiO_2/Si, (b) sapphire, (c) highly resistive Si, and (d) diamond with various PD.

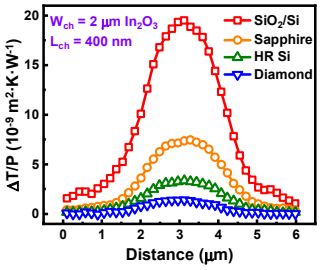

Fig. 9. Cross-sections of PD-normalized ΔT of TG ALD In_2O_3 FETs with different substrates.

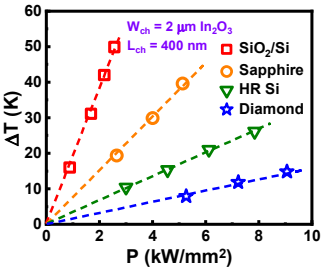

Fig. 10. ΔT extraction of TG ALD In_2O_3 devices with different substrates and power densities.

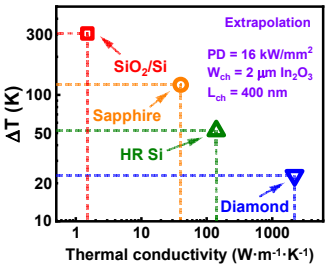

Fig. 11. Comparison of the extrapolated ΔT with different substrates given a constant PD.

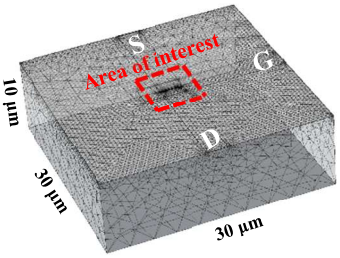

Fig. 12. Model design and mesh build-up of a TG In_2O_3 device for heat-transfer simulation with a finite-element method.

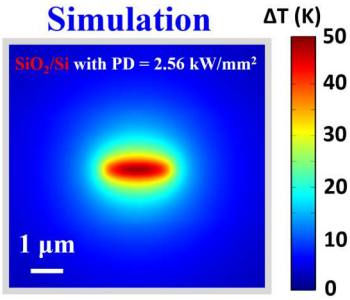

Fig. 13. Simulation outcome of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

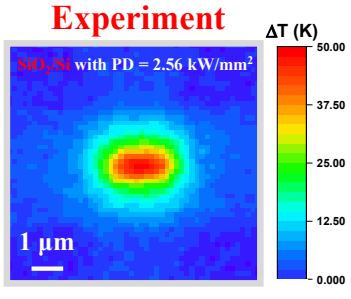

Fig. 14. TR measurement of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

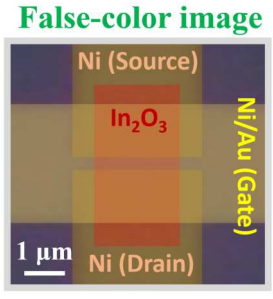

Fig. 15. A false-color top-view image of a fabricated TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

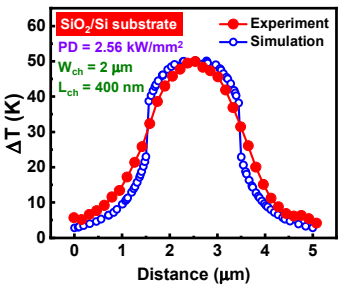

Fig. 16. Cross-sections of the simulated and experimental results of ΔT distribution.

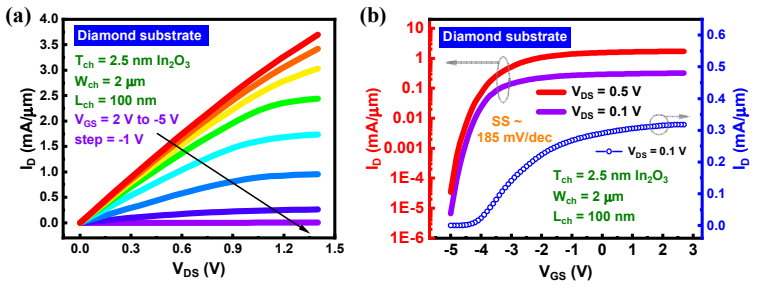

Fig. 17. Output and transfer characteristics of an In_2O_3 FET with L_{ch} of 100 nm and T_{ch} of 2.5 nm on a diamond substrate, performing ultrahigh I_D of 3.7 mA/μm under DC condition.

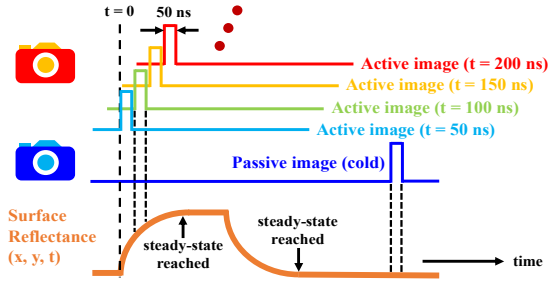

Fig. 18. Working mechanism of transient thermal property study with an ultrafast high-resolution TR imaging system.

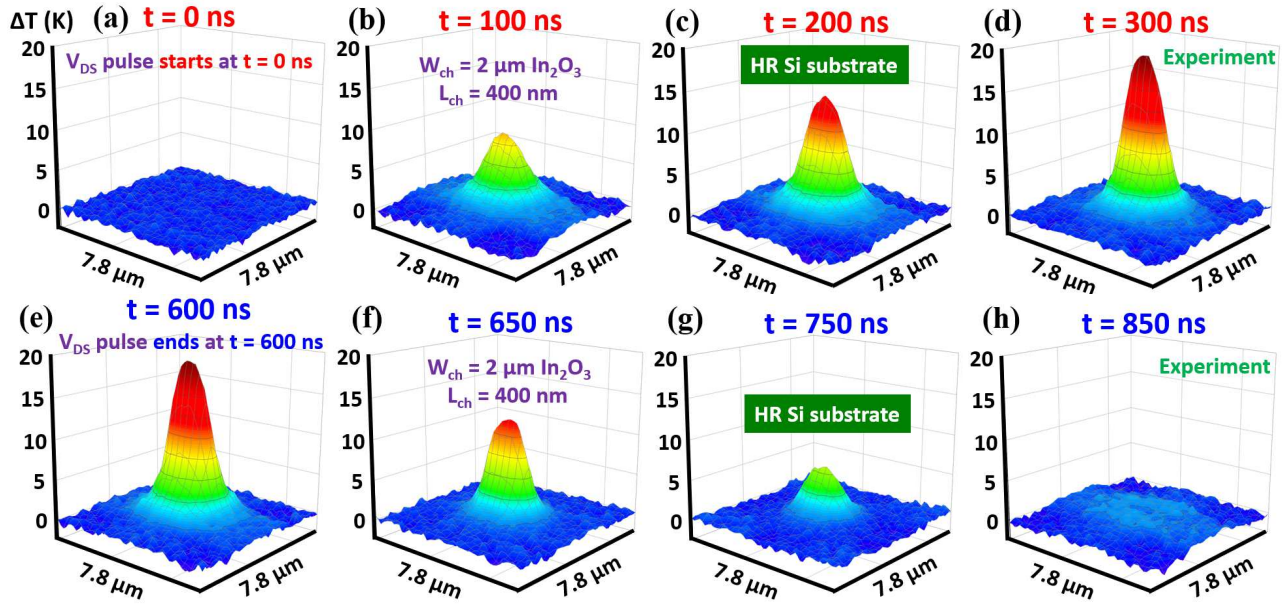

Fig. 19. Transient TR characteristics of a TG ALD In_2O_3 FET on HR Si substrate. The device was self-heated-up by applying a V_{DS} pulse starting at 0 ns and ending at 600 ns. (a)-(d) demonstrate the heat-up process while (e)-(h) demonstrate the cool-down process.

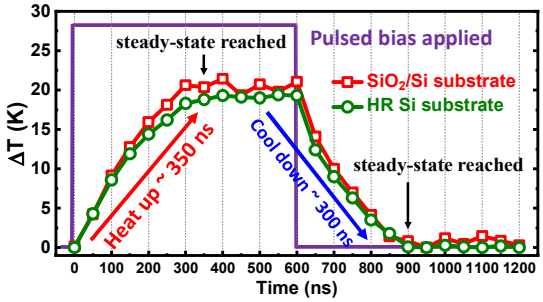

Fig. 20. Transient ΔT results and comparison with different substrates. Roughly 325 ns is needed to reach steady-state in both cases.

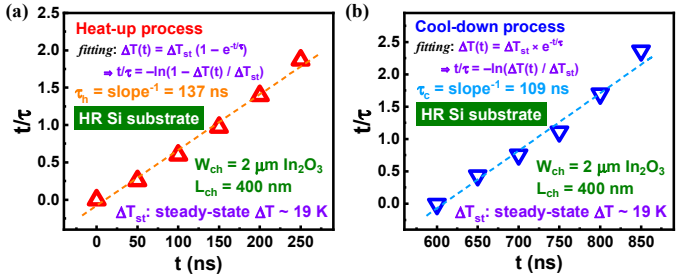

Fig. 21. Time constant extraction of (a) heat-up and (b) cool-down processes from the transient ΔT measurement results with HR Si substrate of Fig. 20. The t/τ values are obtained by plugging the measured individual ΔT(t) values into the indicated formulas.

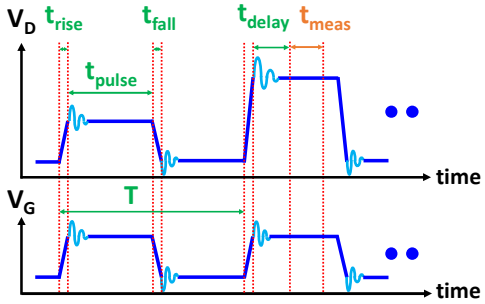

Fig. 22. Diagram sketch of pulse measurement setup in time domain. The light blue damping illustrates the bias stabilization process after being set to desired values.

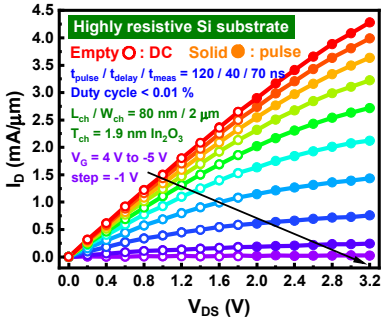

Fig. 23. Output characteristics of a TG ALD In_2O_3 FET with short L_{ch} of 80 nm and T_{ch} of 1.9 nm on HR Si substrate achieving extremely high I_D up to 4.3 mA/μm.

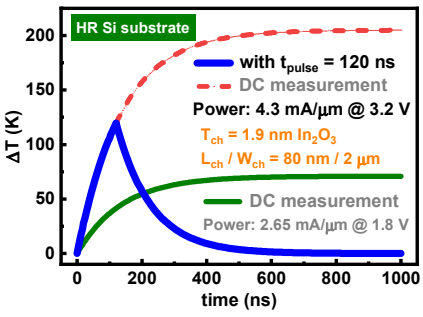

Fig. 24. Transient ΔT calculation of DC and pulse measurements under respective highest PD in Fig. 23.