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# Characterization of Interface and Bulk Traps in Ultrathin Atomic Layer-Deposited Oxide Semiconductor MOS Capacitors With $HfO_2/In_2O_3$ Gate Stack by C-V and Conductance Method

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Oxide semiconductors have attracted revived interest for complementary metal–oxide–semiconductor (CMOS) back-end-of-line (BEOL) compatible devices for monolithic 3-dimensional (3D) integration. To obtain a high-quality oxide/semiconductor interface and bulk semiconductor, it is critical to enhance the performance of oxide semiconductor transistors. Atomic layer-deposited (ALD) indium oxide ($In_2O_3$) has been reported with superior performance such as high drive current, high mobility, steep subthreshold slope, and ultrathin channel. In this work, the interface and bulk traps in the MOS gate stack of ALD $In_2O_3$ transistors are systematically studied by using the C–V and conductance method. A low EOT of 0.93 nm is achieved directly from the accumulation capacitance in C–V measurement, indicating a high-quality gate oxide and oxide/semiconductor interface. Defects in bulk $In_2O_3$ with energy levels in the subgap are confirmed to be responsible for the conductance peak in $G_P/\omega$ versus $\omega$ curves by TCAD simulation of C–V and G–V characteristics. A high n-type doping of $1\times10^{20}/cm^3$ is extracted from C–V measurement. A high subgap density of states (DOS) of $3.3\times10^{20}\ cm^{-3}\ eV^{-1}$ is achieved using the conductance method, which contributes to the high n-type doping and high electron density. The high n-type doping further confirms the capability of channel thickness scaling because the charge neutrality level aligns deeply inside the conduction band.

**Keywords: indium oxide, oxide semiconductors, thin-film transistors, atomic layer deposition, interface and bulk traps, conductance method**

## INTRODUCTION

Oxide semiconductors (Nomura et al., 2004; Kamiya et al., 2010) are widely used in thin-film transistors (TFTs) as channel materials and are considered as promising candidates for complementary metal–oxide–semiconductor (CMOS) back-end-of-line (BEOL) compatible transistors for monolithic three-dimensional (3D) integration. Indium oxide ($In_2O_3$) (Si et al., 2021a; Si et al., 2021b; Si et al., 2021c; Si et al., 2021d) or doped $In_2O_3$ (Matsubayashi et al., 2015; Li

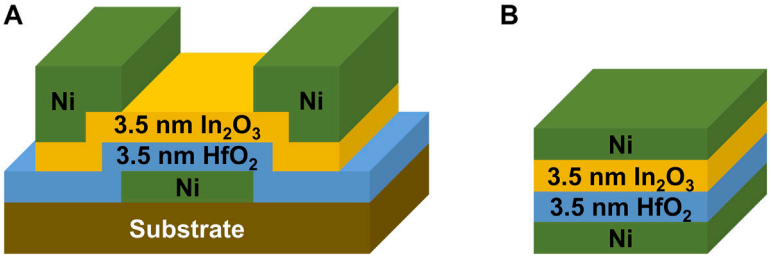


**FIGURE 1 |** Schematic diagram of **(A)** an ALD $In_2O_3$ transistor with 3.5 nm $In_2O_3$ as the channel semiconductor and 3.5 nm $HfO_2$ as the gate dielectric; **(B)** the gate stack capacitor fabricated together with the ALD $In_2O_3$ transistor.

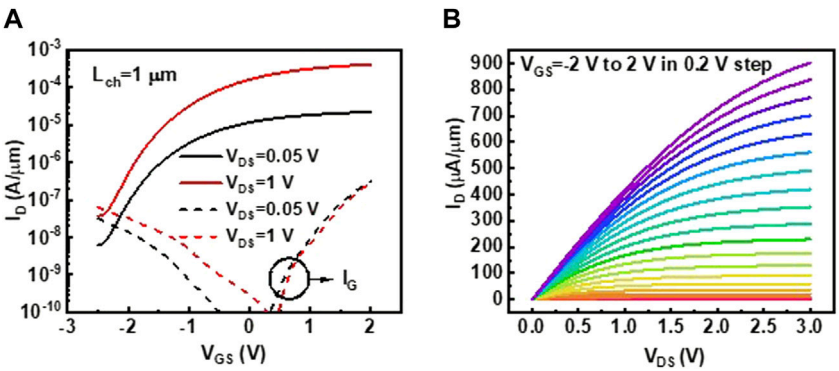


**FIGURE 2 | (A)** $I_D$–$V_{GS}$ and **(B)** $I_D$–$V_{DS}$ characteristics of an $In_2O_3$ transistor with $L_{ch}$ of 1 μm and $T_{ch}$ of 3.5 nm, where in **(A)**, the solid lines are $I_D$–$V_{GS}$ and the dotted lines are $I_G$–$V_{GS}$ curves.

et al., 2019; Chakraborty et al., 2020; Fujiwara et al., 2020; Li et al., 2020; Samanta et al., 2020; Han et al., 2021) deposited by both sputtering and atomic layer deposition (ALD) are being investigated due to high mobility, low variability, wide bandgap, and high stability. Recently, ALD-based oxide semiconductors have attracted much attention due to the atomically smooth surface, low thermal budget, precise thickness control down to sub-1 nm, and capability of depositing a conformal film on 3D structures, achieving high-performance devices with maximum drain current >2 A/mm, high electron mobility >100 $cm^2$/Vs, high on/off ratio > $10^{10}$, and near-ideal subthreshold slope (SS) down to 63.8 mV/dec at room temperature, making them leading candidates as channel semiconductors for monolithic 3D integration (Si et al., 2021a; Si et al., 2021b; Si et al., 2021c; Si et al., 2021d).

$In_2O_3$ has a charge neutrality level (CNL) at above 0.4 eV above the conduction band ($E_C$). It was understood that this is the origin of high electron density and low contact resistance in an atomically thin channel (Si et al., 2021a). Such high electron density is directly associated with the subgap density of states (DOS) in $In_2O_3$. Meanwhile, in oxide semiconductor-based transistors, the electrical performance and reliability are closely connected with the subgap DOS over the bandgap. Therefore, it is important to extract and study the impact of trap states. However, the interface and bulk traps in ultrathin ALD oxide semiconductor devices have not been systematically studied. Capacitance–voltage (C–V) measurements and the conductance method are commonly used to extract interface trap density ($D_{it}$) in MOS capacitors, which is used to evaluate the characteristics of interface and bulk traps in ALD $In_2O_3$ MOS capacitors.

In this work, the interface and bulk traps in the MOS gate stack of ALD $In_2O_3$ transistors are systematically studied by using the C–V and conductance method. ALD $In_2O_3$ transistors and MOS capacitors with 3.5 nm $HfO_2$ as the gate insulator and 3.5 nm $In_2O_3$ as the channel semiconductor are fabricated, achieving a low equivalent oxide thickness (EOT) of 0.93 nm, indicating a high-quality gate oxide and oxide/semiconductor interface. The C–V and conductance method were utilized to study the properties of interface and bulk trap states in the gate stack of $In_2O_3$ transistors. A high n-type doping of $1 \times 10^{20}$/$cm^3$ is achieved by C–V measurement. This is further confirmed by the high conductance peak of $7.6 \times 10^{-6}$ S s/$cm^2$, corresponding to a high subgap DOS of $3.3 \times 10^{20}$ $cm^{-3}$ $eV^{-1}$, which contributes to the high n-type doping and high electron density. The high electron density is because CNL aligns deeply inside the $E_C$, which is speculated to be related to In atoms, thus In-based semiconductors tend to have a high electron density. TCAD simulation is used to study the impact of the interface traps and bulk traps on C–V curves and conductance peaks of the MOS capacitors. It is found that bulk traps across the ultrathin body contribute to the large frequency dispersion in high $V_{GS}$ and the large conductance peak in $G_P/\omega$ versus ω characteristics.

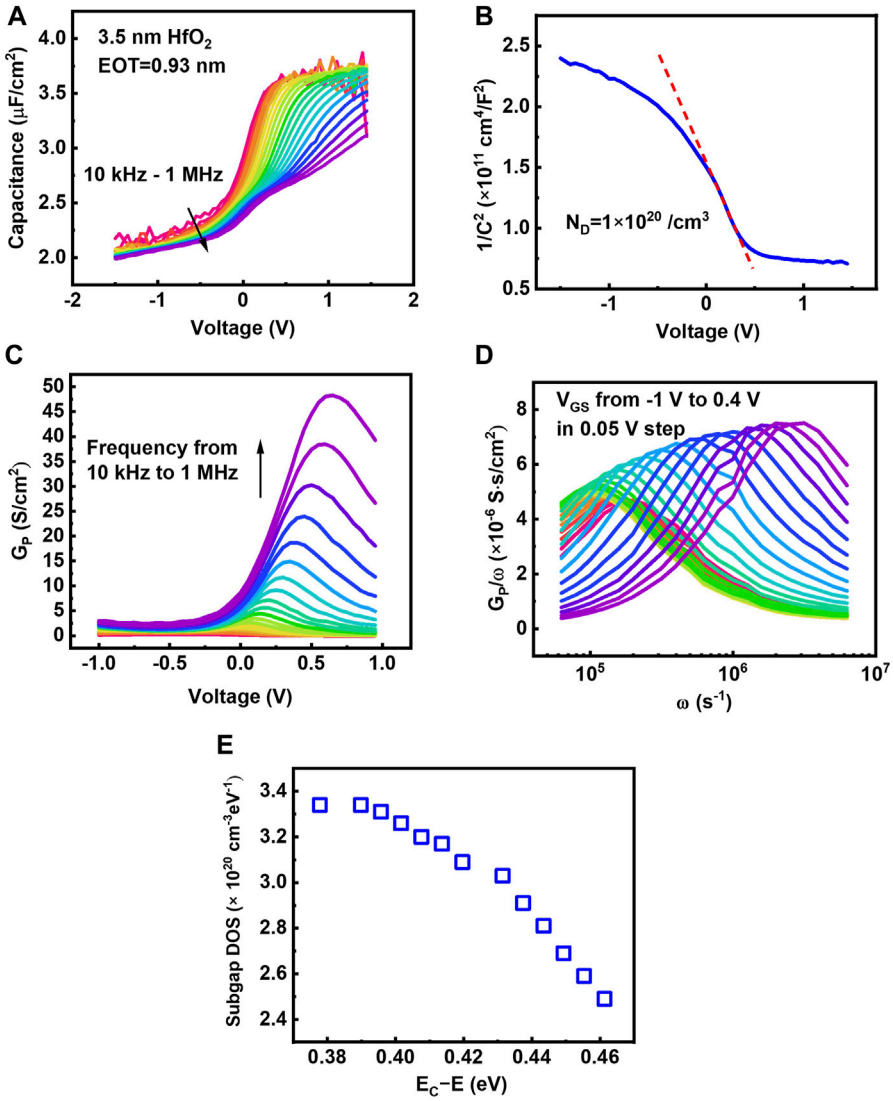


**FIGURE 3 | (A)** C–V, **(B)** $1/C^2$ versus voltage, **(C)** $G_P$ versus voltage, and **(D)** $G_P/\omega$ versus $\omega$ characteristics of the Ni/3.5 nm $In_2O_3$/3.5 nm $HfO_2$/Ni gate stack. **(E)** Subgap DOS distribution extracted by using the conductance method.

## EXPERIMENTS

**Figures 1A,B** show the schematic diagram of an ALD $In_2O_3$ transistor and an MOS capacitor with the same gate stack fabricated together with the transistor. The gate stack contains 40 nm Ni as the gate metal, 3.5 nm $HfO_2$ as the gate insulator, 3.5 nm $In_2O_3$ as the semiconductor channel, and 80 nm Ni as the source/drain (S/D) contacts. The area of MOS capacitors used in this work is 60 μm by 60 μm. The detailed fabrication process of the $In_2O_3$ transistors is similar to that used in Si et al. (2021c). The fabrication process starts with a standard cleaning of the p + Si substrate with 90 nm $SiO_2$ grown thermally for device isolation. Then a bilayer photoresist lithography process is conducted for the sharp lift-off of the 40 nm Ni gate metal by e-beam evaporation. 3.5 nm $HfO_2$ was then deposited by ALD at 200°C, using $[(CH_3)_2N]_4Hf$ (TDMAHf) and $H_2O$ as Hf and O precursors. Then, 3.5 nm $In_2O_3$ was also deposited by ALD at 225°C, using $(CH_3)_3In$ (TMIn) and $H_2O$ as In and O precursors and $N_2$ as the carrier gas. After that, 80 nm Ni was deposited by e-beam evaporation as S/D contacts, patterned by electron beam lithography. The overlap between the gate and S/D electrodes is 2 μm. The devices were annealed in $O_2$ at 200°C for 4 min. No obvious interdiffusion between $HfO_2/In_2O_3$ and $In_2O_3$/Ni is observed in a high-resolution transmission electron microscope (HRTEM), at least at the resolution of ~nm, as demonstrated in our previous work (Si et al., 2022) using a similar process. I–V measurements were performed using a Keysight B1500 semiconductor analyzer, while C–V and conductance measurements were conducted using an Agilent E4980A LCR meter.

The simulations were conducted on the gate stack capacitor to investigate the effects of trap states using TCAD tools. A two-

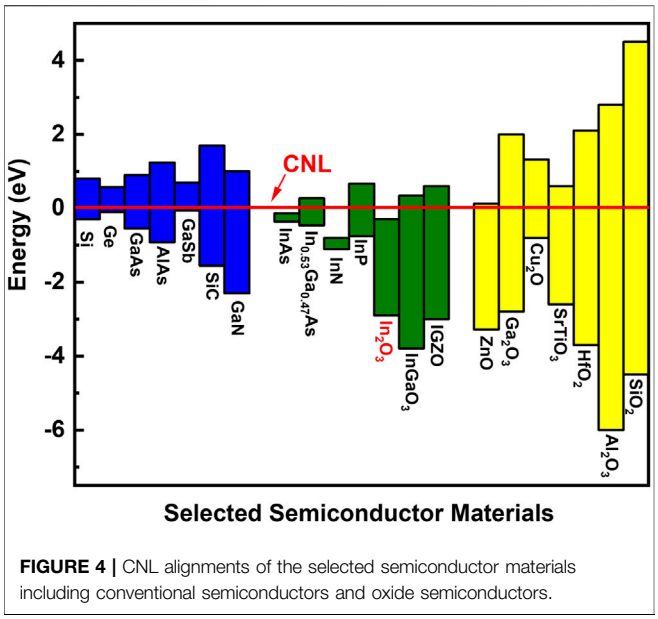


**FIGURE 4 |** CNL alignments of the selected semiconductor materials including conventional semiconductors and oxide semiconductors.

dimensional gate stack capacitor, with 3.5 nm $HfO_2$ as the gate dielectric, 3.5 nm $In_2O_3$ as the semiconductor, and Ni as the top and bottom electrodes, was used for the TCAD simulation, which is the same as the Ni/$In_2O_3$/$HfO_2$/Ni capacitor used in the experiment. During simulation, all structural dimensions and material parameters were kept unchanged. Some typical physical models for MOS capacitor simulation were utilized. To be specific, the CVT transverse field-dependent mobility model and a lateral electric field-dependent model were used for electrons and holes by specifying CVT and FLDMOB, respectively, in the model statement, while Auger recombination was also considered by specifying Auger in the model statement. In addition, the defects model and intdefects model were also used to specify interface trap states at the $In_2O_3$/$HfO_2$ interface and bulk trap states in the $In_2O_3$ layer, respectively. For both bulk traps and interface traps, one tail distribution of acceptor-like traps at the conduction band edge, one tail distribution of donor-like traps at the valence band edge, and one deep-level Gaussian distribution of traps were specified (Kamiya et al., 2010; Jankovic, 2012), with NTA, NTD, and NGA to determine the peak density of these three types of traps, respectively. All traps are uniformly distributed in space, for both interface and bulk traps. C–V and G–V characteristics of the MOS capacitor were simulated to investigate the impacts of interface traps and bulk traps.

## RESULTS AND DISCUSSION

**Figure 2A** shows the $I_D$–$V_{GS}$ characteristics at $V_{DS}$ of 0.05 and 1 V of an ALD $In_2O_3$ transistor with a channel length ($L_{ch}$) of 1 μm and a channel thickness ($T_{ch}$) of 3.5 nm. The gate leakage current ($I_G$) is also presented in **Figure 2A**, which is relatively high due to the highly scaled EOT, resulting in the relatively low on/off ratio and large subthreshold slope (SS). SS down to 63.8 mV/dec was achieved on ALD $In_2O_3$ transistors at room temperature, corresponding to a low $D_{it}$ of $6.3 \times 10^{11}$ $cm^{-2}$ $eV^{-1}$ (Si et al., 2021d). The on/off ratio and SS of the device can be further improved by threshold voltage ($V_T$) engineering. Field-effect mobility ($\mu_{FE}$) is extracted at $V_{DS}$ of 0.05 V using maximum $g_m$ to be 46 $cm^2$/V·s. **Figure 2B** shows the $I_D$–$V_{DS}$ characteristics at $V_{GS}$ from −2 to 2 V of the same ALD $In_2O_3$ transistor as in **Figure 2A**. A maximum drain current of 903 μA/μm is achieved at $V_{DS}$ of 3 V, showing well-behaved $I_D$ saturation characteristics at high $V_{DS}$ due to a drain side pinch-off.

The transport properties of oxide semiconductors, especially indium–gallium–zinc oxide (IGZO), are known to be closely related to the defect states in the bandgap (subgap states) (Kamiya and Hosono, 2010). Here, C–V and G–V methods were adopted to study the characteristics of these defect states in ALD $In_2O_3$ MOS capacitors. The top Ni electrode of the capacitor has no direct overlap with the p + Si substrate, and so the p + Si layer in the substrate will not show any parasitic role when measuring C–V characteristics. **Figure 3A** shows the C–V measurements of the gate stack capacitor fabricated together with the transistor in **Figure 2**, the structure of which is shown in **Figure 1B**. An accumulation capacitance of 3.7 μC/$cm^2$ is achieved, corresponding to an EOT of 0.93 nm. A dielectric constant of 15 for $HfO_2$ is achieved assuming that oxide capacitance ($C_{ox}$) is close to the accumulation capacitance, suggesting a high-quality oxide/semiconductor interface. The large frequency dispersion at high $V_{GS}$ is because of electron generation and recombination from the subgap defect states. The C–V curve also shows a minimum capacitance of 2.0 μC/$cm^2$ at low voltage. At low voltage, $In_2O_3$ is depleted so that the minimum capacitance can be estimated as $C_{ox}$ and the semiconductor capacitance ($C_S$) in series, where $C_S = \epsilon_S\epsilon_0/T_{ch}$ and $\epsilon_0$ is $8.85 \times 10^{-14}$ F/cm as vacuum permittivity. As a result, $\epsilon_S$ of 20 is obtained, which is higher than about 8.9 by optical measurement (Hamberg and Granqvist, 1986). The overestimation of $C_S$ is caused by nonideal effects such as $In_2O_3$ at −1.5 V might not be fully depleted, Maxwell–Wagner effect, and the response from defect states.

The subgap defect states can be divided into two groups: shallow donors that contribute to the conducting electron or other defect states such as deep localized states (Jankovic, 2012). The doping concentration ($N_D$) can be extracted from $1/C^2$ versus voltage characteristics according to $N_D = \frac{2}{q\epsilon_S\epsilon_0 d(1/C^2)/dV}$ (Schroder, 2006), where q is the elementary charge, and $\epsilon_S$ of 8.9 from optical measurement is used. $N_D$ of $1 \times 10^{20}$/$cm^3$ is achieved, as shown in **Figure 3B**, which can be approximated as the density of shallow donor states. These defects are most likely to be oxygen vacancies as they are known to be shallow donors in oxide semiconductors such as IGZO (Jankovic, 2012). A 2D electron density ($n_{2D}$) considering $T_{ch}$ of 3.5 nm is calculated to be $3.5\times10^{13}$/$cm^2$. Such a high $n_{2D}$ also indicates a low $D_{it}$ at the oxide/semiconductor interface.

To evaluate the total density of subgap DOS, the conductance method is applied. **Figure 3C** shows the $G_P$ versus voltage characteristics at different frequencies measured simultaneously with the C–V curve as in **Figure 3A**, where $G_P$ decreases at high voltages suggesting that the impact of leakage current on $G_P$ is small compared to the impact of trap states. $G_P/\omega$ versus ω characteristics are calculated from G–V data and $C_{ox}$ from C–V data, as shown in **Figure 3D**, exhibiting a high conductance peak of $7.6 \times 10^{-6}$ S s/$cm^2$, corresponding to a high subgap DOS of $1.2 \times 10^{14}$ $cm^{-2}$ $eV^{-1}$ or 3.3

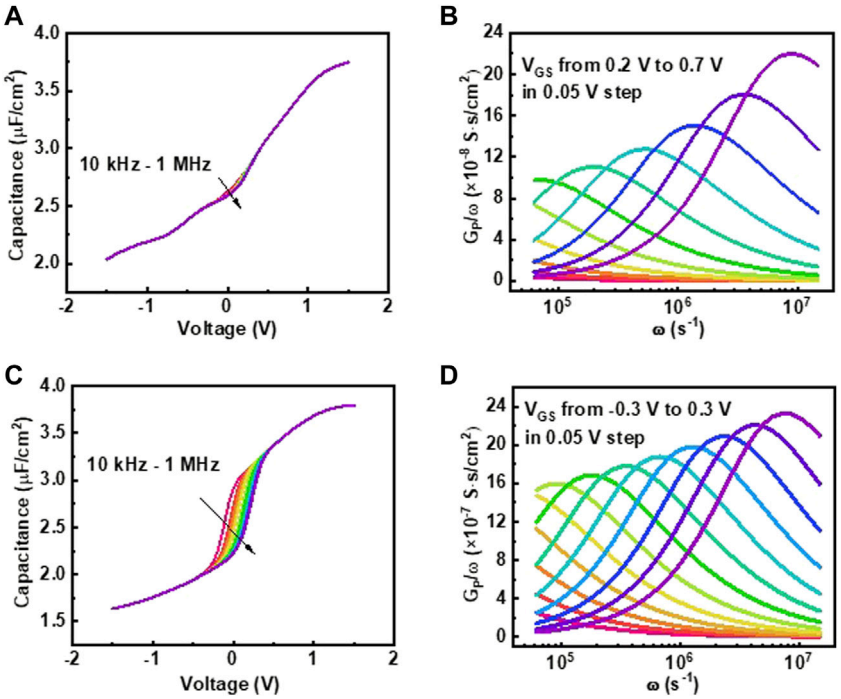


**FIGURE 5 |** Simulated **(A)** C–V and **(B)** $G_P/\omega$ versus ω characteristics of the gate stack capacitor with the same structure as in **Figure 1B**, using $D_{it}$ of $10^{12}$ $cm^{-2}$ $eV^{-1}$. Simulated **(C)** C–V and **(D)** $G_P/\omega$ versus ω characteristics of the gate stack capacitor with the same structure as in **Figure 1B**, using $D_{it}$ of $10^{13}$ $cm^{-2}$ $eV^{-1}$.

× $10^{20}$ $cm^{-3}$ $eV^{-1}$ normalized by $T_{ch}$. Note that the conductance peaks here appear at around V = 0, so that it is not affected by the gate leakage current. **Figure 3E** shows the subgap DOS versus energy level extracted from $G_P/\omega$ versus ω data in **Figure 3D**, with energy mapping obtained from the peak frequency (Brammertz et al., 2007). The conductance measurement further confirms the high subgap DOS in ALD $In_2O_3$, which contributes to the high carrier density.

Note that the high electron density in the ultrathin ALD $In_2O_3$ film is critical to achieve high $I_D$ in an ultrathin semiconducting film. In other words, semiconducting films with CNL alignment deeply inside $E_C$ are more suitable for devices with an ultrathin body in the nanometer scale. Such CNL alignment ensures a low Schottky barrier and a high carrier density, even considering the impact of quantum confinement effects. The CNL alignments of some selected semiconductor materials are plotted in **Figure 4**, including conventional semiconductors such as Si/Ge/III–V and oxide semiconductors such as IGZO (Mönch, 1997; Robertson and Falabretti, 2006; Ye, 2008; Robertson and Clark, 2011; Wager et al., 2012; Swallow et al., 2021). As we can see, in both conventional semiconductors and oxide semiconductors, materials with In atoms tend to have CNL closer to the vacuum level with higher electron density. Therefore, to look for materials deeper inside $E_C$ and with reasonable bandgap is the key to realize high-performance semiconducting materials with ultrathin bodies.

TCAD simulations are conducted to investigate the impact of defects at the oxide/semiconductor interface and in bulk $In_2O_3$ on the C–V and G–V characteristics of ALD $In_2O_3$ MOS capacitors using the same structure as in **Figure 1B**. **Figure 5** shows TCAD simulation results investigating the impact of interface trap states at the $HfO_2/In_2O_3$ interface on C–V measurements and the conductance method. The interface trap density at the $HfO_2/In_2O_3$ interface has been estimated to be 6.3 × $10^{11}$ $cm^{-2}$ $eV^{-1}$ with the subthreshold method (Si et al., 2021d). In this work, SS is much larger because of the impact of gate leakage, but the $D_{it}$ at the $HfO_2/In_2O_3$ interface is expected to be similar to the aforementioned value and independent of channel thickness because of the similar atomic configuration. For the TCAD simulation, a U-shape interface trap states distribution was specified at the $HfO_2/In_2O_3$ interface of the gate stack (Schulz, 1983; Jankovic, 2012), with a minimum $D_{it}$ of $10^{12}$ $cm^{-2}$ $eV^{-1}$ for **Figures 5A,B** and $10^{13}$ $cm^{-2}$ $eV^{-1}$ for **Figures 5C,D**. Acceptor-like and donor-like traps are in tail distribution at the valence band and conduction band edges, respectively. **Figure 5A** and **Figure 5C** present the simulated C–V data of the gate stack capacitor, exhibiting frequency dispersion in the depletion region and no obvious frequency dispersion in the accumulation region. **Figures 5B,D** show the corresponding $G_P/\omega$ versus ω characteristics, showing a much lower conductance peak than the experimental data, even with quite large $D_{it}$. Both C–V and G–V simulation results confirm that interface traps at the $HfO_2/In_2O_3$ interface are not the main reason for the C–V frequency dispersion in the depletion region and high conductance peak extracted from the experiments. Therefore, the frequency dispersion and high conductance peak are most likely contributed by the bulk traps inside $In_2O_3$.

**Figure 6** shows the TCAD simulation results investigating the impact of the bulk trap states in the $In_2O_3$ layer on C–V and G–V characteristics. The bulk trap distribution in the semiconductor layer

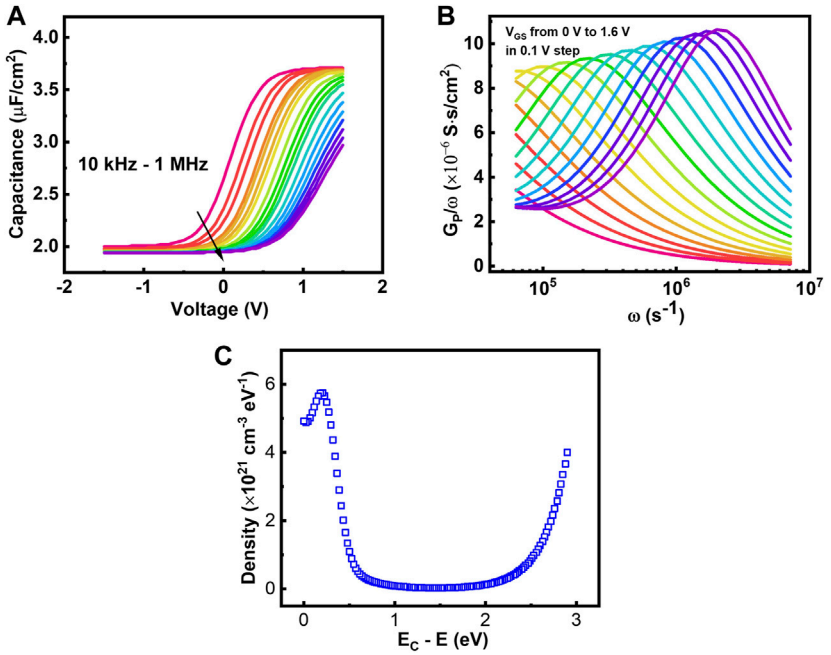


**FIGURE 6 |** Simulated **(A)** C–V and **(B)** $G_P/\omega$-ω characteristics of the gate stack, considering the impact of bulk traps. **(C)** Bulk trap state distribution used in the simulation.

for simulation is shown in **Figure 6C**, considering trap states with both Gaussian and tail distributions (Kamiya et al., 2010). The bulk trap levels below mobility edge have a peak density of nearly $6\times10^{21}$ $cm^{-3}$ $eV^{-1}$. **Figure 6A** shows simulated C–V characteristics of the gate stack capacitor, showing a significant frequency dispersion in the accumulation region. **Figure 6B** shows the corresponding $G_P/\omega$ versus ω data. A high conductance peak of about $1.1 \times 10^{-5}$ S·s/$cm^2$ can be extracted from the simulation results. Both simulated C–V characteristics and $G_P/\omega$-ω characteristics are highly consistent with the experimental results, which proves that bulk traps of more than $10^{21}$ $cm^{-3}$ $eV^{-1}$ exist in the $In_2O_3$ layer. Thus, bulk traps in $In_2O_3$ are the main cause for C–V frequency dispersion and the high conductance peak, instead of interface trap states at the $HfO_2/In_2O_3$ interface. It is understood that part of the donor trap states is frozen at high frequency, leading to the reduction of effective $N_D$ and the flat band voltage shift, so that a large frequency dispersion at high voltage can be observed.

## CONCLUSION

In summary, ALD $In_2O_3$ transistors and MOS capacitors with 3.5 nm $HfO_2$ as the gate insulator and 3.5 nm $In_2O_3$ as the channel semiconductor are fabricated. The interface and bulk traps in this MOS gate stack of ALD $In_2O_3$ transistors are systematically studied by using the C–V and conductance method. A low EOT of 0.93 nm is achieved directly from the accumulation capacitance in the C–V curve, indicating a high-quality gate oxide and oxide/semiconductor interface. Defects in bulk $In_2O_3$ with the energy level in subgap are confirmed to be responsible for the conductance peak in $G_p/\omega$ versus ω curves by TCAD simulations of C–V and G–V characteristics. A high n-type doping of $1 \times 10^{20}/cm^3$ is achieved by C–V measurement, which is further confirmed by the high conductance peak of $7.6 \times 10^{-6}$ S·s/$cm^2$, corresponding to a high subgap DOS of $3.3 \times 10^{20}$ $cm^{-3}$ $eV^{-1}$, which contributes to the high n-type doping and high electron density. The high electron density is because CNL aligns deeply inside the $E_C$, which is speculated to be related to In atoms, thus In-based semiconductors tend to have high electron densities.

## DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

## AUTHOR CONTRIBUTIONS

MS and ZL performed device fabrication. MS and ZL did the electrical measurements. ZW and MS analyzed the electrical data. PY conceived the idea on CNL alignment. ZW conducted TCAD simulations. ZW and MS analyzed the simulation data. ZW, MS, and PY wrote the manuscript.

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