Applied Physics Letters

Vertically stacked multilayer atomic-layer-deposited sub-1-nm In_2O_3 field-effect transistors with back-end-of-line compatibility

Cite as: Appl. Phys. Lett. **120**, 202104 (2022); https://doi.org/10.1063/5.0092936
Submitted: 24 March 2022 • Accepted: 28 April 2022 • Published Online: 16 May 2022

Zhuocheng Zhang, Zehao Lin, Mengwei Si, et al.

Applied Physics Letters ARTICLE scitation.org/journal/apl

Vertically stacked multilayer atomic-layer-deposited sub-1-nm In_2O_3 field-effect transistors with back-end-of-line compatibility

Cite as: Appl. Phys. Lett. **120**, 202104 (2022); doi: 10.1063/5.0092936
Submitted: 24 March 2022 · Accepted: 28 April 2022 ·
Published Online: 16 May 2022

View Online Export Citation CrossMark

Zhuocheng Zhang,[1,2] Zehao Lin,[1,2] Mengwei Si,[1,2] Di Zhang,[3] Hongyi Dou,[3] Zhizhong Chen,[1,2] Adam Charnas,[1,2] Haiyan Wang,[3] and Peide D. Ye[1,2,a)]

AFFILIATIONS

[1]Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA
[2]Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA
[3]School of Materials Engineering, Purdue University, West Lafayette, Indiana 47907, USA

[a)]Author to whom correspondence should be addressed: yep@purdue.edu

ABSTRACT

In this work, we demonstrate vertically stacked multilayer sub-1-nm In_2O_3 field-effect transistors (FETs) with surrounding gate in a back-end-of-line (BEOL) compatible low-temperature fabrication process. A typical bottom-gated single layer In_2O_3 FET with maximum on-state current (I_{ON}) of 890 μA/μm at $V_{DS} = 0.8$ V and an on/off ratio over 10^6 is achieved with a channel length (L_{ch}) of 100 nm. The effects of HfO_2 capping and O_2 annealing are systematically studied, which is critical to realizing the multilayer FETs. Each atomically thin In_2O_3 channel layer with a thickness (T_{IO}) of 0.9 nm is realized by atomic layer deposition (ALD) at 225 °C. Multilayer FETs with a number of In_2O_3 layers up to 4 and 1.2 nm-thick HfO_2 between each individual layer are fabricated. An enhancement of on-state current (I_{ON}) from 183 μA in a single layer In_2O_3 FET to 339 μA in a 4 layer device with an on/off ratio of 3.4×10^4 is achieved, demonstrating the key advantage of the multilayer FETs to improve the current. Several critical features, such as large-area growth, high uniformity, high reproducibility, ultrathin body, flexibility, and BEOL compatibility, have turned ALD In_2O_3 into a noteworthy candidate for next-generation oxide semiconductor channel materials.

Exploration for back-end-of-line (BEOL) compatible next-generation channel materials is becoming crucial for monolithic 3D integration at advanced technology nodes. Oxide semiconductors, as one competitive candidate, have been widely studied over the past few decades and become the leading material in the field of flat panel displays due to three main advantages.[1–6] First, the high transparency due to the large bandgap of oxide semiconductors enables numerous applications in flexible displays and wearable devices. Second, the amorphous microstructure makes oxide semiconductors film relatively uniform and avoids variation of electrical properties caused by grain boundary problems in poly-Si thin film transistors (TFTs).[7] Third, the bottom of the conduction band in amorphous oxide semiconductors is primarily composed of the isotropically spread metal *ns* orbitals, which has possible direct overlap with neighboring metal *ns* orbitals, so the chemical bond is insensitive to distortion and the mobility is much higher than covalent semiconductors consisting of sp^3 orbitals with strong directivity.[8]

Nevertheless, the large film thickness by sputtering and the lack of effective gate control due to the degeneracy in the conduction band have impeded oxide semiconductors to be used as active channel materials in ultra-scaled TFTs.[9] Remarkably, recent atomic layer deposition (ALD) deposited nanometer-thin In_2O_3 field-effect transistors (FETs) exhibit maximum on-state currents over 2 mA/μm and well-behaved switching characteristics with the on/off ratio over 10^6 and the minimum subthreshold slope (SS) of 88 mV/dec.[10] Compared to the most sputtered oxide semiconductor thin films, the emerging ALD channel offers two main advantages. First, ALD has an accurate film thickness control in atomic scale and high reproducibility. Second, ALD provides large-area uniformity and excellent conformity on 3D structures.[11,12] Hence, carrier scattering due to surface roughness can

be reduced with the atomically smooth surface of the In_2O_3 thin film enabled by ALD. On the other hand, it has been confirmed that the ALD deposited In_2O_3 has a strong thickness-dependent electron transport, which is attributed to the quantum confinement effect on the alignment of trap neutral level (TNL).[13,14] The bandgap increases from 1.4 eV in bulk In_2O_3 to 2.43 eV in a 0.7 nm-thick film as the thickness decreases, which is smaller than most other semiconductors of which the bandgap is usually larger than 3 eV.[14] Therefore, the lack of gate control due to extremely high carrier density can be solved by lowering the film thickness and a maximum on-state current (I_{ON}) of 2.5 mA/μm with a high field effect mobility (μ_{FE}) of 113 cm^2/V·s has been reported in recent back-gate In_2O_3 FETs with a channel thickness of 2.2 nm and a channel length of 40 nm.[15] In addition, an enhancement-mode operation is also achieved through O_2 plasma or low temperature O_2 annealing because of the filling of oxygen vacancies,[16,17] making the ALD deposited In_2O_3 film a choice as the channel material in the complementary metal-oxide-semiconductor (CMOS) design and BEOL compatible monolithic 3D integration.

In this work, we systematically study the effects of HfO_2 capping and O_2 annealing to effectively control the threshold voltage (V_T) of each channel layer based on typical atomically thin In_2O_3 FETs with I_{ON} of 890 μA/μm at $V_{DS} = 0.8$ V, the on/off ratio over 10^6, the channel thickness (T_{IO}) of 2 nm, and the channel length (L_{ch}) of 100 nm. Vertically stacked multilayer sub-1-nm-thin In_2O_3 FETs with surrounding gate with the dielectric of 5 nm HfO_2 are realized with an enhancement of I_{ON} as the number of In_2O_3 channel layers increases, demonstrating the key advantage of multilayer FETs.

Figure 1(a) shows the schematic diagram of a single layer In_2O_3 FET grown by ALD. The gate stack includes 40 nm Ni as the bottom gate and 5 nm HfO_2 as the gate dielectric. Figure 1(b) shows the 3D schematic diagram of a stacked four-layer In_2O_3 FET with 0.9 nm In_2O_3 as each semiconducting channel separated by 1.2 nm HfO_2. Figure 1(c) shows the cross-sectional view of the device schematic in source/drain direction. Thickness of films is accurately controlled by ALD cycles and measured by ellipsometry. The whole vertically stacked channel is surrounded by 40 nm Ni as gate metal and 5 nm HfO_2 as gate dielectric so that all inner In_2O_3 channels can be modulated by the surrounding gate. The detailed device fabrication process is described in the supplementary material. Figure 1(d) shows the scanning transmission electron microscopy (STEM) image of a stacked five-layer In_2O_3 structure with clear interfaces between In_2O_3 and HfO_2. Figure 1(e) shows the energy dispersive x-ray spectroscopy (EDS) image of the same stack, which also confirms the multilayer structure. Figure 1(f) shows the scanning electron microscopy (SEM) image of a typical fabricated device with sharp edge and well-defined L_{ch} of 1 μm. All devices have a channel width of 2 μm. Figure 1(g) shows a low surface roughness of 0.38 nm for the ALD deposited In_2O_3 film measured by atomic force microscope (AFM). This result has relatively small variance for different batches of ALD In_2O_3 films, indicating high reproducibility in potential large-scale industrial manufacture. The fabrication of vertically stacked multilayer In_2O_3 FETs

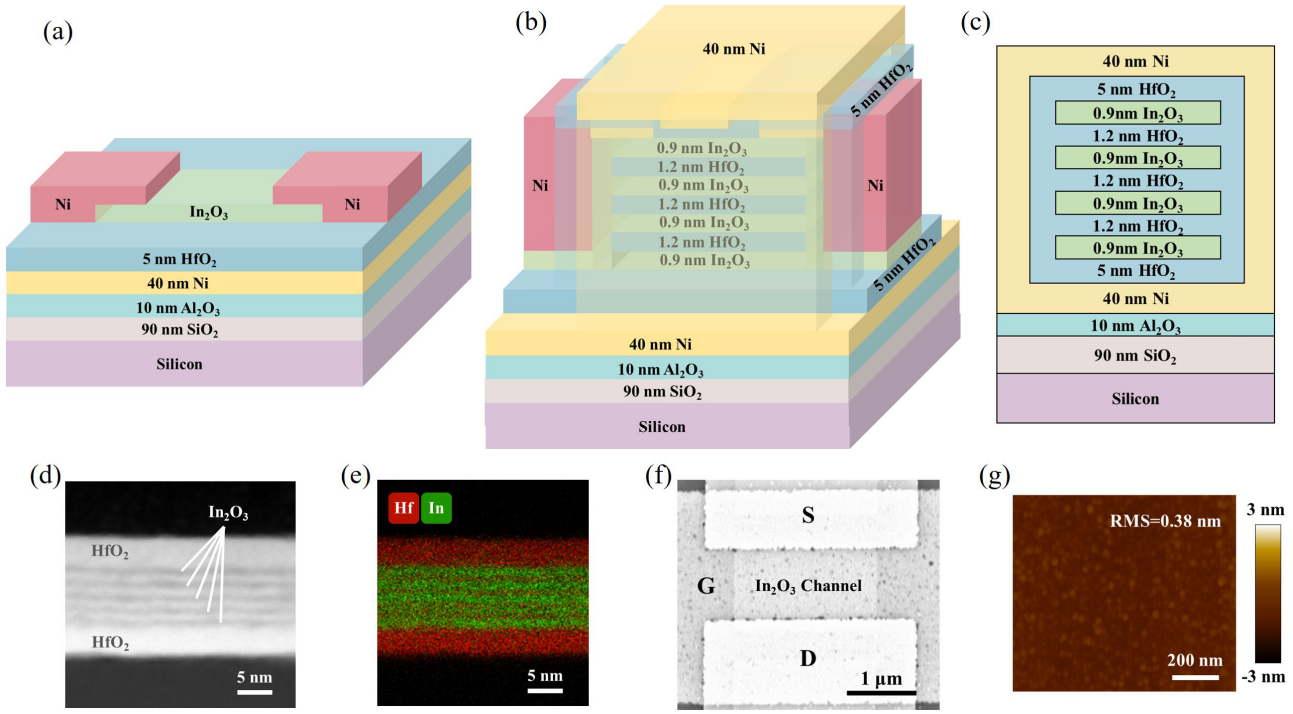

FIG. 1. (a) Device schematic of a single-layer ALD In_2O_3 FET with 5 nm HfO_2 as bottom gate dielectric. Device schematic of a vertically stacked four-layer In_2O_3 FET with 5 nm HfO_2 as surrounding gate dielectric in (b) a 3D model, (c) cross-sectional view in the S/D direction. (d) STEM image and (e) EDS image of the vertically stacked five-layer ALD In_2O_3 structure. (f) SEM image (top view) of a finished vertically stacked multilayer In_2O_3 FET with surrounding gate. (g) AFM measurement of 2 nm In_2O_3 thin film deposited on a Si substrate with a surface roughness (RMS) of 0.38 nm.

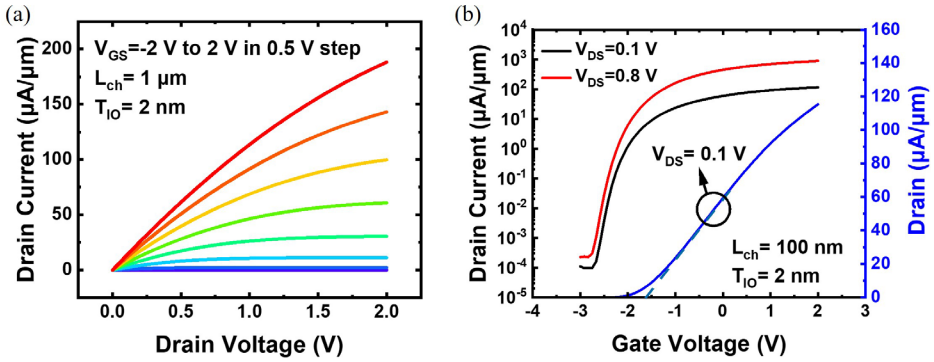

FIG. 2. (a) Output characteristics of a single layer In_2O_3 FET with 5 nm HfO_2 as bottom gate dielectric and channel length of 1 μm. (b) Transfer characteristics of a single layer In_2O_3 FET with 5 nm HfO_2 as bottom gate dielectric and channel length of 100 nm, showing I_{ON} of 890 $\mu A/\mu m$ at $V_{DS} = 0.8$ V.

has a low thermal budget of 250 °C, which is in general BEOL compatible for monolithic 3D integration.

Figure 2 shows the typical output and transfer characteristics of the bottom-gated single layer In_2O_3 FET with T_{IO} of 2 nm. Drain current saturation is observed at large V_{DS} in the device with L_{ch} of 1 μm. Maximum I_{ON} of 890 $\mu A/\mu m$ at $V_{DS} = 0.8$ V, the on/off ratio over 10^6, the subthreshold slope (SS) of 130 mV/dec, and μ_{FE} of 23 $cm^2/V{\cdot}s$ are achieved in the single layer In_2O_3 FET with L_{ch} of 100 nm. To investigate the conducting mechanism of the ALD deposited In_2O_3 films, Fig. 3 presents the evolution of the transfer characteristics of the same single layer In_2O_3 FET after HfO_2 capping and multiple times of O_2 annealing in (a) log-scale plot at $V_{DS} = 0.8$ V and (b) linear-scale plot at $V_{DS} = 0.1$ V. A loss of gate control over the In_2O_3 channel is observed after 3 nm HfO_2 capping by ALD on the as-fabricated device at 200 °C, whereas the control is gradually retrieved after following O_2 annealing at 250 °C with clear positive V_T shift. Such phenomena can be understood by the band diagram of In_2O_3 shown in Fig. 3(c). It is known that oxygen vacancies act as shallow donors and determine the carrier density in In_2O_3 related films.[16–18] Modulation of oxygen pressure during film deposition or thermal annealing contributing to the change in electrical conductivity has been widely investigated in ITO, In-Zn-O (IZO), In-Ga-Zn-O (IGZO), etc.[1–6,18,19] Therefore, it is likely that oxygen atoms in atomically thin In_2O_3 film are scavenged by the ALD growth of HfO_2 due to a more stable Hf–O bond with a dissociation energy of 801 kJ/mol compared to In–O bond of 346 kJ/mol.[20,21] The created oxygen vacancies in In_2O_3 provide extra electrons, and the Fermi level moves deeply into the conduction band, resulting in a large electron density, negative V_T shift, and the lack of gate control. More defects can also be generated in the bulk film and interface. Conversely, oxygen vacancies can be filled and defects can be healed by O_2 annealing, which reduces the interface trap density and lowers electron density with increasing annealing time, moves Fermi level toward the conduction band edge, and gradually restores gate control. Further experiments on material characterization are still needed to validate this explanation. In addition, the different gate control capabilities between top and bottom gates in a dual-gated single layer In_2O_3 FET are also studied in Fig. 4. The measurement was done by adjusting single top/bottom gate voltage with another grounded. A better gate control is obtained in bottom-gated control condition because the carrier density of In_2O_3 under S/D contact can only be modulated by bottom gate, leading to favorably controlled contact resistance (R_C). Meanwhile, the bottom In_2O_3/HfO_2 interface has less oxygen vacancies than the top In_2O_3/HfO_2 interface, since In–O chemical bond is weaker than Hf–O one so that the ALD growth of In_2O_3 on top of HfO_2 cannot break the surface Hf–O bond of the bottom HfO_2 film.

Figures 5(a)–5(d) present the transfer characteristics of stacked one, two, three, and four-layer In_2O_3 FETs with L_{ch} of 50 nm and the surrounding gate structure shown in Fig. 1. Each In_2O_3 channel layer

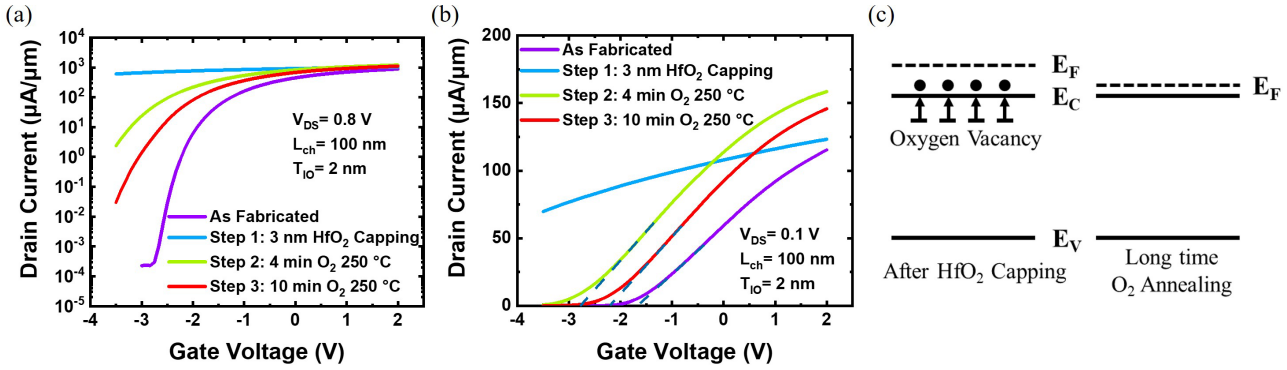

FIG. 3. (a) Logscale plot of the evolution of transfer characteristics of a bottom-gated single layer In_2O_3 FET with $V_{DS} = 0.8$ V after HfO_2 capping and O_2 annealing. (b) Linear plot of the evolution of transfer characteristics of a bottom-gated single layer In_2O_3 FET with $V_{DS} = 0.1$ V after HfO_2 capping and O_2 annealing. It shows the challenge of top-gate HfO_2 integration. (c) Band diagram of In_2O_3 after HfO_2 capping and long-time O_2 annealing showing the change of E_F.

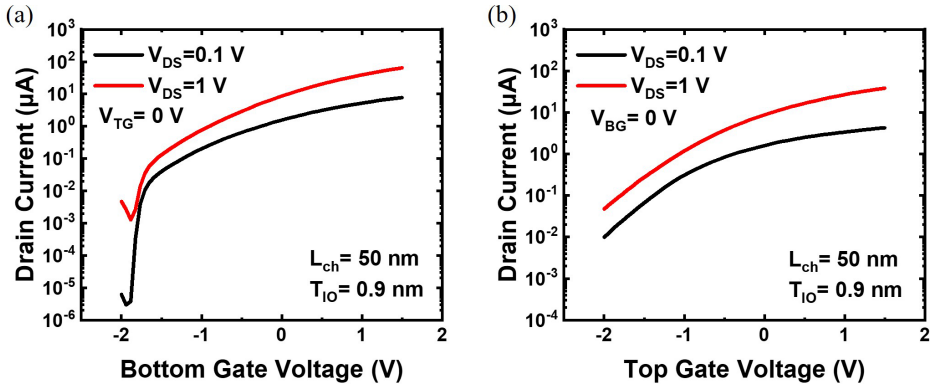

FIG. 4. (a) Transfer characteristics of a single layer In_2O_3 FET under bottom gate control with V_{TG} set to 0 V. (b) Transfer characteristics of a single layer In_2O_3 FET under top gate control with V_{BG} set to 0 V.

with T_{IO} of 0.9 nm is separated by 1.2 nm HfO_2, and an on/off ratio around 10^5 is achieved. Figure 5(e) shows the output characteristics of a stacked four-layer In_2O_3 FET with L_{ch} of 1 μm, exhibiting drain current saturation at large V_{DS} as one-layer one shown in Fig. 2. Figure 5(f) summarizes I_{ON} at $V_{DS} = 1$ V, $V_{GS} = 1.7$ V and total In_2O_3 channel thickness vs the number of vertically stacked layers. An increase in drain current is realized by stacking more In_2O_3 channel layers, confirming that the key advantage of multilayer FETs for enhancing I_{ON} since multilayer FET is claimed by Si industry as the technology for 3 nm node and beyond. Nevertheless, a modest current gain from 183 μA in a single layer In_2O_3 FET to 339 μA in a four-layer device is observed, which seems a limited enhancement for the stacked channel. This is because the surrounding gate only has a relatively weak control of the inner second and third In_2O_3 channel compared to it can directly modulate the carrier density of first and fourth In_2O_3 channels over the top and bottom 5 nm-thick HfO_2. Such deficiency can be improved by inserting gate metal between each In_2O_3 to achieve an equally strong gate control of all conducting channels. The nonlinear increase in I_{ON} is due to a 200 nm L_{ch} difference between top and the other In_2O_3 layers, which is a process issue with e-beam lithography and can be eliminated eventually.

Figure 6(a) shows R_C extracted by the transfer length method (TLM) vs $V_G - V_T$. R_C is relatively large due to the sub-1-nm In_2O_3 channel, which can be improved by increasing channel thickness or

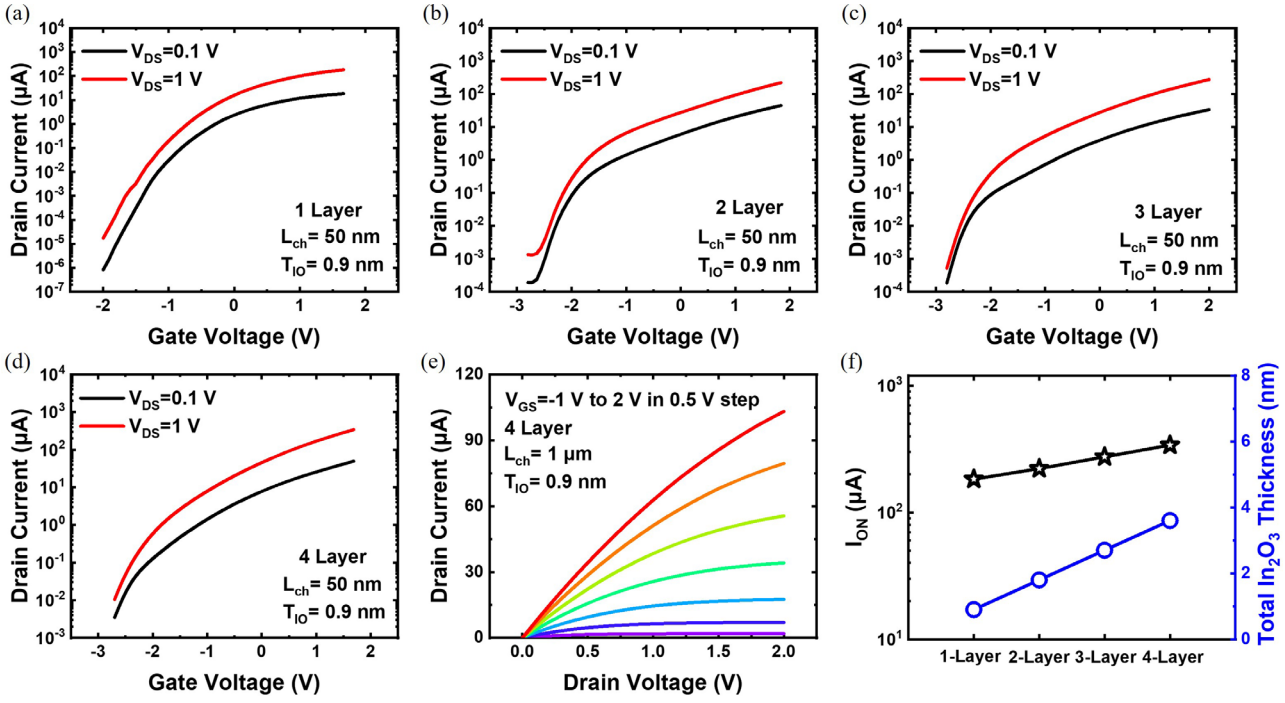

FIG. 5. Transfer characteristics of a (a) single-layer, (b) two-layer, (c) three-layer, and (d) four-layer In_2O_3 FET with surrounding gate. (e) Output characteristics of a four-layer In_2O_3 FET with surrounding gate and channel length of 1 μm. (f) On-state current at V_{DS} of 1 V, V_{GS} of 1.7 V and total In_2O_3 channel thickness vs number of layers, showing increasing current with more In_2O_3 layers.

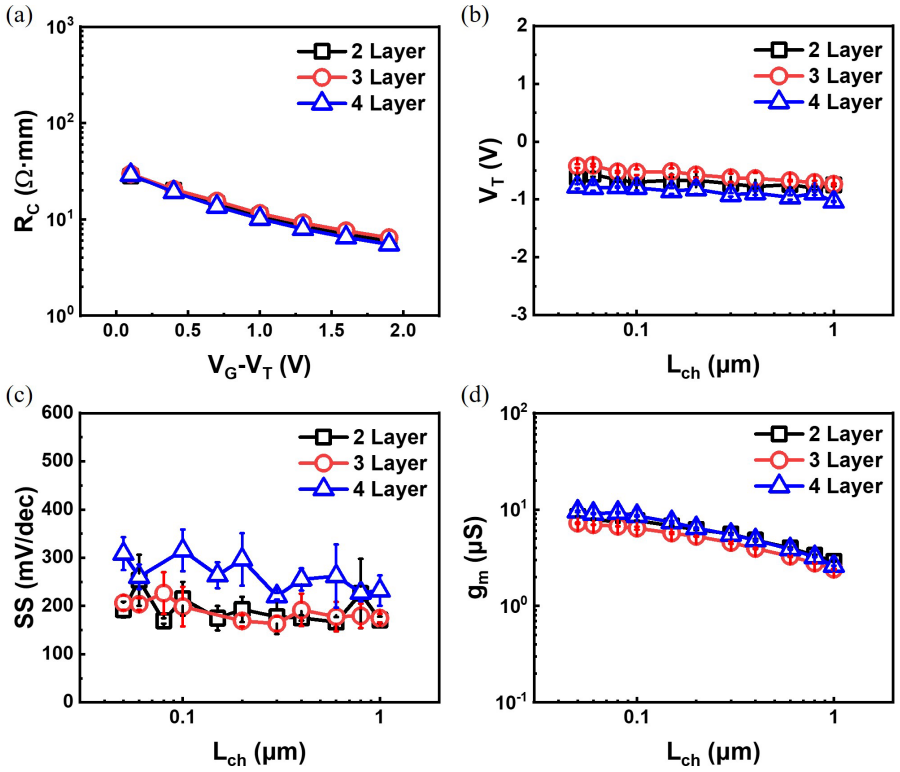

FIG. 6. (a) Contact resistance vs $V_G - V_T$ of stacked multilayer In_2O_3 FETs. (b) V_T, (c) SS, and (d) g_m scaling metrics of stacked multilayer In_2O_3 FETs with surrounding gate, L_{ch} from 50 nm to 1 μm. Each data point represents the average of at least three devices.

raised S/D contacts. The device performance of multilayer FETs still has large room to improve by optimizing the fabrication process. Figures 6(b)–6(d) summarize the scaling metrics of stacked multilayer In_2O_3 FETs with L_{ch} from 50 nm to 1 μm statistically. Each data point represents the average of at least three devices. Figure 6(b) shows V_T vs L_{ch}, which is extracted by the linear extrapolation method at $V_{DS} = 0.1$ V. Notably, the device has a strong immunity to short channel effects due to the ultrathin In_2O_3 channel, whose thickness is even comparable to monolayers of 2D semiconductors, such as MoS_2. Moreover, high-quality HfO_2 gate dielectric can be realized by ALD on the 3D In_2O_3 channel, while it is impeded by the lack of dangling bonds on the van der Waals surface in 2D materials. Both factors contribute to extremely small transistor characteristic length,[22] offering great potential for ultimately scaled FETs. Figure 6(c) presents SS vs L_{ch} characteristics. Minimum SS of 163 mV/dec is obtained in a three-layer In_2O_3 FET, which can be further improved by improving interface quality and scaling gate dielectric. Figure 6(d) summarizes the intrinsic transconductance vs L_{ch} for In_2O_3 FETs with different channel layers. Figure 7 presents a benchmarking of I_{ON} for ALD In_2O_3 FETs and other sputtered oxide semiconductors. As can be seen, ALD deposited oxides have more accurate thickness control in sub-1-nm region compared to sputtered films. Meanwhile, the current level of the atomically thin ALD In_2O_3 FETs can compete with other sputtered oxides with larger thickness, demonstrating outstanding performance of ALD In_2O_3 as a promising BEOL-compatible oxide semiconductor channel.

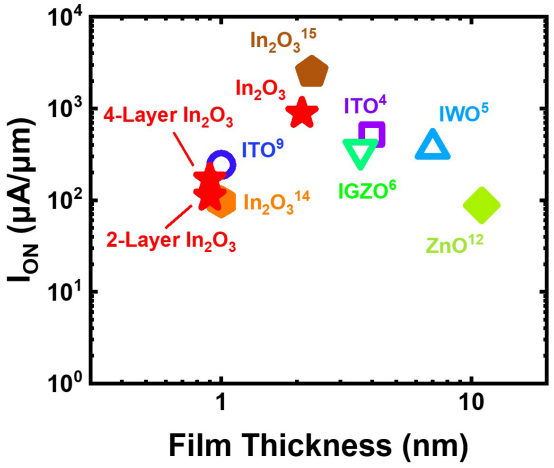

FIG. 7. Benchmark of I_{ON} vs film thickness of recent thin film oxide semiconductor transistors. Solid symbols represent films grown by ALD.

In conclusion, BEOL-compatible vertically stacked multilayer In_2O_3 FETs with surrounding gate are demonstrated. Each atomic-layer-thin 0.9 nm In_2O_3 channel layer and 1.2 nm HfO_2 separation layer are realized by accurately controlled ALD at 225 °C. Several distinct features, namely, large-area growth, high uniformity, excellent conformability, ultrathin body, and low thermal budget fabrication process demonstrate ALD In_2O_3 as a competitive oxide semiconductor channel material for future monolithic 3D integration and ultimately scaled electronics.

See the supplementary material for the details of device fabrication and characterization.

The authors gratefully acknowledge the funding support from Semiconductor Research Corporation (SRC) Nanoelectronic Computing Research Innovative Materials and Processes for Accelerated Compute Technologies Center and Defense Advanced Research Projects Agency/SRC Joint University Microelectronics Program Applications and Systems-driven Center for Energy Efficient integrated Nano Technologies Center on this work.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, Jpn. J. Appl. Phys. **45**(5B), 4303–4308 (2006).
[2]H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. **89**(11), 112123 (2006).
[3]E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**(22), 2945–2986 (2012).
[4]S. M. Li, M. C. Tian, Q. G. Gao, M. F. Wang, T. Y. Li, Q. L. Hu, X. F. Li, and Y. Q. Wu, Nat. Mater. **18**(10), 1091–1097 (2019).
[5]W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, paper presented at the 2020 IEEE Symposium on VLSI Technology, 2020.
[6]S. Samanta, K. Han, C. Sun, C. Wang, A. V. Y. Thean, and X. Gong, paper presented at the 2020 IEEE Symposium on VLSI Technology, 2020.
[7]T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11**(4), 044305 (2010).
[8]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**(7016), 488–492 (2004).
[9]M. Si, J. Andler, X. Lyu, C. Niu, S. Datta, R. Agrawal, and P. D. Ye, ACS Nano **14**(9), 11542–11547 (2020).
[10]M. Si, Z. Lin, A. Charnas, and P. D. Ye, IEEE Electron Device Lett. **42**(2), 184–187 (2021).
[11]J. Sheng, H.-J. Jeong, K.-L. Han, T. Hong, and J.-S. Park, J. Inf. Disp. **18**(4), 159–172 (2017).
[12]M. Wang, D. Zhan, X. Wang, Q. Hu, C. Gu, X. Li, and Y. Wu, IEEE Electron Device Lett. **42**(5), 716–719 (2021).
[13]P. D. Ye, J. Vac. Sci. Technol. A **26**(4), 697–704 (2008).
[14]M. Si, Y. Hu, Z. Lin, X. Sun, A. Charnas, D. Zheng, X. Lyu, H. Wang, K. Cho, and P. D. Ye, Nano Lett. **21**(1), 500–506 (2021).
[15]M. Si, Z. Lin, Z. Chen, and P. D. Ye, in Proceeding of the 2021 IEEE Symposium on VLSI Technology, 2021.
[16]A. Charnas, M. Si, Z. Lin, and P. D. Ye, Appl. Phys. Lett. **118**(5), 052107 (2021).
[17]M. Si, A. Charnas, Z. Lin, and P. D. Ye, IEEE Trans. Electron Devices **68**(3), 1075–1080 (2021).
[18]T. Kamiya and H. Hosono, NPG Asia Mater. **2**(1), 15–22 (2010).
[19]S. Y. Park, J. H. Song, C. K. Lee, B. G. Son, C. K. Lee, H. J. Kim, R. Choi, Y. J. Choi, U. K. Kim, C. S. Hwang, H. J. Kim, and J. K. Jeong, IEEE Electron Device Lett. **34**(7), 894–896 (2013).
[20]H. Fujiwara, Y. Sato, N. Saito, T. Ueda, and K. Ikeda, IEEE Trans. Electron Devices **67**(12), 5329–5335 (2020).
[21]Y.-R. Luo, *Comprehensive Handbook of Chemical Bond Energies* (CRC Press, 2007).
[22]Y. Liu, X. D. Duan, H. J. Shin, S. Park, Y. Huang, and X. F. Duan, Nature **591**(7848), 43–53 (2021).