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The Impact of Channel Semiconductor on the Memory Characteristics of Ferroelectric Field-Effect Transistors

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ABSTRACT In this work, channel semiconductor is identified and demonstrated to have significant impact on the memory characteristics of ferroelectric field-effect transistors (Fe-FETs). It is understood that, to achieve high electron density at on-state, it requires high hole density at the off-state to realize the charge balance and strong ferroelectric polarization switching in n-type Fe-FETs. Therefore, Fe-FETs with a wider bandgap semiconductor channel have a much smaller memory window than Fe-FETs with a narrower bandgap semiconductor channel due to the insufficient polarization switching. The simple device physics suggests that narrow bandgap semiconductor channel such as Ge is preferred for Fe-FETs with large memory window.

INDEX TERMS Fe-FET, hafnium zirconium oxide, ferroelectric, polarization switching, charge balance.

I. INTRODUCTION

Ferroelectric field-effect transistor is a promising device candidate for future non-volatile memory applications. The ferroelectricity in hafnium oxide (HfO_2) was revealed by introducing certain dopant, such as Si, Zr, Al etc., to stabilize the orthorhombic phase [1], [2]. Fe-FETs employing ferroelectric (FE) HfO_2 in the gate stack attract tremendous attention due to its CMOS compatible process, long retention, and fast read/write speed [3]–[15].

FE HfO_2 are known to have high remnant polarization around $10 \sim 30$ $\mu C/cm^2$. Ferroelectric/dielectric (FE/DE) stack are commonly used in Fe-FETs because it is critical to realize high-quality interface using interfacial layer as an ultrathin DE in metal-oxide-semiconductor (MOS) type transistors although atomic layer deposited FE HfO_2 is easy to integrate on different semiconductor channels. It was pointed out that the FE/DE stack cannot be simply understood using continuous displacement field condition at FE/DE interface [9], [11], [15], [16]. The reason is that dielectric materials such as SiO_2 or Al_2O_3 cannot support such high charge density below their breakdown field. Therefore, the interfacial charge at FE/DE interface and leakage-assist polarization switching must be considered for charge balance [15].

Although the charge balance in the FE/DE stack could be simply understood by introducing interfacial charge in metal-FE/DE-metal structure, the complete understanding of the gate stack considering both gate insulator and different semiconducting channel has not been achieved. Fig. 1 shows the charge balance condition of a Fe-FET with metal/FE/semiconductor (MFS) structure. For simplicity and focusing on the discussion of the impact of semiconductor channels, MFS is used instead of metal/FE/DE/semiconductor structure. The conclusion remains the same when considering the FE/DE interface. As can be seen, both electron and hole are required for charge balance. Considering the high polarization charge density in FE HfO_2, both high electron density and high hole density are required to obtain ferroelectric polarization switching, especially for Fe-FET with low-doped channel. For highly doped channel, space charge region can compensate the positive charge partly. This charge balance condition points out

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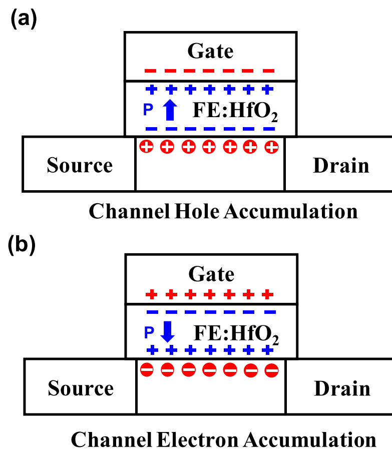

FIGURE 1. Charge balance condition of Fe-FET in (a) polarization up and (b) polarization down states.

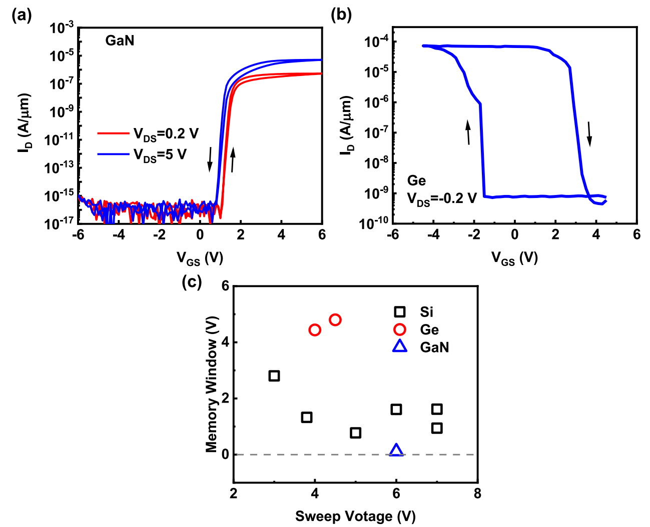

FIGURE 2. (a) $I_D - V_{GS}$ characteristics of a GaN MOS-HEMT with 15 nm FE HZO as gate insulator and a channel length of 7 μm. (b) $I_D - V_{GS}$ characteristics of a Ge Fe-FET with 10 nm FE HZO as gate insulator and a channel length of 100 nm. (c) Comparison of memory window versus sweep voltage in Fe-FETs with Si ([4], [6]–[8], [12]), Ge ([7]) and GaN as channel semiconductors.

a fact that was commonly ignored so far, which has significant impact on the memory characteristics of Fe-FETs. For example, because hole density in n-type GaN is very low, the full polarization switching in high-quality GaN Fe-FET is difficult and almost impossible. Therefore, channel materials can have high impact on the memory characteristics of Fe-FETs if we explore novel materials beyond Si. Meanwhile, the ability to achieve both high electron density and high hole density are also affected by many other factors such as interface traps, surface traps, bulk traps, bandgap of semiconductor, and device structure, etc. Thus, to understand the impact of channel semiconductor on the memory characteristics of Fe-FETs is important to explore Fe-FETs for future non-volatile memory applications.

In this work, the impact of channel semiconductors on the memory characteristics of Fe-FETs are investigated by both experiment and simulation. The memory window (MW) of Fe-FETs exhibits significant dependence on channel materials. It is found Fe-FETs with a narrow bandgap channel have much larger MW than Fe-FETs with a wide bandgap channel. Such phenomenon is understood by the lack of sufficient hole density to satisfy charge balance condition and not enough electric field to trigger polarization switching, which is confirmed by TCAD simulation of electrostatic potential and carrier density.

II. FE-FET EXPERIMENTS WITH DIFFERENT CHANNEL SEMICONDUCTORS

Fig. 2 compares the experimental Fe-FETs with different channel materials. Fig. 2(a) shows the $I_D - V_{GS}$ characteristics of a GaN MOS-HEMT with 15 nm FE hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO) as gate insulator and channel length (L_{ch}) of 7 μm. The device structure and fabrication process are the same as the planar MOS-HEMT in previous report [17], except for the application of 15 nm HZO as ferroelectric gate insulator. The application of GaN MOS-HEMT structure instead of GaN MOSFET here is due to the difficulty in realizing GaN MOSFET device experimentally. The different device structure does not affect the conclusion in this work. The integration of HZO on AlGaN/GaN MOS-HEMT leads to a dramatic positive threshold voltage shift and the realization of enhancement-mode operation as shown in Fig. 2(a), being consistent to the previous reports on the similar material system [18]. A counterclockwise hysteresis loop is achieved with a small MW of 0.11 V and gate voltage sweep range from −6 V to 6 V. The very small hysteresis is similar to ferroelectric minor loop instead of a full ferroelectric polarization switch because high-quality AlGaN/GaN heterostructure couldn't provide sufficient hole density to realize ferroelectric polarization switching. It is impossible to realize bulk inversion in GaN material systems in great contrast to Ge or Si. Fig. 2(b) shows the $I_D - V_{GS}$ characteristics of a Ge p-type Fe-FET with 10 nm HZO as gate insulator and L_{ch} of 100 nm. The device structure and fabrication process are previously reported in [7]. The $I_D - V_{GS}$ curve shows a clear and strong ferroelectric hysteresis loop with a MW as high as 4.8 V and gate voltage sweep range from −4.5 V to 4.5 V. Note that clockwise loop is ferroelectric one for a p-type Fe-FET. We ascribe the observed large MW in Ge Fe-FETs to the narrow bandgap of Ge and easy realization of inversion. Fig. 2(c) shows the comparison of MW versus sweep voltage of Ge, Si and GaN Fe-FETs from the experimental results in this work and literature reports. The sweep voltage is defined as (maximum sweep voltage – minimum sweep voltage)/2. As we can see, Ge Fe-FET shows a significantly higher MW compared to Si Fe-FETs ([4], [6]–[8], [12]). The MW of GaN Fe-FET is close zero. Fig. 2(c) demonstrates that Fe-FETs with a narrow bandgap channel have a much larger MW compared to Fe-FETs with a wide bandgap channel.

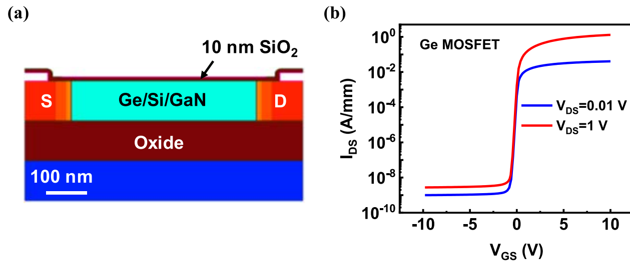

FIGURE 3. (a) Schematic diagram of the device structure in simulation with Si, Ge and GaN as channel semiconductors. (b) $I_D - V_{GS}$ characteristics of a simulated Ge nMOSFET.

Such channel material dependence phenomenon is understood by two reasons. (i) Fe-FETs with wide bandgap channel are difficult to achieve high electron density and high hole density in the same device. Therefore, full polarization switching is difficult because charge balance condition (as shown in Fig. 1) cannot be satisfied. (ii) The voltage drop across the gate insulator (V_{OX}) at off-state in Fe-FET with a wide bandgap channel is much smaller than gate voltage, so that the electric field in the gate insulator is not large enough to trigger full polarization switching. Thus, strong polarization switching at off-state is difficult. This conclusion is universal and can be applied to all different channel semiconductors.

III. SIMULATION OF ELECTROSTATIC POTENTIAL AND CARRIER DENSITY

To confirm the above understanding, TCAD simulation is performed to simulate the electrostatic potential and carrier density distribution in nMOSFETs with Ge, Si and GaN as channel materials. Fig. 3(a) shows the schematic diagram of the device structure in simulation, with Si, Ge and GaN as channel semiconductors. A dielectric gate insulator (10 nm SiO_2) is used here to simulate V_{OX}, not considering the ferroelectricity. Then, this V_{OX} can be used to compare with the coercive voltage of ferroelectric gate insulator. The device has a channel length L_{ch} of 400 nm and channel thickness of 100 nm. A body contact is used and grounded to exclude the floating body effect. Fig. 3(b) shows the $I_D - V_{GS}$ curve of a simulated Ge nMOSFET with a threshold voltage near 0 V.

Fig. 4 shows the electrostatic potential as a function of y position at the center of channel at $V_{GS} = -10$ V and $V_{GS} = 10$ V in devices with Ge, Si and GaN as channel. At $V_{GS} = 10$ V, most voltage drop is across the gate insulator for all three devices with Ge, Si and GaN channels. V_{OX} at $V_{GS} = 10$ V are 9.8 V, 9.9 V and 9.4 V for devices with Ge, Si and GaN as channel, respectively. V_{OX} are all close to V_{GS} because high electron density is formed at the oxide/semiconductor interface and electrons at the surface of the channel screen the electric field penetration into the semiconductor body. This V_{OX} is sufficiently large to trigger the ferroelectric switch if we replace SiO_2 by HZO. However, V_{OX} at $V_{GS} = -10$ V becomes -9.1 V, -8.7 V and -1.8 V

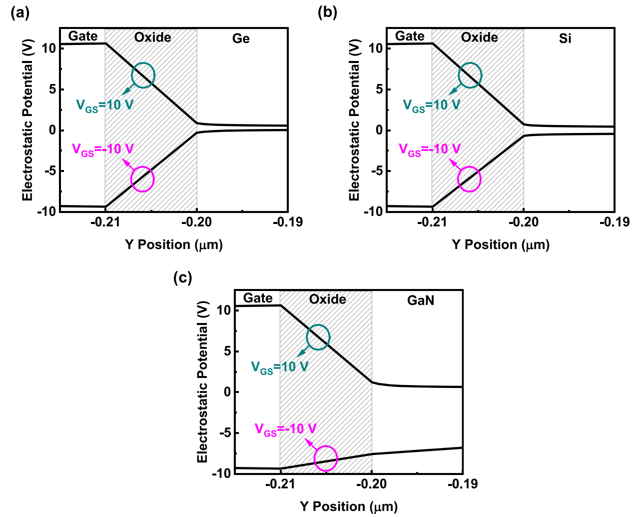

FIGURE 4. Electrostatic potential as a function of y position at the center of channel at $V_{GS} = -10$ V and $V_{GS} = 10$ V in (a) Ge, (b) Si and (c) GaN nMOSFETs.

for devices with Ge, Si and GaN as channel, respectively. For devices with Ge and Si channels, most voltage drop is still across the gate insulator because high hole density is formed at the oxide/semiconductor interface by inversion. However, for device with GaN channel, as shown in Fig. 4(c), V_{OX} becomes much smaller than V_{GS} because the electrostatic potential distribution inside the GaN body due to the lack of sufficient inversion hole density at oxide/semiconductor interface.

Fig. 5 shows the electron and hole density as a function of y position at the center of channel at $V_{GS} = 10$ V and $V_{GS} = -10$ V in devices with Ge, Si and GaN channels. For devices with Ge and Si channels, both high electron density at on-state and high hole density at off-state are achieved. For device with GaN channel, electron density at on-state is high but hole density at off-state is very low, leading to the low V_{OX} at off-state for device with GaN channel. This is the fundamental property of a wide bandgap semiconductor

The low hole density and low V_{OX} confirms ferroelectric polarization switching in Fe-FETs with a wide bandgap channel material is difficult because charge balance cannot be satisfied and V_{OX} is usually smaller than coercive voltage of FE gate insulator at off-state. Thus, Fe-FETs with wider bandgap channel materials have a much smaller MW or even near zero-hysteresis. Note that, the simulation in this work assume an ideal condition with no interface or bulk traps. And it is also a static simulation without considering the dynamics. Considering these non-ideal factors, devices with narrower bandgap materials are easier to achieve high electron density and high hole density, similar to metal-FE-metal structure, even considering the Fermi level pinning by interface and bulk traps. Devices with narrower bandgap materials can also accumulate electrons and holes faster due to the faster carrier generation and recombination times.

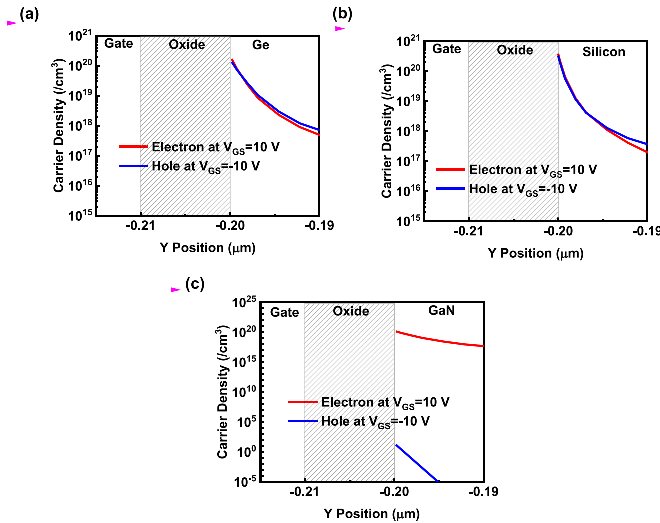

FIGURE 5. Electron and hole density as a function of y position at the center of channel at $V_{GS} = 10$ V and $V_{GS} = -10$ V in (a) Ge, (b) Si and (c) GaN nMOSFETs.

Therefore, Ge Fe-FETs could have a much larger MW than those from Si Fe-FETs as shown in experiments.

Fe-FETs with FE HfO_2 as gate insulator is discussed in this work but the conclusion can also be extended to Fe-FETs with other ferroelectric materials as gate insulators. The remnant polarization and coercive field of the ferroelectric materials can affect the Fe-FET operation, according to the charge balance in Fig. 1. For example, in Fe-FETs with large remnant polarization, more electrons and holes are needed to reach full polarization switching. The coercive voltage of the ferroelectric materials should also be considered because the voltage drop across the gate insulator is less than the applied gate voltage.

IV. CONCLUSION

In conclusion, the impact of channel semiconductors on the memory characteristics of Fe-FETs are studied. It is understood that to achieve high electron density at on-state and high hole density at the off-state are critical to achieve strong ferroelectric polarization switching in n-type Fe-FETs. Therefore, Fe-FETs with a wider bandgap channel have a much smaller memory window than the devices with a narrower bandgap channel due to the insufficient polarization switching. Fe-FETs with narrow bandgap materials as channel, such as Ge, are preferred for high-performance non-volatile memory application.

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