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# Enhanced electrical performances with HZO/$\beta$-$Ga_2O_3$ 3D FinFET toward highly perceptual synaptic device application

Seohyeon Park [a,1], Jaewook Yoo [a,1], Seokjin Oh [i], Hongseung Lee [a], Minah Park [a], Seongbin Lim [a], Soyeon Kim [a], Sojin Jung [a], Bongjoong Kim [h], Keun Heo [g], Taehwan Moon [f], TaeWan Kim [d,e], Mengwei Si [c], Peide D. Ye [b], Hagyoul Bae [a,*]

[a] Department of Electronic Engineering, Jeonbuk National University, 567 Baekje-daero, Deokjin-gu, Jeonju, 54896, Republic of Korea
[b] School of Electrical and Computer Engineering, Purdue University, 465 Northwestern Ave., West Lafayette, IN, 47907, USA
[c] Department of Electronic Engineering, Shanghai Jiao Tong University, 800 Dongchuan Road, Minhang, Shanghai, 200240, China
[d] Department of Intelligent Semiconductor Engineering and School of Advanced Fusion Studies, University of Seoul, Seoul, 02504, Republic of Korea
[e] 2D Epi, inc, Jeonju, 54896, Republic of Korea
[f] Department of Intelligence Semiconductor Engineering, Ajou University, Suwon, 16499, Republic of Korea
[g] School of Semiconductor Science and Technology, Jeonbuk National University, 567 Baekje-daero, Deokjin-gu, Jeonju 54896, Republic of Korea
[h] Department of Mechanical & System Design Engineering, Hongik University, Seoul, 04066, Republic of Korea
[i] School of Electrical Engineering, Kookmin University, Seoul, 02707, Republic of Korea

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ABSTRACT

In this study, we have demonstrated a novel high-performance ferroelectric FinFET (Fe-FinFET) that integrates ultra-wide-bandgap (UWBG) beta-gallium oxide ($\beta$-$Ga_2O_3$) channel with an atomic layer deposited (ALD) hafnium zirconium oxide (HZO) ferroelectric layer for the first time, and experimentally validated the effectiveness of the robust $\beta$-$Ga_2O_3$ platform as a memory application. Compared with conventional planar ferroelectric FET (FeFET), the Fe-FinFET exhibits a markedly wider counter-clockwise hysteresis loop in its transfer characteristics, achieving a large memory window (MW) of 13.9 V with a single HZO layer. When normalized to the actual channel width, the Fe-FinFETs show an improved $I_{ON}/I_{OFF}$ ratio of $2.3 \times 10^7$ and a subthreshold swing value of 110 mV/dec; Y-function method further indicates that the intrinsic mobility is improved to $4.25 \times 10^2$ $cm^2$/Vs. The enhanced polarization due to larger electric fields across the ferroelectric layer in Fe-FinFET is validated using Sentaurus TCAD, and this result is further supported by the energy-dependent distribution of interface trap density ($D_{it}$) extracted in both forward and reverse sweep directions. After $5 \times 10^6$ program/erase (PGM/ERS) cycles, the MW was maintained at 9.2 V, and the retention time was measured up to $3 \times 10^4$ s with low degradation. To verify its potential as an artificial synapse, we trained a convolutional neural network (CNN) and achieved an accuracy of 91.7 %. These results establish the HZO/$\beta$-$Ga_2O_3$ Fe-FinFET as a promising candidate for high voltage-enduring, non-volatile memory devices that also offer synaptic functionality for neuromorphic applications.

## 1. Introduction

As silicon-based transistors approach their ultimate scaling limits, the search for alternative channel materials and device architectures has become essential [1,2]. Semiconductors classified as ultrawide bandgap (UWBG) including gallium nitride (GaN), silicon carbide (SiC), and beta-gallium oxide ($\beta$-$Ga_2O_3$) provide distinct advantages over silicon-based devices, enabling for smaller, faster, and more efficient electronics, especially when high voltages, high frequencies, or elevated temperatures are involved [3]. Among these UWBG materials, $\beta$-$Ga_2O_3$ is considered the only material capable of single-crystal mass growth from the early stages of development [4].

Monolithic $\beta$-$Ga_2O_3$ with a UWBG of 4.6–4.9 eV has been identified as an emerging candidate for next-generation electronic devices. Its UWBG property enables the $\beta$-$Ga_2O_3$ material to have high breakdown electric fields, high carrier mobility, and sustainability under large

* Corresponding author.
*E-mail address:* hagyoul.bae@jbnu.ac.kr (H. Bae).
[1] Seohyeon Park and Jaewook Yoo contributed equally.

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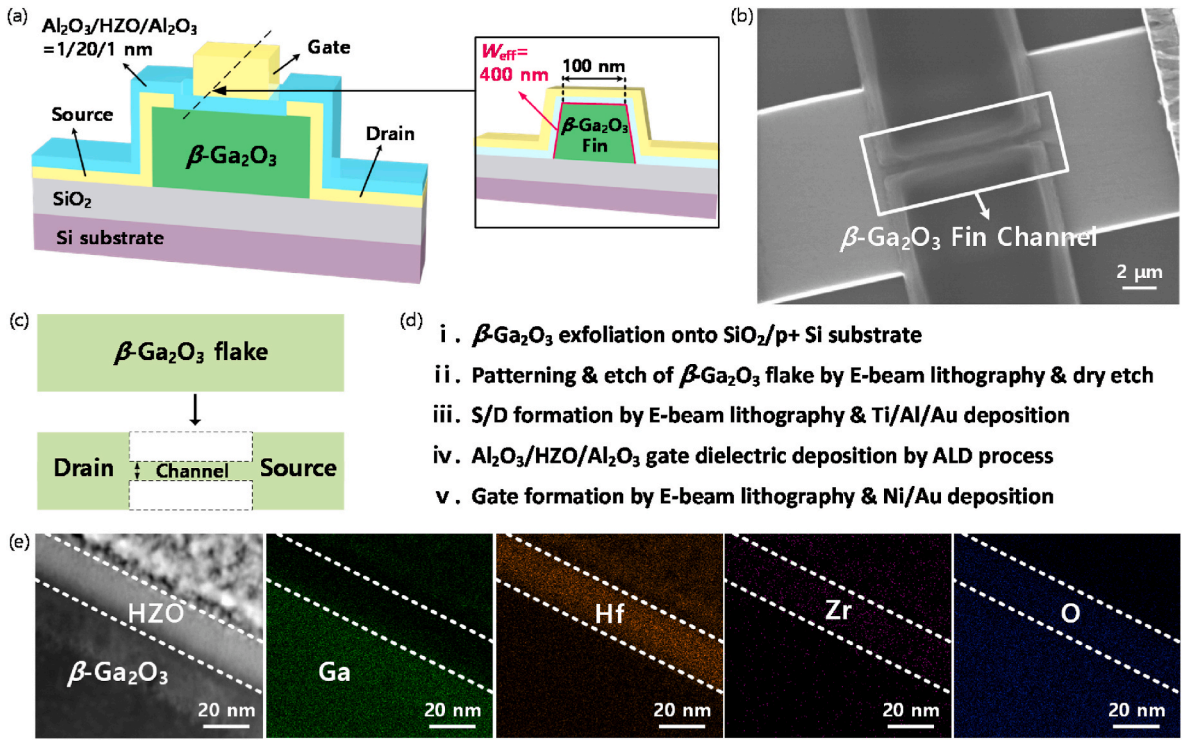


**Fig. 1.** (a) Schematic of HZO/$\beta$-$Ga_2O_3$ Fe-FinFET. (b) SEM image of the fabricated 3D fin structure after RIE etching process. (c) Top-view schematic of fin-structure patterning. (d) Key process steps of device fabrication. (e) TEM images of fabricated HZO/$\beta$-$Ga_2O_3$ layers and EDS elemental mapping with scanning TEM images of Ga, Hf, Zr, and O.

electric fields, high power, and high operating temperatures [5–11]. $\beta$-$Ga_2O_3$ with these properties is particularly attractive for electronic devices exhibiting high-voltage operation in harsh environments [12–14].

Meanwhile, hafnium zirconium oxide (HZO) has shown ferroelectric behavior at high temperatures. The HZO layer is a promising component because it is compatible with complementary metal-oxide-semiconductor (CMOS) in back-end-of-line (BEOL) thermal budget (<400 °C) and exhibits strong ferroelectricity even at very thin thickness (<10 nm) [15–18]. These properties make HZO applicable to various devices, including ferroelectric field-effect transistor (FeFET), ferroelectric random-access memory (FeRAM), and ferroelectric tunnel junction memory (FTJ) [19,20]. FeFETs have been highlighted for their ability to be manufactured simply by inserting a ferroelectric film into the gate stack of a conventional MOSFET. Therefore, FeFETs can exhibit non-volatile memory behaviors while maintaining the same footprint as traditional FETs.

Accordingly, ferroelectric UWBG semiconductor devices have the potential to fill the need for robust electrical operation of neuromorphic applications. A HZO/$\beta$-$Ga_2O_3$ planar FeFET achieved high on-chip learning accuracy at high temperatures, with improved electrical performance [21].

From a channel-architecture perspective, three-dimensional devices such as FinFET have already demonstrated aggressive scaling and clear performance improvements through numerous prior studies. Nevertheless, experimental studies on ferroelectric UWBG FinFETs are still lacking, leaving their potential performance gains, long-term reliability, and potential for neuromorphic applications unexplored.

In this work, HZO/$\beta$-$Ga_2O_3$ ferroelectric FinFET (Fe-FinFET) with a fin width of 100 nm was fabricated. The fabricated Fe-FinFET presented robust electrical performances with accelerated electric dipole switching, high $I_{ON}/I_{OFF}$ ratio, steep subthreshold swing (SS), and large memory window (MW) compared with planar FeFET. TCAD simulation indicated enhanced electric fields in the ferroelectric layer of the Fe-FinFET, a finding that is consistent with the sweep-direction-dependent energy distribution of interface trap density ($D_{it}$). Furthermore, this study demonstrated significantly improved retention time and endurance, and 91.7 % accuracy in a CNN simulation using the CIFAR-10 dataset, for high reliability and expandability to memory devices in the neuromorphic field. The wide bandgap and stable conductivity of the $\beta$-$Ga_2O_3$ channel effectively support HZO polarization switching, thereby contributing to the realization of stable and reliable memory operation.

## 2. Device fabrication

Fig. 1 (a) shows the cross-sectional view of the manufactured device along both channel width and length directions. For fabrication of the HZO/$\beta$-$Ga_2O_3$ Fe-FinFETs, thin nanomembrane flakes were realized by cleaving the $\beta$-$Ga_2O_3$ bulk substrate into small pieces and employing a mechanical exfoliation technique with adhesive tape [18]. The exfoliated flake with a thickness of 130 nm was transferred onto a 270 nm $SiO_2$/p + type Si substrate. Photoresist (PR) was then applied, and electron beam lithography (EBL) was used for fin patterning, followed by development. Dry etching was performed to create a fin-structured channel. Source and drain electrodes were patterned by EBL. Fig. 1 (b) shows the scanning electron microscope (SEM) image of an etched $\beta$-$Ga_2O_3$ channel with a width of 100 nm. Before metallization, an Ar plasma bombardment with a radio frequency power of 100 W was applied to improve the contact resistance ($R_C$) by generating oxygen vacancies to enhance the surface of $\beta$-$Ga_2O_3$ flakes. Ti/Al/Au (15/60/50 nm) metal electrodes were deposited using electron beam evaporation and the lift-off process. A ferroelectric HZO gate stack of $Al_2O_3$/HZO/$Al_2O_3$ (1/20/1.

nm) was deposited by the atomic layer deposition (ALD) process. Applying the 1 nm amorphous $Al_2O_3$ layer on the bottom of the stack achieved better interface quality, and the top $Al_2O_3$ was deposited to avoid degradation of the HZO layer by reaction with other

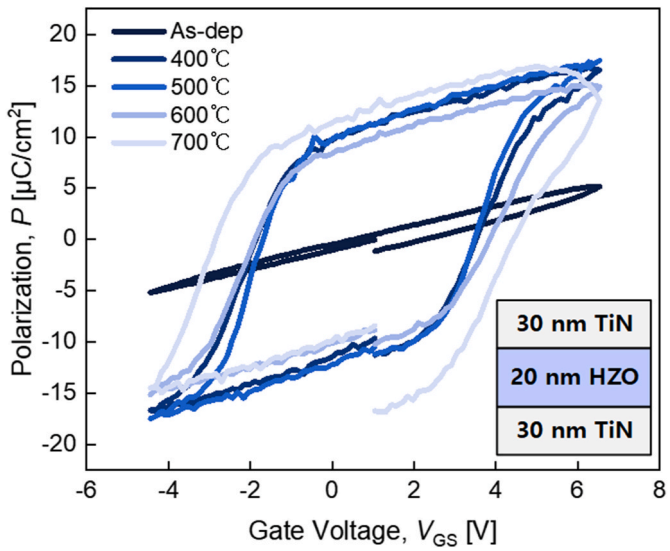


**Fig. 2.** Ferroelectric hysteresis loops of TiN/HZO/TiN capacitor with an HZO thickness of 20 nm annealed at various temperatures.

contamination sources [22]. EBL was carried out for gate patterning, and Ni/Au (50/50 nm) gate metal was formed via electron beam evaporation and lift-off process. The device was suitably fabricated with each part of the $\beta$-$Ga_2O_3$ flake and HZO layer. Their components and accurate locations were confirmed through the scanning transmission electron microscopy (STEM)-energy dispersive X-ray spectroscopy (EDS) mapping images, as shown in Fig. 1 (c). To check the ferroelectricity of HZO, TiN/HZO/TiN (30/20/30 nm) metal-ferroelectric-metal capacitors at different annealing temperatures were fabricated and characterized. As the annealing temperature increases, the formation of the ferroelectric phase and the crystallinity of the HZO layer are enhanced, leading to an increase in remanent polarization ($P_r$) and consequently improved electrical characteristics. These changes are reflected in the polarization–voltage ($P$–$V$) loop results shown in Fig. 2. The devices were annealed at 400–700 °C in a $N_2$ environment for 1 min by rapid thermal annealing, exhibiting clear ferroelectric $P$-$V$ hysteresis loops. The HZO layers of the fabricated Fe-FinFETs and planar FeFETs were annealed at 500 °C, where a clear ferroelectric hysteresis loop appeared.

## 3. Results and discussion

The drain-to-source current ($I_{DS}$)–gate-to-source voltage ($V_{GS}$) curves of Fe-FinFET and planar FeFET are shown in Fig. 3(a) and (b), which are considered normalized to the actual channel width for comparison of the intrinsic device properties.

The exfoliated $\beta$-$Ga_2O_3$ nanomembrane flakes were obtained from the same bulk substrate, and flakes with a uniform thickness were selected and subjected to the same process to ensure device uniformity and comparability. A typical counter-clockwise loop with good polarization switching behavior was observed in the transfer characteristics, indicating reliable polarization switching. The key device performance parameters of Fe-FinFET are significantly superior to those of the planar FeFET. With the fin structure, these characteristics can be improved through enhanced gate controllability of the surrounding gate

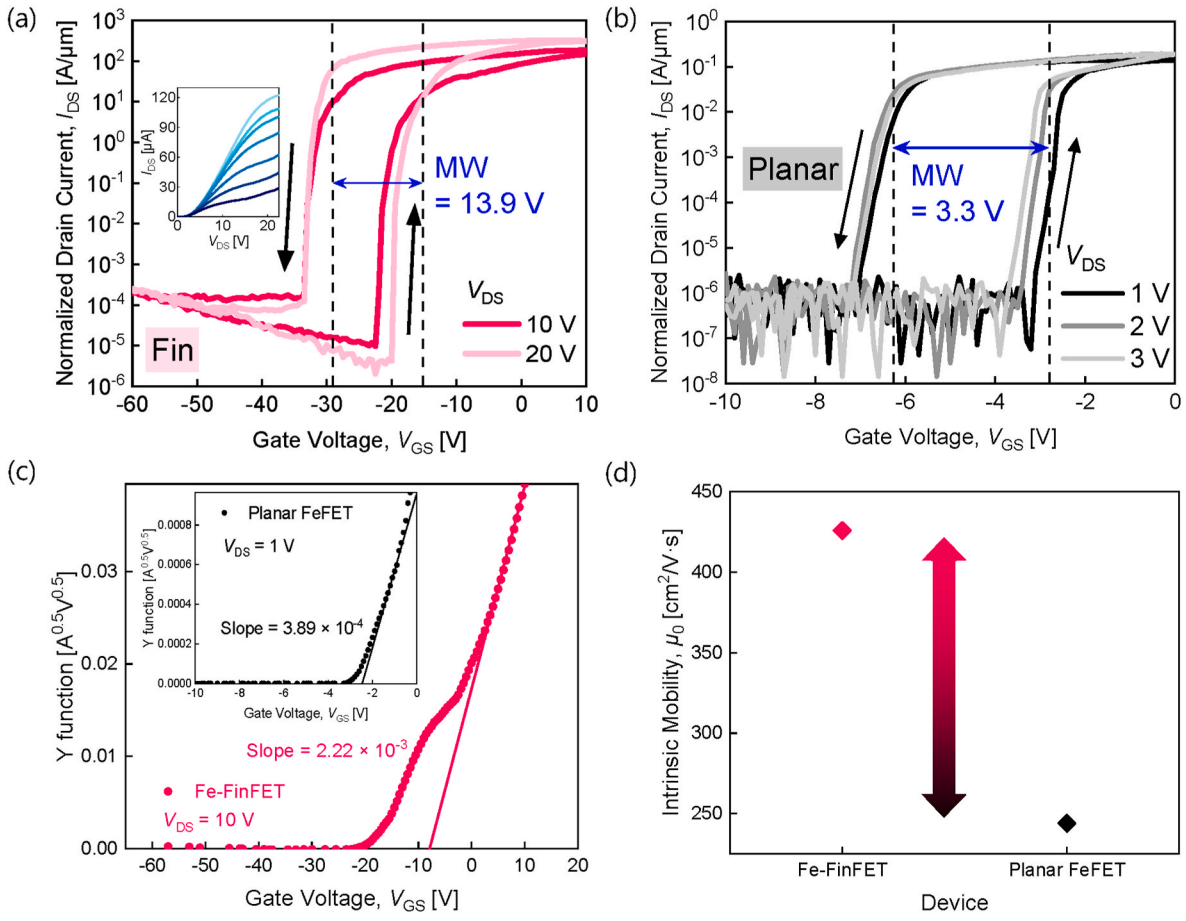


**Fig. 3.** $I_{DS}$-$V_{GS}$ with counter-clockwise hysteresis loop of (a) Fe-FinFET and $I_{DS}$-$V_{DS}$ (inset) and (b) Planar FeFET. (c) Calculated Y-function with gate bias of Fe-FinFET and planar FeFET (inset). (d) Comparison of extracted intrinsic mobility using the Y-function method.

**Table 1**
Comparison of electrical performances of fin and planar structures.

| | Fe-FinFET | Planar FeFET |
|---|---|---|
| $I_{ON}$ [A/μm] | 16.93 | $3 \times 10^{-3}$ |
| $I_{ON}/I_{OFF}$ ratio | $2.3 \times 10^{7}$ | $8.1 \times 10^{4}$ |
| Subthreshold swing, SS [mV/dec] | 110 | 160 |
| Memory Window, MW [V] | 13.9 | 3.3 |

architecture and the strengthened electric field across the HZO layer, as demonstrated by the subsequent TCAD simulation. The wide $V_{GS}$ operation range reinforced by structural modifications is further extended through the incorporation of the UWBG $\beta$-$Ga_2O_3$, ultimately leading to maximized memory window expansion. Indeed, the Fe-FinFET exhibited a MW of 13.9 V at the maximum sweep voltage from −60 V to 10 V on the HZO single layer, which is more than 4.2 times larger than that of planar FeFET at 3.3 V in the linear region, where the MW was extracted from the threshold voltage ($V_T$) difference. A wide MW is required to separate program and erase operations for discrete data storage in practical non-volatile memory applications [19,20]. Moreover, by achieving large MW, the ferroelectric memory can accurately implement multi-level memory states as a neuromorphic device. This multi-state storage capability enables precise modulation of synaptic weight values in neuromorphic computing, contributing to high recognition accuracy and energy-efficient operation [17,23,24]. In this way, the MW of 13.9 V demonstrates that the HZO/$\beta$-$Ga_2O_3$ Fe-FinFET can be a strong candidate for future robust neuromorphic devices. The intrinsic.

mobility($\mu_0$) is extracted using the Y-function method to analyze the impact of structural variation [25]. The Y-function is defined as $Y = \frac{I_{DS}}{\sqrt{g_m}}$, where $g_m$ is transconductance. After obtaining the Y-function (shown in Fig. 3 (c)), $\mu_0$ can be calculated using the slope obtained from the Y-function with $C_{ox}$ and device geometry. The $\mu_0$ of the Fe-FinFET is $4.25 \times 10^2$ $cm^2/V{\cdot}s$, which is about 1.74 times improved compared to the planar FeFET, shown in Fig. 3 (d).

Table 1 presents a comparison of the properties of the HZO/$\beta$-$Ga_2O_3$ Fe-FinFET with planar FeFET. Compared with the planar FeFET, the Fe-FinFET in this study exhibited enhanced electrical performances and excellent memory characteristics under high density.

For the ferroelectric material to fully polarize, a sufficient electric field across the ferroelectric layer is necessary [26]. The electric field enhancement in the conventional FinFET of Si substrate and $HfO_2$ gate insulator was understood using technology computer-aided design (TCAD) simulation (Synopsys Sentaurus) [27]. The simulation condition was $V_G = 5$ V, $V_D = 0$ V, $V_S = 0$ V, and $HfO_2$ layer thickness = 2 nm. As depicted in Fig. 4 (a), the FinFET has a higher electric field across the $HfO_2$ layer than the planar-structured FET; it is confirmed that as the electric field strength increases due to the increase of capacitance density and multidirectional potential gradients inherent in three-dimensional gate structure, polarization switching in HZO films becomes more complete and faster, indicating accelerated domain wall motion and enhanced dipole alignment under stronger fields [28–30].

The surface potential ($\psi_S$) and $D_{it}$ were extracted using the differential body factor (DBT) technique for Fe-FinFETs and planar FeFETs, and the influence of internal field strength on interface trap behavior was investigated. These results are shown in Fig. 4(b) and (c), respectively [31,32]. The high agreement between the extracted results and the general $D_{it}$ model indicates that the experimentally obtained results

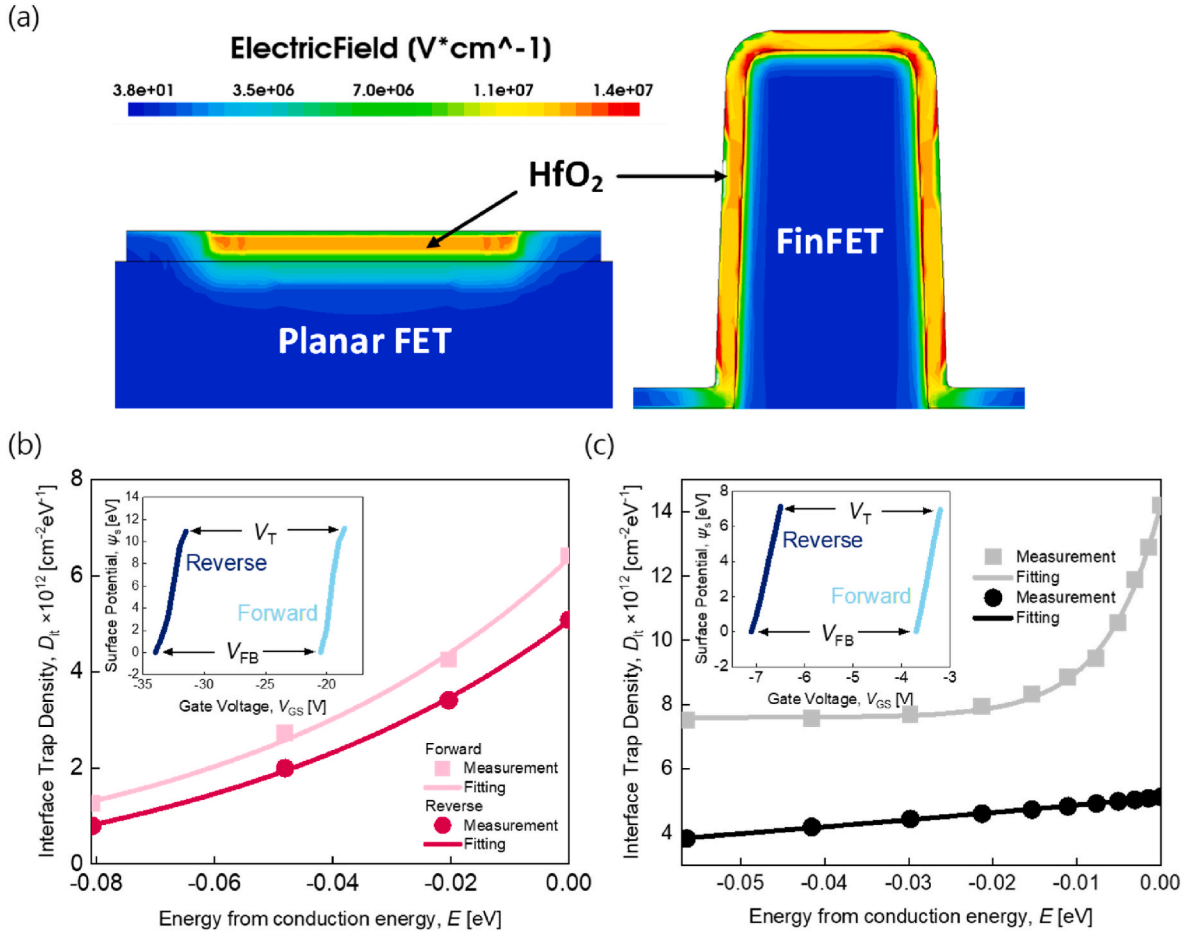


**Fig. 4.** (a) TCAD simulation results for the electric field at the $HfO_2$ layer of planar FET and FinFET. $D_{it}$ and surface potential (inset) for fin and planar structure, shown in (b) and (c), respectively.

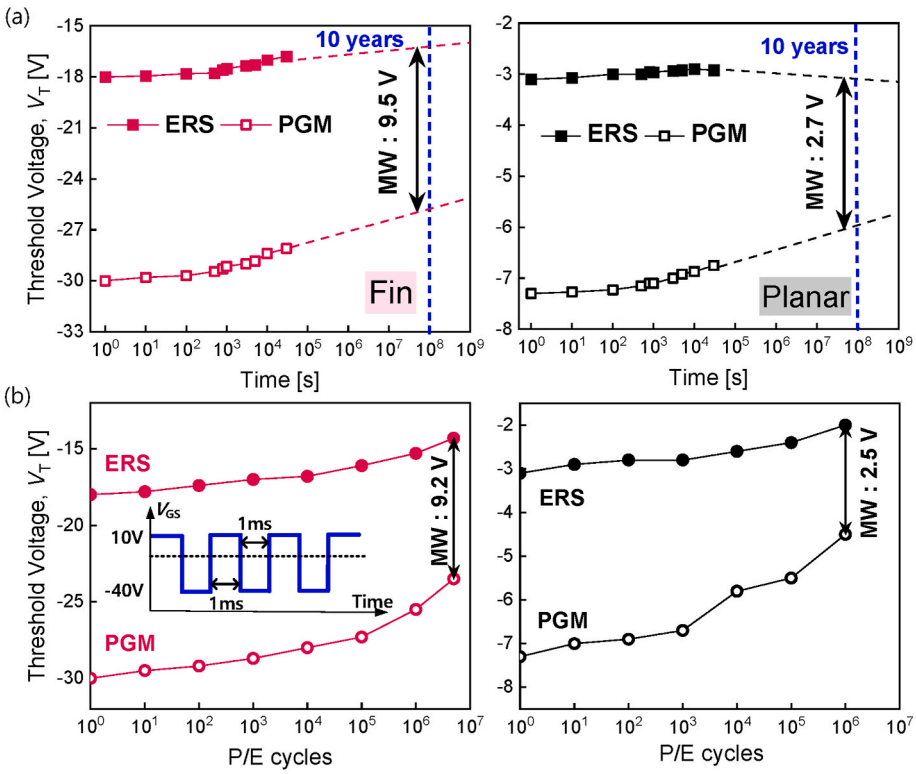


**Fig. 5.** (a) Retention and (b) Endurance characteristics of Fe-FinFET and planar FeFET, respectively.

from DBT from raw data fit the empirical model well, as a superposition of two exponential functions. The Fe-FinFET exhibits a larger $\psi_S$ value within the same voltage range, indicating that the HZO is subjected to a higher electric field and possesses better switching characteristics. Under reverse bias (+→ −), the extracted $D_{it}$ exhibited nearly identical trap levels in both devices, which is attributed to polarization-induced electron repulsion that suppresses carrier capture into the trap states. In contrast, under.

forward bias (−→ +), the Fe-FinFET exhibited a $D_{it}$ of 6.4 × $10^{12}$ $cm^{-2}eV^{-1}$, whereas the planar FeFET with a weaker electric field showed a higher $D_{it}$ of 1.4 × $10^{13}$ $cm^{-2}eV^{-1}$. This can be explained by the relatively weaker polarization, which increases electron injection near the interface and thereby promotes trapping [33,34]. On the other side, in the Fe-FinFET with a strong electric field, the enhanced polarization switching induces more effective carrier displacement and recombination [4,35]. Therefore, the Fe-FinFET, indicating higher electric fields, exhibits enhanced ferroelectric polarization switching and lower $D_{it}$.

Retention and endurance characteristics to investigate the ferroelectric memory reliability of the HZO/$\beta$-$Ga_2O_3$ Fe-FinFET are shown in Fig. 5. According to the retention characteristics, when linearly extrapolated to 10 years, the MW of the Fe-FinFET is maintained over 9.5 V. The endurance performance as a memory device was tested by program/erase (PGM/ERS) cycling with a fixed pulse width of 1 ms and repeated voltages of −40 V and 10 V. The Fe-FinFET shows lower deterioration over up to $10^6$ cycles at larger MW, compared to the planar FeFET. This demonstrates that the FinFET with its tri-gate structure enhances gate-to-channel coupling and electric field concentration, thereby stabilizing ferroelectric polarization and enabling efficient repeated switching.

The learning method was applied to the Canadian Institute for Advanced Research (CIFAR)-10 dataset containing RGB color images to the ResNet18 model as a Convolutional Neural Network (CNN) architecture for evaluation of recognition accuracy [36,37]. The ResNet18 architecture utilizes 17 convolutional layers that perform convolution

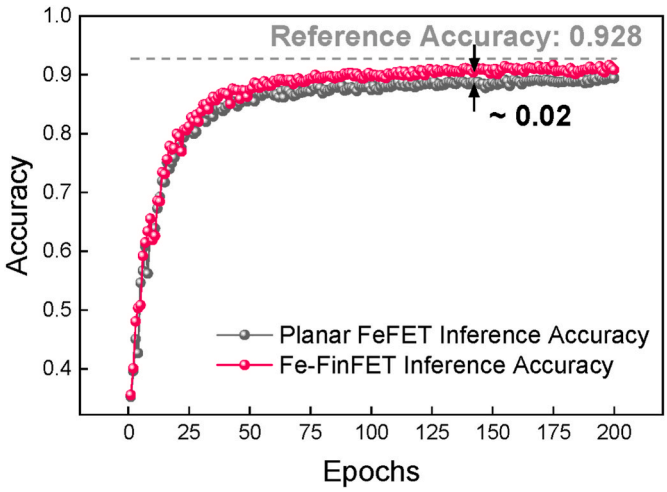


**Fig. 6.** CIFAR-10 accuracy using neural network simulation is performed using 7-bit synaptic weights for Fe-FinFET and 5-bit synaptic weights for planar FeFET.

operations and 10 output neurons to implement one fully connected layer. The simulation was implemented using TensorFlow by adjusting the resolution bits of each synaptic weight and neuron within the neural network, enabling inference [38,39].

Fig. 6 illustrates the validation accuracy during training when the resolution bits of Fe-FinFET and planar FeFET are implemented with the ResNet18 architecture. The validation dataset is sourced from the test dataset to evaluate the neural network's inference accuracy. The resolutions of the Fe-FinFET and planar FeFET devices in terms of synaptic weights in the neural network were measured at 7 bits and 5 bits, respectively, through our experimental programming measurements. By applying voltage pulses and calculating the number of stable and

distinguishable conductivity states, we confirm that Fe-FinFET and planar FeFET exhibited analog weight resolutions of 7 bits (128 states) and 5 bits (32 states), respectively. The inference accuracy of ResNet18, shown as the gray baseline in Fig. 6, is 92.8 %, with both synaptic weights and neurons represented in floating-point resolution [37]. The neural network performance with the Fe-FinFET device achieved an accuracy of 91.7 %, while that of the planar FeFET was 89.7 %. This suggests that Fe-FinFETs enable finer weight granularity, resulting in more precise updates and consistently higher accuracy across pulse epochs. Higher accuracy of Fe-FinFET-based neural networks reflects the device's capability to support reliable synaptic updates, which is advantageous for implementing biologically plausible learning rules and achieving high-performance neuromorphic computing systems.

## 4. Conclusion

This study presented the first HZO/$\beta$-$Ga_2O_3$ Fe-FinFET with a fin width of 100 nm. We report that the UWBG Fe-FinFETs achieved low SS of 110 mV/dec, high Ion/Ioff ratio of $2.3 \times 10^7$, and notably a wide MW of 13.9 V in a single ferroelectric layer, which was validated through simulations and $D_{it}$ compared to planar FeFETs. In addition, highly reliable retention and endurance characteristics are confirmed by electrical measurements, and high accuracy is achieved through CIFAR-10 simulation, confirming high reliability for device operation. Notably, this study demonstrated that the integration of HZO/UWBG $\beta$-$Ga_2O_3$ with the FinFET architecture enabled high-performance and reliable ferroelectric memory operation, highlighting its potential for implementing high-performance synaptic memory applications. In this study, the relatively high operation voltage and modest switching speed reflect limits in VT control and interfacial/ferroelectric switching kinetics. To address these limitations, comprehensive device- and process-level co-optimization—spanning the gate stack, ferroelectric/semiconductor thicknesses, interface quality, and operating schemes—will be required within the scaled device architecture, and further study is needed.

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## CRediT authorship contribution statement

**Seohyeon Park:** Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Resources, Project administration, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Jaewook Yoo:** Writing – review & editing, Formal analysis, Data curation, Conceptualization. **Seokjin Oh:** Validation, Software. **Hongseung Lee:** Software. **Minah Park:** Investigation. **Seongbin Lim:** Investigation. **Soyeon Kim:** Visualization. **Sojin Jung:** Visualization. **Bongjoong Kim:** Resources. **Keun Heo:** Resources. **Taehwan Moon:** Methodology, Formal analysis, Conceptualization. **TaeWan Kim:** Resources. **Mengwei Si:** Resources, Data curation. **Peide D. Ye:** Resources. **Hagyoul Bae:** Supervision, Conceptualization.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

Data will be made available on request.

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