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First demonstration of robust tri-gate β-Ga_2O_3 nano-membrane field-effect transistors

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Abstract

Nano-membrane tri-gate β-gallium oxide (β-Ga_2O_3) field-effect transistors (FETs) on SiO_2/Si substrate fabricated via exfoliation have been demonstrated for the first time. By employing electron beam lithography, the minimum-sized features can be defined with the footprint channel width of 50 nm. For high-quality interface between β-Ga_2O_3 and gate dielectric, atomic layer-deposited 15 nm thick aluminum oxide (Al_2O_3) was utilized with tri-methyl-aluminum (TMA) self-cleaning surface treatment. The fabricated devices demonstrate extremely low subthreshold slope (*SS*) of 61 mV dec^{-1}, high drain current (I_{DS}) ON/OFF ratio of 1.5×10^9, and negligible transfer characteristic hysteresis. We also experimentally demonstrated robustness of these devices with current–voltage (*I–V*) characteristics measured at temperatures up to 400 °C.

Keywords: tri-gate, β-Ga_2O_3 FETs, exfoliation, wide bandgap, atomic layer deposition, single-channel, multi-channel

(Some figures may appear in colour only in the online journal)

1. Introduction

β-Ga_2O_3 is one of the promising materials for next-generation power electronics owing to its ultra-wide bandgap of 4.6–4.9 eV, high breakdown electric field of 8 MV cm^{-1}, high electron mobility of 100–150 $cm^2\ V^{-1}{\cdot}s^{-1}$, and sustainability for high-temperature operation and mass production with low-cost fabrication [1–8]. In addition, the β-Ga_2O_3 material has a higher Baliga's figure-of-merit (FOM) than that of silicon carbide (SiC) and gallium nitride (GaN) [9, 10]. Owing to these advantages, monolithic β-Ga_2O_3 transistors could also be considered for high-temperature operation in harsh environments. In particular, stable operation of electronic devices in severe conditions, mainly at high temperatures, is indispensable for many applications in the defense, automotive, nuclear instrumentation, and aerospace fields [11, 12]. Recently, several studies have demonstrated improved electrical performances of β-Ga_2O_3 FETs by using double-gate [13], multi-channel with wrap-gate [14], vertical channel [15], back-gate [16], and recessed-gate [17, 18] devices. In particular, among these advanced technologies, structure innovation to enhance gate controllability to boost higher current density and suppress interface or short-channel effect becomes critical during device research [19, 20]. There are still opportunities to achieve better switching characteristics, higher integration density, and lower power consumption in β-Ga_2O_3 materials and device development.

In this study, the fabrication and performance of tri-gate β-Ga_2O_3 FETs with single and multi channel structures formed from nano-membranes are presented. In the single channel structure, a narrow channel with a width (W_{ch}) of 50 nm is fabricated to exploit the high ON/OFF ratio of I_{DS}

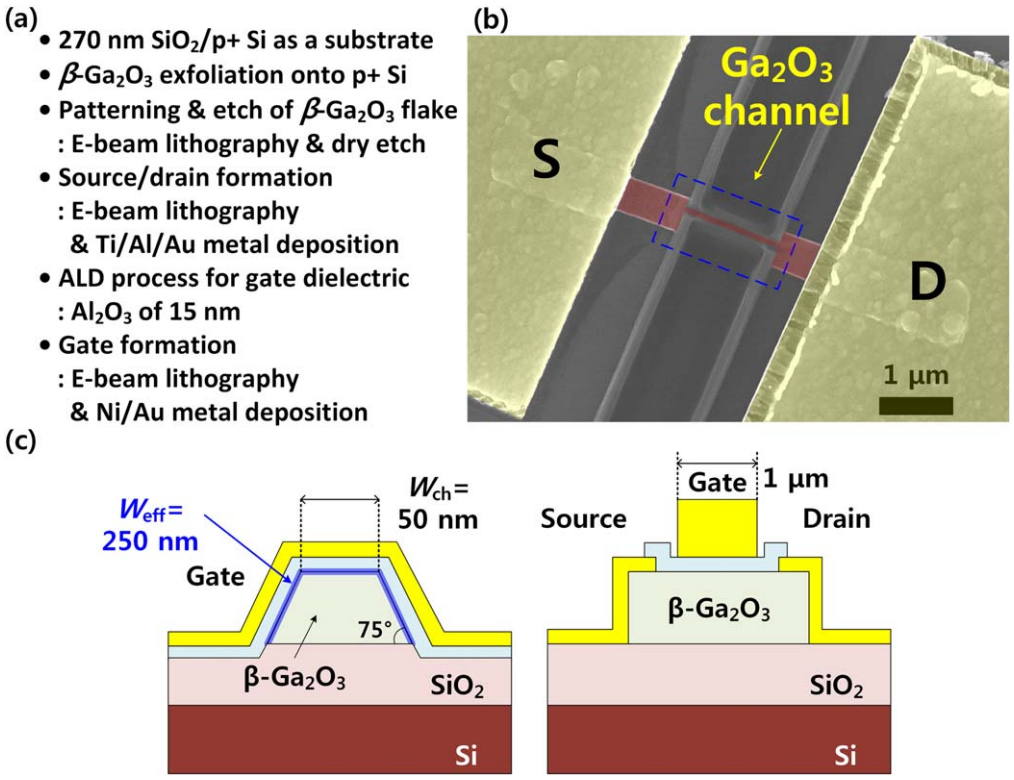

Figure 1. (a) Process flow for device fabrication of exfoliated tri-gate β-Ga_2O_3 nano-membrane FETs with the top-gate structure. (b) SEM image of a fabricated device. (c) Cross-sectional schematics along both channel width and length directions.

and superior subthreshold slope, while maintaining reliable performance at temperature from room temperature (RT) to 400 °C.

2. Device fabrication

Figure 1(a) lists the key fabrication steps for the tri-gate nano-membrane β-Ga_2O_3 FETs on the SiO_2/Si substrate. For the fabrication of the top-gate devices, thin (100) β-Ga_2O_3 nano-membranes with a Sn doping concentration of 2.7×10^{18} cm^{-3} was transferred from the bulk β-Ga_2O_3 substrate onto a p + Si wafer with a 270 nm SiO_2 as gate dielectric. The tri-gate active channel region was defined by electron (e)-beam lithography and the dry-etch process. To form narrower β-Ga_2O_3 with tri-gate structure, we used a BCl_3/Ar gas mixture in an inductively coupled plasma-reactive ion etching (ICP-RIE) system (Panasonic E620 Etcher) for 15 min [21]. The etching rate of (100) β-Ga_2O_3 is about 10 nm min^{-1} under process conditions: RF power of 100 W; BCl_3 flow of 15 sccm; Ar flow of 60 sccm; and pressure of 0.6 Pa. Subsequently, the source (S) and drain (D) regions were formed via e-beam lithography patterning, Ti/Al/Au (15/60/50 nm) metallization, and lift-off process. No post-deposition thermal annealing was performed. By employing the atomic layer deposition (ALD) process, high-quality Al_2O_3 gate dielectric was deposited to minimize gate leakage current and high-quality interface by self-cleaning effect using TMA as the precursor [22, 23]. Subsequently, e-beam lithography was carried out for gate patterning and Ni/Au (50/80 nm) metal gate was deposited via an e-beam evaporator. Figure 1(b) presents the scanning electron microscope (SEM) image showing the etched β-Ga_2O_3 channel with W_{ch} of 50 nm, a gate length (L_G) of 1 μm, and a channel height (H_{ch}) of 95 nm. As the fabricated device has a 3D tri-gate structure, the total effective channel width (W_{eff}) is approximately 250 nm, which is 5 times wider than the footprint W_{ch} of 50 nm. Figure 1(c) shows the cross-sectional view of the fabricated device along both channel width and length directions. Using atomic force microscopy (AFM), the measured physical thickness of the exfoliated β-Ga_2O_3 nano-membrane is approximately 95 nm.

3. Experimental results and discussion

Figure 2(a) shows the measured transfer characteristics (I_{DS}–V_{GS}) of the fabricated tri-gate β-Ga_2O_3 FET with W_{eff} of 250 nm and L_G of 1 μm, showing the following excellent electrical performances: (1) $I_{ON} = 350$ mA mm^{-1} normalized with the W_{eff}; (2) $I_{ON}/I_{OFF} = 1.5 \times 10^9$; (3) $SS_{min} = 61$ mV dec^{-1}; (4) DIBL = 12 mV V^{-1}; (5) $V_{hys} = 30$ mV. The electrical characterizations were performed using a Keysight B1500 semiconductor parameter analyzer, a Keithley 4200-SCS parameter analyzer with a high-temperature measurement system (Micromanipulator H1000 Thermal Chuck System), and a Cascade Summit probe station. Figure 2(b) shows the measured output characteristics (I_{DS}–V_{DS}) as a function of V_{GS} from 0 to –20 V. A maximum drain current density (I_{DS_max}) of 350 mA mm^{-1} in the fabricated device on

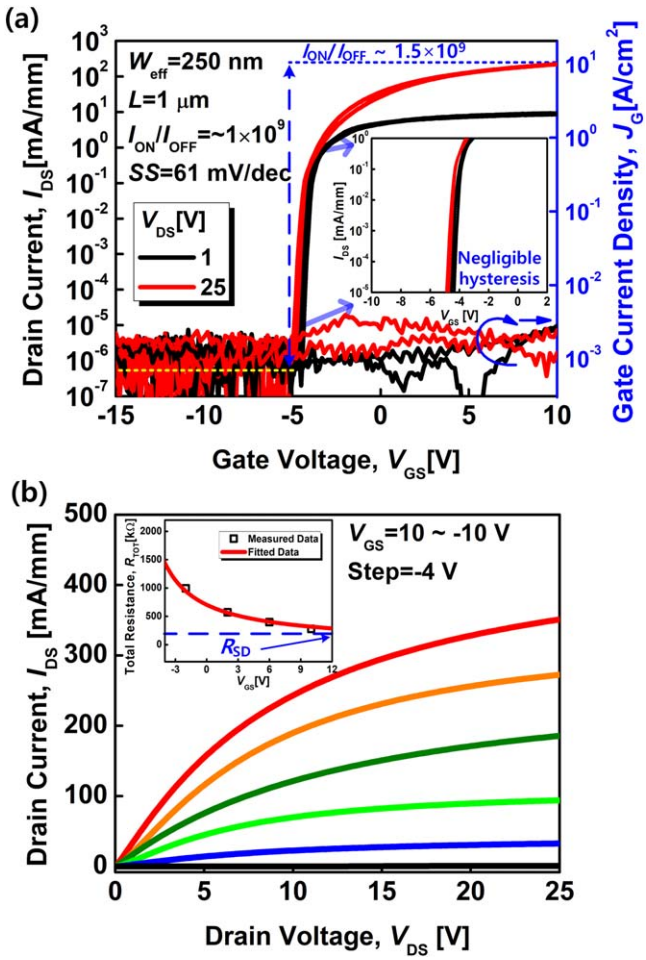

Figure 2. (a) Measured I_{DS}–V_{GS} transfer characteristics and (b) I_{DS}–V_{DS} output characteristics of the fabricated tri-gate β-Ga_2O_3 FET.

the SiO_2/Si substrate is obtained, which is higher than that obtained in our previous study of top-gate devices on SiO_2/Si substrate [24]. In this study, improvements, i.e. steep *SS* and high I_{ON}/I_{OFF} ratio were obtained by using SiO_2/Si substrate instead of diamond substrate in terms of cost effectiveness and process simplification, but we expect that the tri-gate β-Ga_2O_3 FETs on diamond substrate could give rise to further improved I_{DS_max} due to its high thermal conductivity (κ = 1000–2200 W m^{-1}·K^{-1}), as a further study. This proposed tri-gate structure enables to control β-Ga_2O_3 channel from three sides of the gate and improve the gate electrostatics significantly as in Si CMOS technology. The threshold voltage (V_T) is determined to be −2.8 V by the constant current method. The parasitic source/drain resistances (R_{SD}) is obtained by extrapolating V_{GS} based on channel resistance method (CRM) as shown in the inset of figure 2(b) [25]. The R_C and sheet resistance (R_{SH}) is extracted to be 8.0 Ω·mm and 6.2 kΩ/□, respectively. Further studies on β-Ga_2O_3 contacts are highly demanded in the development of β-Ga_2O_3 device technology [26].

The measured I_{DS}–V_{GS} characteristics of the fabricated tri-gate β-Ga_2O_3 FET on the SiO_2/Si substrate measured at various temperatures ranging from RT to 400 °C are shown in figure 3 with negligible hysteresis. Although I_{OFF} starts to

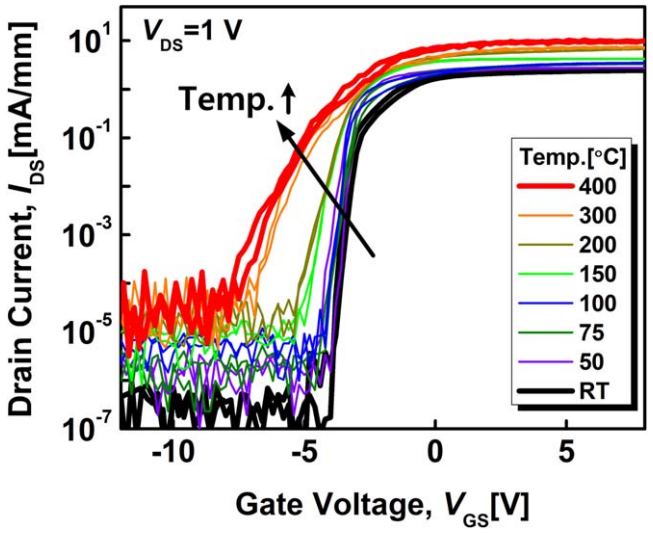

Figure 3. Measured I_{DS}–V_{GS} characteristics of the fabricated tri-gate β-Ga_2O_3 FETs on SiO_2/Si substrate at various temperatures ranging from RT to 400 °C.

gradually increase as the temperature increases, our proposed tri-gate β-Ga_2O_3 FETs have more stable characteristics for temperatures up to 400 °C compared to previous results [6, 13]. The variations in the extracted *SS*, V_T, field-effect mobility (μ_{FE}), and I_{ON}/I_{OFF}, as a function of temperature are plotted in figure 4. The value of *SS* increases from 61 mV dec^{-1} to 710 mV dec^{-1} and V_T shifts toward a negative direction due to thermally excited carriers from interface states between the channel and the gate dielectric, as shown in figures 4(a) and (b). The interface trap density (D_{it} [eV^{-1} cm^{-2}]) of the fabricated devices is extracted to 1.0 × 10^{11} eV^{-1} cm^{-2} at RT. The significant increase of *SS* beyond Boltzmann thermal limit indicates a large amount D_{it} of 1.6 × 10^{13} eV^{-1} cm^{-2} could be activated at 400 °C. In addition, μ_{FE} decreases also due to the increased D_{it} at the interface and the phonon scattering in channel at high temperatures as shown in figure 4(c) [6, 13, 27]. We should also note that, even at 400 °C, I_{ON}/I_{OFF} was observed to be approximately 3 × 10^5, as shown in figure 4(d). The tri-gate β-Ga_2O_3 FETs with ALD Al_2O_3 as gate dielectric demonstrate robust electrical performances at high temperatures. Furthermore, the measured *I*–*V* characteristics at RT were again obtained after cooling the device from high temperature to RT.

As shown in figure 5, we also demonstrated the feasibility of the multi-channel tri-gate β-Ga_2O_3 FETs for a high integration density. The inset shows the SEM image for top view of the fabricated device with 3 channels. In case of multi-channel devices, overall device performances are also comparable to the single-channel devices. To provide clear evidences for advantages of tri-gate β-Ga_2O_3 FETs, we fabricated three types of devices with different gate structures ((i) tri-gate, (ii) planar-gate, and (iii) bottom-gate) under same process conditions and investigated the impact of the tri-gate β-Ga_2O_3 FETs via comparison with other devices, as shown in figure 6. Table 1 shows the comparison data of the fabricated devices with different gate structures. It is noteworthy

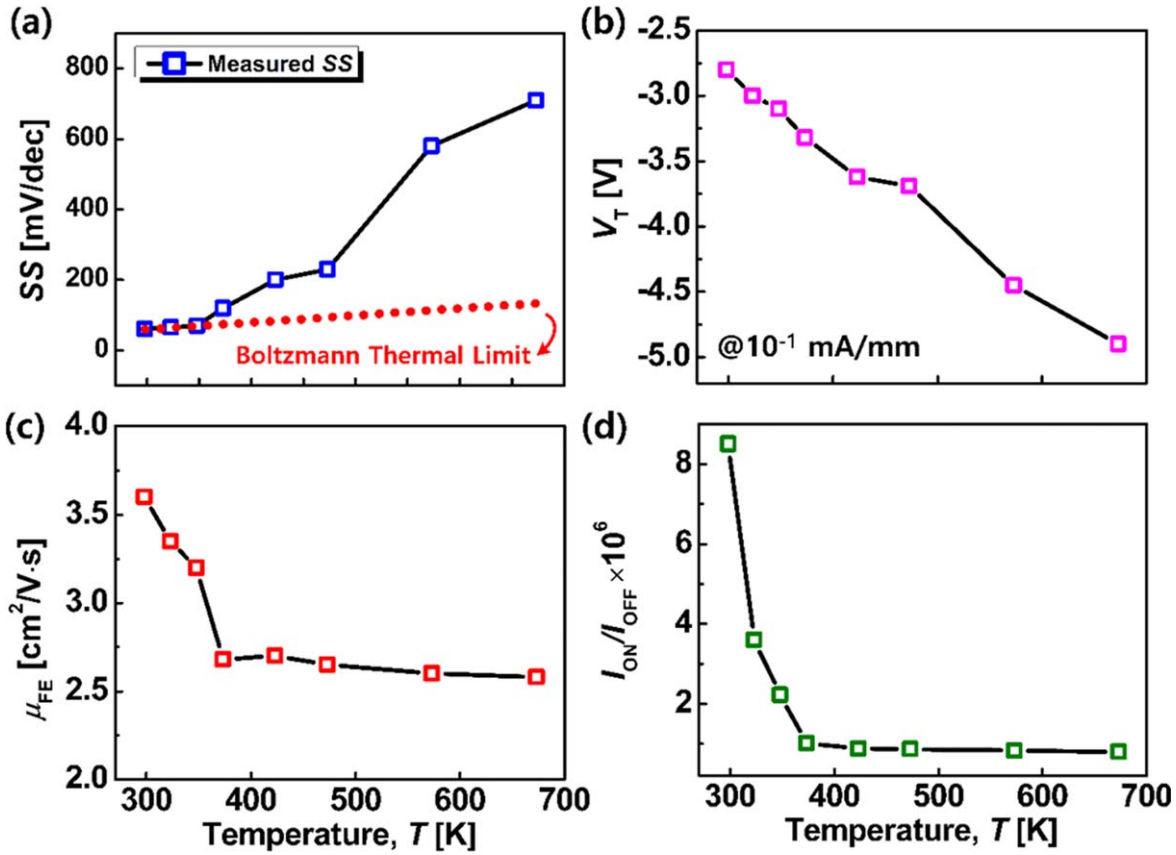

Figure 4. Temperature dependences (RT–400 °C) at $V_{DS} = 1$ V of typical device parameters such as (a) *SS* (dashed line: Boltzmann thermal limit of *SS*), (b) V_T, (c) μ_{FE}, and (d) I_{ON}/I_{OFF} of the tri-gate β-Ga_2O_3 FETs on the SiO_2/Si substrate.

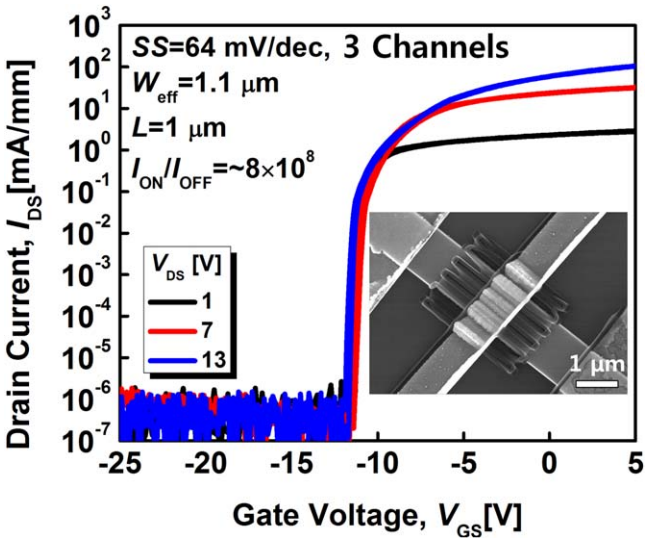

Figure 5. Measured I_{DS}–V_{GS} characteristics of the fabricated β-Ga_2O_3 FETs with multi channels. Inset shows SEM image for top view of the fabricated device with 3 channels.

that the tri-gate β-Ga_2O_3 FETs have high channel ratio (W_{eff}/perimeter of channel width (W_{peri})) of 0.85 and aspect ratio (AR) of 2 resulting in better electrical performances such as I_{ON}/I_{OFF}, *SS*, and D_{it} [28, 29]. In this regard, minimizing the device degradation caused by interface states and modulating the effective charges from β-Ga_2O_3 channel in tri-gate β-Ga_2O_3 FETs can be important since the switching characteristics are very strongly influenced by interface between β-Ga_2O_3 and bottom SiO_2 substrate.

A benchmark of the fabricated tri-gate β-Ga_2O_3 FETs is summarized in table 2. The overall electrical performances of the fabricated tri-gate β-Ga_2O_3 FETs with a single channel are improved over different types of devices reported previously. In particular, our proposed device is highly scalable with an active channel area of 0.05 μm^2 by employing an extremely scaled β-Ga_2O_3 structure. The D_{it} of the fabricated device shows a high-quality interface compared with previously reported results [30, 31]. In the positive bias stress experiments, we also found accumulation of positive charges at the bottom-interface (or edges) leads to the degradation of *SS* and negative shift of V_T [32]. Therefore, more comprehensive study is required for the investigation of stress-induced instability considering the device geometry, as a further study.

4. Conclusion

In this study, top-gate tri-gate nano-membrane β-Ga_2O_3 FETs were successfully demonstrated for the first time. By adopting the single fin-like structure with a W_{ch} of 50 nm, the fabricated devices have improved subthreshold slope and I_{ON}/I_{OFF}

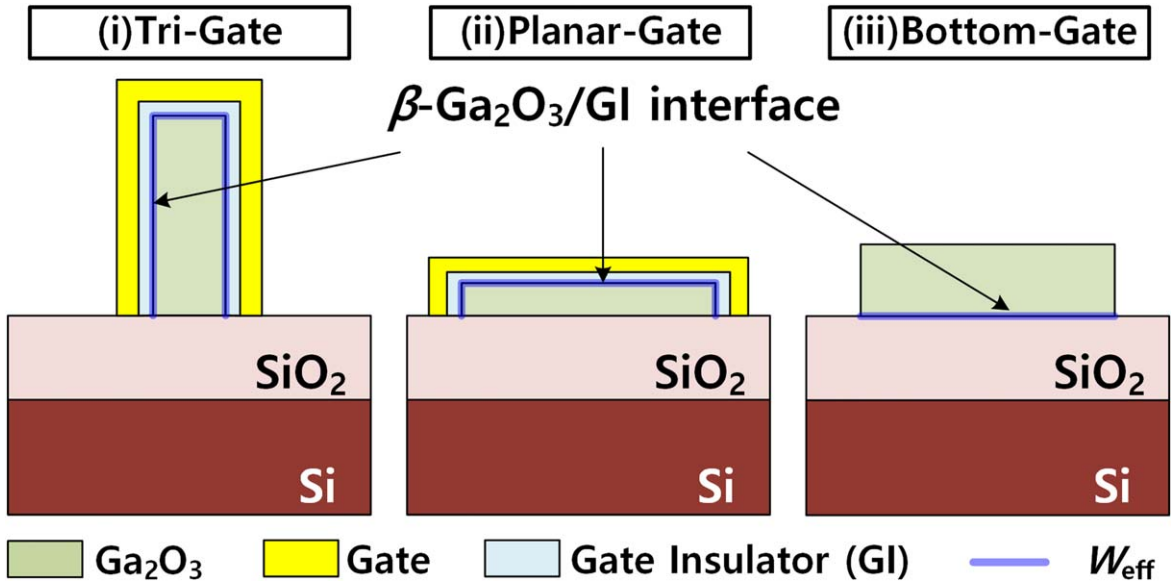

Figure 6. Schematics of cross-sectional view for the fabricated devices with different gate structures: (i) tri-gate, (ii) planar-gate, (iii) bottom-gate.

Table 1. Comparison data with different gate structures.

@V_{DS} = 1 V	Sample #1	Sample #2	Sample #3
Structure	Single channel	Planar	Bottom-Gate
Gate dielectric	Al_2O_3	Al_2O_3	SiO_2
I_{ON}/I_{OFF}	$\sim 1.3 \times 10^7$	$\sim 9.5 \times 10^6$	$\sim 1.2 \times 10^6$
SS_{min} [mV dec^{-1}]	61	100	250
Type	Flake	Flake	Flake
D_{it} [eV^{-1}cm^{-2}]	$\sim 1 \times 10^{11}$	$\sim 9 \times 10^{11}$	$\sim 1 \times 10^{12}$
W_{eff}	250 nm	1 μm	1.5 μm
Channel ratio (W_{eff}/W_{peri})	0.85	0.55	0.45
Aspect ratio (AR)	2	0.12	0.1

Table 2. Benchmarking for electrical performances of Ga_2O_3 FETs.

	This work	Reference [13]	Reference [14]	Reference [15]
I_{ON}/I_{OFF} (Max.)	$\sim 1.5 \times 10^9$	$\sim 7 \times 10^7$	$\sim 5 \times 10^5$	$\sim 1 \times 10^9$
SS_{min} [mV dec^{-1}]	61	70	158	200
# of Ch.	Single	—	48	20
Type	Flake	Flake	MOVPE	Epitaxial growth
D_{it} (Max.) [eV^{-1} cm^{-2}]	$\sim 1 \times 10^{11}$	—	$\sim 1 \times 10^{12}$	—
Temp.	RT $\sim$ 400 °C	RT $\sim$ 250 °C	RT	RT
V_{hys}	30 mV	30 mV	700 mV	100 mV
I_{DS_max}	350 mA mm^{-1}	1 mA mm^{-1}	3 mA mm^{-1}	1 kA cm^{-2}
W_{eff}	250 nm	7 μm	24 μm	50 μm

resulting from enhanced top gate controllability. Moreover, the fabricated devices demonstrate sustainable reliability under high temperatures of up to 400 °C, validating its use in applications involving harsh environments. Multi-channel devices also represent improved electrical performances comparable to single-channel devices for high integration density. Consequently, we expect that tri-gate β-Ga_2O_3 FETs have the potential as a low-cost and high-performance power

device technology after the establishment of epitaxy materials.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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