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Letter
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Steep-Slope WSe_2 Negative Capacitance Field-Effect Transistor

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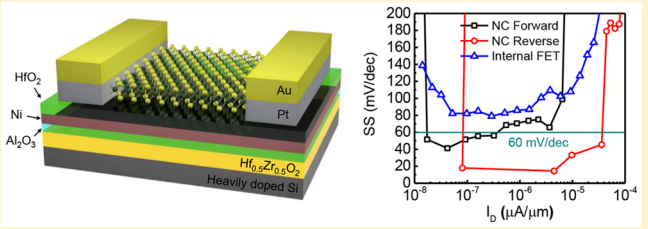
Supporting Information

ABSTRACT: P-type two-dimensional steep-slope negative capacitance field-effect transistors are demonstrated for the first time with WSe_2 as channel material and ferroelectric hafnium zirconium oxide in gate dielectric stack. F4-TCNQ is used as p-type dopant to suppress electron leakage current and to reduce Schottky barrier width for holes. WSe_2 negative capacitance field-effect transistors with and without internal metal gate structures and the internal field-effect transistors are compared and studied. Significant SS reduction is observed in WSe_2 negative capacitance field-effect transistors by inserting the ferroelectric hafnium zirconium oxide layer, suggesting the existence of internal amplification (~10) due to the negative capacitance effect. Subthreshold slope less than 60 mV/dec (as low as 14.4 mV/dec) at room temperature is obtained for both forward and reverse gate voltage sweeps. Negative differential resistance is observed at room temperature on WSe_2 negative capacitance field-effect-transistors as the result of negative capacitance induced negative drain-induced-barrier-lowering effect.



KEYWORDS: *Tungsten diselenide, negative capacitance, ferroelectric oxide, steep slope, internal metal gate*

The so-called Boltzmann Tyranny (associated with the Boltzmann distribution of carriers) defines the fundamental thermionic limit of the subthreshold slope (SS) of a metal-oxide-semiconductor field-effect transistor (MOSFET) at 60 mV/dec at room temperature, which prohibits the decrease of the supply voltage and power consumption. Negative capacitance FETs (NC-FETs) have been proposed and attracted much attention to overcome this thermionic limit of SS.[1−14] In an NC-FET, the insulating ferroelectric material layer served as a negative capacitor so that channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV/dec at room temperature. Transition metal dichalcogenides (TMDs) have been intensely explored as two-dimensional (2D) semiconductors for future device technologies because of the atomically ultrathin body for the ideal electrostatic control of the channel. It would be highly desirable to integrate ferroelectric insulator and 2D ultrathin channel materials as 2D NC-FETs to achieve subthermionic SS for low power dissipation and excellent immunity to short channel effects for transistor scaling. Very recently, n-type 2D NC-FETs with molybdenum disulfide (MoS_2) as channel material and Si CMOS compatible Hf-based ferroelectric oxide as gate dielectric have been demonstrated with subthermionic SS at room temperature.[10−14] However, both p-type and n-type FETs are required for complementary metal-oxide-semiconductor (CMOS) device technology but no p-type 2D NC-FETs with sub-60 mV/dec subthreshold slope was reported. Tungsten diselenide (WSe_2) is one of the most studied TMDs as a highly promising p-type channel material, because of its balanced conduction and valence band edges and high hole mobility.[15−22] Intrinsic WSe_2 FETs usually exhibit ambipolar transport behavior due to the band alignment of metal to WSe_2 near the middle of the bandgap, so that doping technique is required to obtain high performance WSe_2 transistors. P-type chemical doping in WSe_2 such as NO_2 and 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F4-TCNQ) has been studied to enhance the hole transport and to reduce the Schottky barrier width.[15,20]

In this Letter, we demonstrate for the first time steep-slope p-type WSe_2 NC-FETs by combining ferroelectric hafnium zirconium oxide (HZO) gate stack and F4-TCNQ p-type chemical doping. The effect of internal metal gate (IMG) on the performance of WSe_2 NC-FET is also studied by inserting a metal layer between ferroelectric HZO and the positive gate oxide. For WSe_2 NC-FET without IMG and after F4-TCNQ doping, minimum SS of 40.2 mV/dec and less than 60 mV/dec are achieved for both forward and reverse gate-to-source voltage (V_{GS}) sweeps on the p-type WSe_2 NC-FETs with a low hysteresis of less than 0.2 V. For WSe_2 NC-FETs without IMG and before F4-TCNQ doping, the transistors exhibit ambipolar transport behavior and a high drain current (I_D) is achieved on nFET due to the enhanced electric field from the ferroelectricity in the gate oxide. Negative differential resistance (NDR), correlated to the drain coupled negative capacitance effect, is also observed on both n-type and p-type NC-FETs. For WSe_2 NC-FET with IMG and after F4-TCNQ doping, SS_{For} = 41.2 mV/dec and SS_{Rev} = 14.4 mV/dec are achieved

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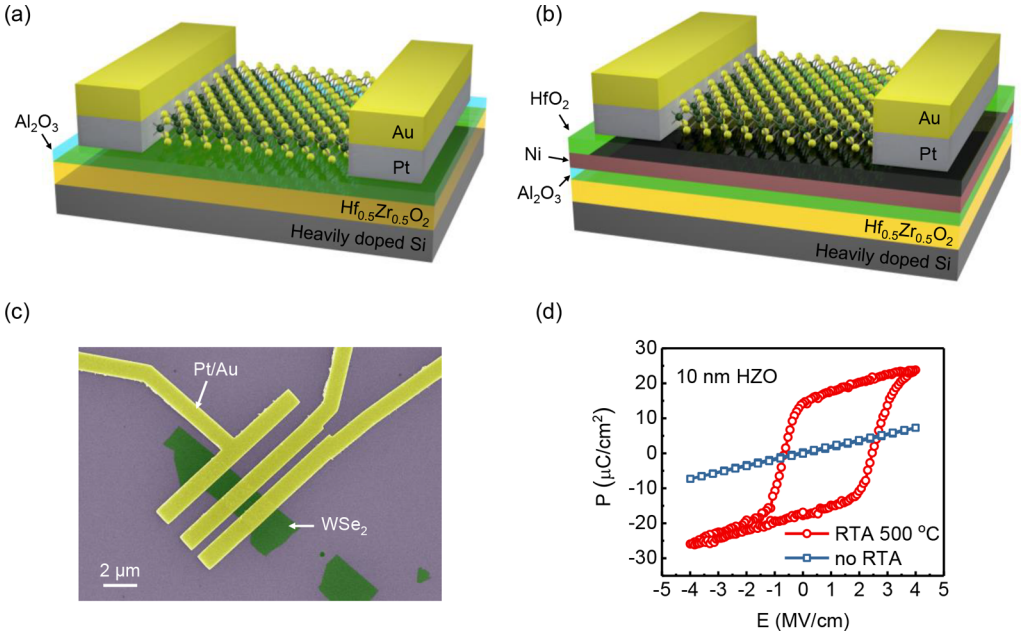

Figure 1. (a) Schematic view of a WSe_2 NC-FET without IMG. The gate stack includes the heavily doped Si as gate electrode, 20 nm HZO as the ferroelectric capacitor, and 2 nm Al_2O_3 as capping layer. The 30 nm Pt/50 nm Au are used as source/drain electrodes. (b) Schematic view of a WSe_2 NC-FET with IMG. The gate stack includes the heavily doped Si as gate electrode, 20 nm HZO, 3 nm Al_2O_3, 20 nm Ni as IMG, and 10 nm HfO_2 as the gate dielectric for internal FET. The 30 nm Pt/50 nm Au are used as source/drain electrodes. (c) False-color top-view SEM image of a representative WSe_2 NC-FET. (d) Polarization versus electric field for ferroelectric MIM (TiN/10 nm HZO/TiN) capacitor with 500 °C RTA and without RTA. HZO exhibits clear ferroelectricity after 500 °C annealing.

with negative hysteresis due to the ferroelectric switching, while the SS of internal WSe_2 FET is 79.1 mV/dec. The SS of the WSe_2 NC-FET with IMG is much smaller than the SS measured from the internal WSe_2 FET, suggesting the existence of internal amplification by the ferroelectric HZO.

The experimental device schematic of a WSe_2 NC-FET without IMG is shown in Figure 1a, which consists of few-layer WSe_2 as channel, 2 nm amorphous aluminum oxide (Al_2O_3) layer and 20 nm polycrystalline HZO layer as the gate dielectric, heavily doped silicon substrate as the gate electrode and Pt/Au source/drain contacts. The device schematic of a WSe_2 NC-FET with IMG is shown in Figure 1b, which consists of few-layer WSe_2 as channel, 20 nm polycrystalline HZO, 3 nm amorphous Al_2O_3, 20 nm Ni layer as IMG and 10 nm HfO_2 as gate dielectric of internal FET, heavily doped silicon substrate as the gate electrode and Pt/Au source/drain contacts. HZO was deposited by atomic layer deposition (ALD) as a ferroelectric insulator layer[23] on a heavily doped silicon substrate after standard solvent clean and hydrogen fluoride passivation. $Hf_{1-x}Zr_xO_2$ film was deposited at 250 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), and H_2O as the Hf precursor, Zr precursor, and O precursor, respectively. The $Hf_{1-x}Zr_xO_2$ film with $x = 0.5$ was achieved by controlling HfO_2/ZrO_2 cycle ratio to be 1:1. Another 2 or 3 nm Al_2O_3 layer was in situ deposited at 250 °C, using $Al(CH_3)_3$ as Al precursor and H_2O as oxygen precursor, as an encapsulation layer to prevent the degradation of HZO by the reaction with moisture in air and the amorphous Al_2O_3 layer was also used for capacitance matching and gate leakage current reduction through polycrystalline HZO. A rapid thermal annealing (RTA) in nitrogen ambient was then performed for 1 min at 500 °C to enhance the ferroelectricity, as shown in Figure 1d. Clear dielectric to ferroelectric transition can be seen after annealing on the metal−insulator−metal (MIM, TiN/10 nm HZO/TiN) capacitor. As the working speed of NC-FETs is directly related with the ferroelectric polarization switching speed, the MIM capacitor structure is also used in high-frequency measurement up to 0.5 MHz to study the time response of ferroelectric switching in HZO, as shown in Figure 2 and in Supporting Information (SI) Section 1. For WSe_2 NC-FETs with IMG, the IMG pattern was then defined by electron-beam lithography, followed by 20 nm Ni electron-beam evaporation and lift-off process. Another 10 nm HfO_2 was deposited by ALD at 250 °C using TDMAHf and H_2O as precursors. WSe_2 flakes were then transferred to the substrate by scotch tape-based mechanical exfoliation from a bulk crystal (Nanosurf, Inc.). Electrical contacts using 30 nm Pt and 50 nm Au electrodes were fabricated using electron-beam lithography, electron-beam evaporation, and lift-off process. A false-color top-view scanning electron microscopy (SEM) image of a representative WSe_2 NC-FET is shown in Figure 1c, capturing the Pt/Au source/drain electrodes and the WSe_2 flakes. Electrical measurement

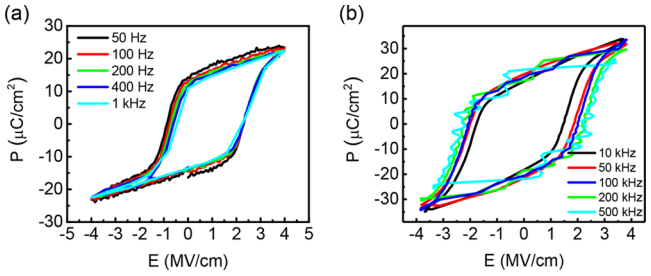

Figure 2. (a) Polarization versus electric field hysteresis loop of a TiN/10 nm HZO/TiN capacitor measured by a Radiant RT66C ferroelectric tester from 50 Hz to 1 kHz. (b) Polarization versus electric field hysteresis loop of the same capacitor measured using RC circuit and arbitrary function generator (square wave).

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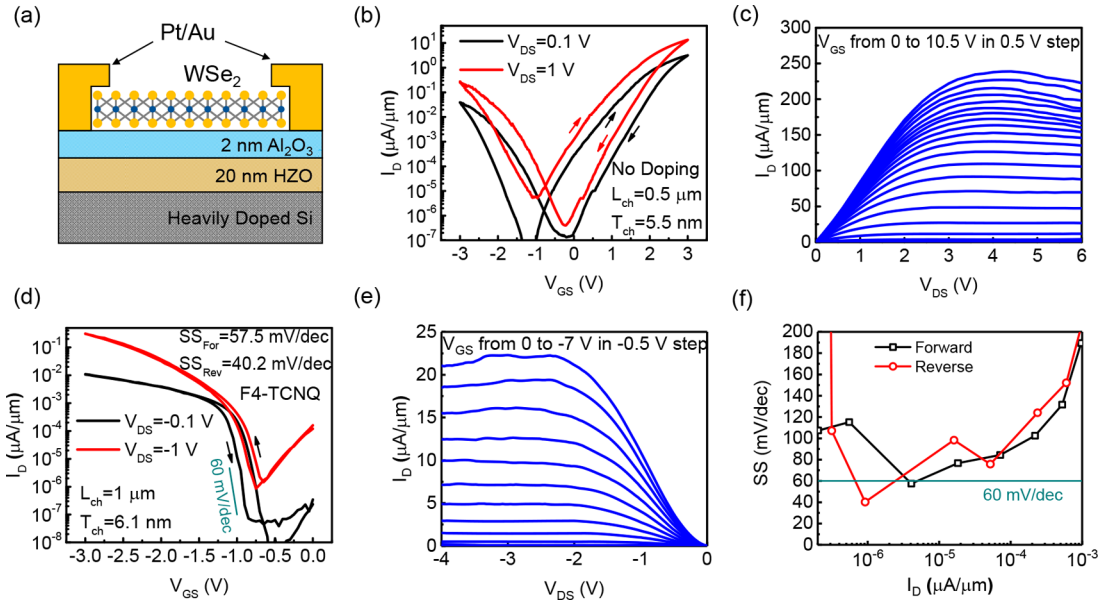

Figure 3. (a) Cross-sectional view of WSe_2 NC-FETs without internal metal gate. (b) I_D-V_{GS} in 20 mV V_{GS} step and (c) I_D-V_{DS} characteristics of a WSe_2 NC-FET before F4-TCNQ doping. This device has a channel length of 0.5 μm and channel thickness of 5.5 nm. A high maximum drain current of 239 μA/μm is achieved. Clear NDR can be observed in I_D-V_{DS} characteristics because of the negative DIBL effect induced by negative capacitance. (d) I_D-V_{GS} in 50 mV V_{GS} step and (e) I_D-V_{DS} characteristics of WSe_2 NC-FETs after F4-TCNQ doping. This device has a channel length of 1 μm and channel thickness of 6.1 nm. The device exhibits SS_{Rev} = 40.2 mV/dec, SS_{For} = 57.5 mV/dec at V_{DS} = −0.1 V. SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps. Clear NDR can be observed in I_D-V_{DS} characteristics because of the negative DIBL effect induced by negative capacitance. (f) SS versus I_D characteristics of p-type WSe_2 NC-FET without IMG and after F4-TCNQ doping, of the same device as in panel d.

was first carried out on the completed WSe_2 NC-FETs. The measured sample was then soaked in an isopropyl alcohol solution of 0.75 mmol/L F4-TCNQ for 12 h followed by N_2 drying for p-type doping of the channel. F4-TCNQ is an organic molecule with a large electron affinity of 5.2 eV. It is widely used as a p-type dopant for graphene, black phosphorus, TMDs and other low dimensional materials.[20,24−26] After doping, the WSe_2 NC-FETs were electrically characterized again under ambient condition. All electrical measurements were carried out at room temperature. The $I-V$ measurement was done using a B1500 system with HRSMU and with HR-ADC in AUTO mode. The time in $I-V$ measurement for each data point can be calculated as time = default integration time × factor, where factor = 20 in this work. Default integration time is related with the current level and can be found from the B1500 manual. Estimated time constants for different current levels are listed as following, 1 pA, 25.6 ms; 10 pA, 25.6 ms; 100 pA, 12.8 ms; 1 nA, 6.4 ms; 10 nA, 6.4 ms; 100 nA, 16 ms; 1 μA, 1.6 ms; 10 μA, 3.2 ms; 100 μA, 1.6 ms.

To study the ferroelectric property of the gate stack, especially the ferroelectric switching at high speed, ferroelectric MIM (TiN/10 nm HZO/TiN) capacitors are used as test structure. The polarization versus electric field ($P-E$) characteristics is measured in two different ways. At low frequency from 50 Hz to 1 kHz, $P-E$ is measured by a Radiant RT66C ferroelectric tester (voltage sweep), as shown in Figure 2a. At high frequency from 10 kHz to 0.5 MHz, $P-E$ is measured (Figure 2b) based on the transient response to square wave voltage signal in RC circuit,[4] which is discussed in detail in SI Section 1. The $P-E$ shows clear ferroelectric switching up to 0.5 MHz. The measurement at high frequency above 0.1 MHz becomes noisier because of the bandwidth of the measurement system. Therefore, the frequency-dependent measurement here confirmed that in ferroelectric HZO, the ferroelectric switching speed can be at least at megahertz level but the upper limit of ferroelectric switching speed has not been detected by current experimental setup.

The electrical performance of WSe_2 NC-FET without IMG is shown in Figure 3. Figure 3a shows the cross-sectional view of a WSe_2 NC-FET without IMG. The I_D-V_{GS} characteristics of a WSe_2 NC-FET before F4-TCNQ doping is shown in Figure 3b. This device has a channel length (L_{ch}) of 0.5 μm and channel thickness (T_{ch}) of 5.5 nm, measured by atomic force microscopy (AFM). The I_D-V_{GS} characteristics were measured in bidirection forwardly (V_{GS} from high to low) and reversely (V_{GS} from low to high) in 20 mV V_{GS} step. SS is extracted for both forward sweep (SS_{For}) and reverse sweep (SS_{Rev}) at low V_{DS}. The device exhibits SS_{For} = 249.9 mV/dec, SS_{Rev} = 176.0 mV/dec for nFET and the device exhibits SS_{For} = 297.4 mV/dec, SS_{Rev} = 225.8 mV/dec for pFET. Figure 3c shows I_D-V_{DS} characteristics of the same WSe_2 NC-FET as shown in Figure 3b. The gate voltage is stressed up to 10.5 V and maximum gate voltage over EOT in this device is about 2.4 V/nm. A high maximum drain current of 239 μA/μm is achieved. The similar on-state performance enhancement on MoS_2 nFETs and black phosphorus pFETs were also observed in our previous works.[11,27] By applying ferroelectric gate stack, on-state performance of 2D FETs is significantly enhanced. SS is far above the thermionic limit at room temperature for two reasons. First, the ambipolar transport, which means electron current overwhelms hole current in the off-state of pFET while hole current overwhelms electron current in the off-state of nFET, prevents the device deeply into off-state from gate control. Second, SS is degraded by the impact of the large Schottky barriers for both electrons and holes.[28] Therefore,

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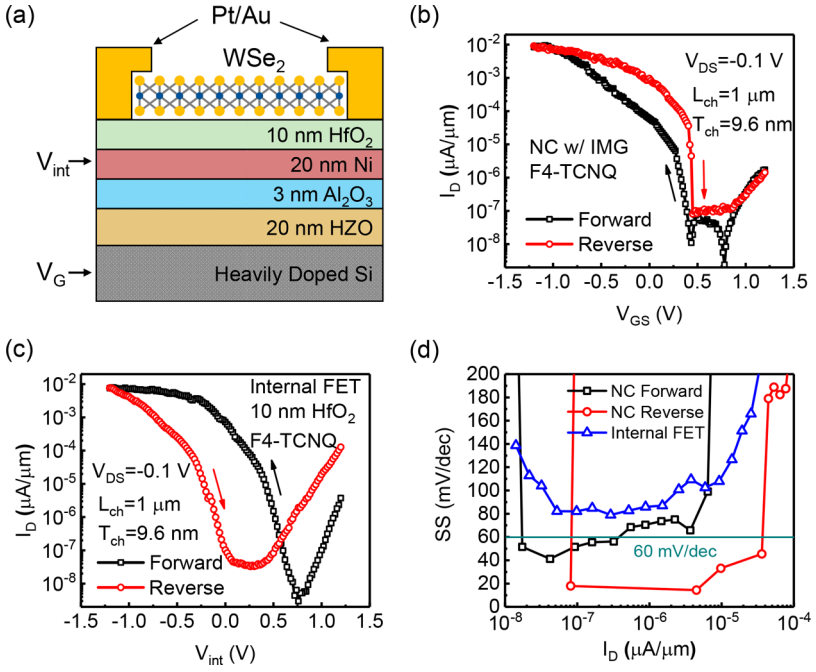

Figure 4. (a) Cross-sectional view of WSe_2 NC-FETs with internal metal gate. (b) I_D-V_{GS} characteristics in 20 mV V_{GS} step of a representative WSe_2 NC-FET with IMG and after F4-TCNQ doping. This device has a channel length of 1 μm and channel thickness of 9.6 nm. The device exhibits SS_{Rev} = 14.4 mV/dec, SS_{For} = 41.2 mV/dec at V_{DS} = −0.1 V. SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps. (c) I_D-V_{GS} characteristics in 20 mV V_{GS} step of the internal WSe_2 FET of the same device as in Figure 4b. The device exhibits SS = 79.1 mV/dec (d) SS versus I_D characteristics of p-type WSe_2 NC-FET with IMG and the internal WSe_2 FET.

suppressing the ambipolar effect and reducing the Schottky barriers are the keys to reduce SS in WSe_2 NC-FETs.

F4-TCNQ was applied to WSe_2 to realize p-type channel doping. With p-type dopant in channel, the electron carrier density inside the WSe_2 channel is significantly reduced and electron branch is suppressed. Meanwhile, the Schottky barrier width for hole transport is reduced, which leads to the reduction of contact resistance and the enhancement of hole branch and on-current for pFETs. Figure 3d shows the I_D-V_{GS} characteristics of a typical WSe_2 p-type NC-FET with F4-TCNQ doping in 50 mV V_{GS} step. This device has a channel length of 1 μm, and channel thickness of 6.1 nm, measured by AFM. The device exhibits SS_{Rev} = 40.2 mV/dec, SS_{For} = 57.5 mV/dec SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps, as shown in Figure 3f. SS of p-type NC-FET below the thermionic limit is the result of the negative capacitance effect. Meanwhile, a low hysteresis (defined as V_{GS} difference at 1 pA/μm in I_D-V_{GS} characteristics) of 0.18 V is also obtained. Figure 3e shows I_D-V_{DS} characteristics of the same WSe_2 NC-FET as shown in Figure 3d. In conventional MOSFETs, the threshold voltage (V_{th}) shifts toward the negative direction as drain voltage. The drain-induced-barrier-lowering (DIBL), defined as DIBL = $-\Delta V_{th}/\Delta V_{DS}$, is usually positive. With ferroelectric gate stack, the DIBL effect could be reversed in NC-FETs.[29,30] The negative DIBL origins from the negative capacitance coupling from drain to the interfacial layer between Al_2O_3 and HZO. NDR can naturally occur as a result of the negative DIBL effect because the positive drain voltage can induce negative charge into the channel. NDR is observed for both WSe_2 n-type NC-FET and p-type NC-FET, as shown in Figure 3c,e, indicating the effectiveness of the negative capacitance effect in ferroelectric HZO.

The electrical performance of WSe_2 NC-FET with IMG and after F4-TCNQ doping is shown in Figure 4. Figure 4a shows the cross-sectional view of a WSe_2 NC-FET with IMG. The IMG here is used to enhance the negative capacitance effect for SS reduction. Figure 4b shows the I_D-V_{GS} characteristics of a WSe_2 p-type NC-FET with IMG and after F4-TCNQ doping (IMG floating) in 20 mV V_{GS} step. This device has a channel length of 1 μm, and channel thickness of 9.6 nm. The device exhibits SS_{Rev} = 14.4 mV/dec, SS_{For} = 41.2 mV/dec, and a negative hysteresis of −0.12 V (at I_D = 1 pA/μm). Figure 4c shows the I_D-V_{GS} characteristics of the internal WSe_2 FET of the same device as in Figure 4b, using IMG as gate electrode in 20 mV V_{GS} step. Figure 4d shows SS versus I_D characteristics in the off-state of I_D-V_{GS} characteristics in Figure 4b,c. SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps, suggesting the existence of internal amplification. The internal amplification, defined as dV_{int}/dV_{GS}, is calculated to be 10/1.8 for reverse/forward gate voltage sweep. Note that the positive hysteresis of the internal WSe_2 FET, as shown in Figure 4c, is induced by trapping and detrapping process in the gate oxide or the oxide/semiconductor interface. This positive hysteresis is much larger compared with WSe_2 NC-FET shown in Figure 3d, suggesting the existence of negative capacitance/ferroelectric effect in the gate stack, which leads to the reduction of positive hysteresis.

In conclusion, WSe_2 NC-FETs with ferroelectric HZO gate stack are demonstrated. Chemical doping of F4-TCNQ is applied to suppress the electron current in the off-state of p-type NC-FETs and to reduce the Schottky barrier width for holes. The doped devices exhibit steep-slope switching characteristics with less than 60 mV/dec for bidirectional sweeps. Sub-60 mV/dec SS (as low as 14.4 mV/dec) and negative DIBL effect conclusively confirm the realization of

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negative capacitance effect in WSe_2 2D-FETs with HZO as gate dielectric.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b00816.

Additional details for transient RC measurement of ferroelectric HZO, statistical and cycling measurement of HZO MIM capacitor, gate stack leakage current, detailed numerical simulation, and modeling of enhancement by IMG (PDF)

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Author Contributions

P.D.Y. conceived the idea and supervised the experiments. M.S. did the device fabrication, DC electrical measurement and analysis. M.S. and W.C. did the P−E measurement. C.J. and M.A.A. conducted numerical simulation. M.S. and Y.D. performed the F4-TCNQ doping. M.S. and P.D.Y. cowrote the manuscript and all authors commented on it.

Notes

The authors declare no competing financial interest.

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