

## MATERIALS SCIENCE

## Heterogeneous integration of ultrawide bandgap semiconductors for radio frequency power devices

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Ultrawide bandgap (UWBG) semiconductors offer high critical electric fields and saturation velocities ideal for radio frequency (rf) devices, but achieving both shallow-level doping and high thermal conductivity ( $k_T$ ) in a single material remains difficult. We demonstrate a scalable, exfoliation-based layer-transfer process to heterogeneously integrate gallium oxide ( $\text{Ga}_2\text{O}_3$ ) thin films with shallow dopants onto high- $k_T$  aluminum nitride (AlN) substrates. This method obviates ion implantation and interfacial dielectric layers used in conventional approaches. A large conduction band offset (3.4 electron volts) at the  $\text{Ga}_2\text{O}_3/\text{AlN}$  interface improves electron confinement in the  $\text{Ga}_2\text{O}_3$  channel. T-gate rf power transistors achieve a maximum oscillation frequency of 90 gigahertz and output power densities of 4.6 watts per millimeter at 2 gigahertz and 4.1 watts per millimeter at 6 gigahertz—among the highest for UWBG devices. A minimal noise figure of 0.48 decibels at 8 gigahertz—among the lowest reported in this frequency range—further highlights the platform's promise for next-generation rf applications.

## INTRODUCTION

Radio frequency (rf) semiconductor devices are used ubiquitously in applications like telecommunication, consumer electronics, aerospace, defense, and health care, with a global market over \$23 billion (<https://fortunebusinessinsights.com/rf-semiconductor-market-110167>). The overarching design target of many rf devices is to concurrently achieve high cutoff frequency ( $f_T$ ) and maximum oscillation frequency ( $f_{\text{max}}$ ), high output power density ( $P_{\text{out}}$ ), high efficiency, low noise, and high linearity. The frequency and power performance of rf devices can be substantially boosted by deploying wide bandgap (WBG) and ultrawide bandgap (UWBG) semiconductors, due to their superior properties including large bandgap, high critical electric field ( $E_C$ ), and high saturation velocity ( $v_{\text{sat}}$ ) (1, 2). The past two decades have witnessed the commercialization of WBG gallium nitride (GaN) rf power devices with a market size over \$740 million (3). On the horizon, UWBG semiconductors such as gallium oxide ( $\text{Ga}_2\text{O}_3$ ), aluminum nitride (AlN), boron nitride, and diamond promise a superior performance limit for rf devices (4). For example, the Johnson figure-of-merit ( $\text{JFOM} = E_C^2 \times v_{\text{sat}}^2 / 4\pi^2$ ), a widely used material indicator for rf device performance, is three times higher in  $\text{Ga}_2\text{O}_3$  compared to GaN (5, 6).

In addition to  $E_C$  and  $v_{\text{sat}}$ , the availability of shallow-level dopant and high thermal conductivity ( $k_T$ ) are also crucial to rf devices. The deep-level dopant can limit the device's breakdown voltage ( $BV$ ) and current density (7), and low  $k_T$  results in high junction temperature, both limiting the device power capacity. In addition, the relatively slow ionization of deep-level dopant could also limit the device switching frequency (8). Unfortunately, shallow dopants and low  $k_T$  are very challenging or even impossible to achieve in a single UWBG material (2). For example,  $\text{Ga}_2\text{O}_3$  is known to offer shallow donors,

large-area wafer, and a decent electron mobility, but it suffers a very low  $k_T$  that is only 1/6 of Si, 1/10 of GaN, and 1/20 of SiC (5). On the other hand, AlN and diamond have a high  $k_T$  but lack shallow-level dopants (2). Such material properties limit the rf device performance. For example, the state-of-the-art  $\text{Ga}_2\text{O}_3$  rf transistors, despite having achieved a  $f_T$  of 10 to 27 GHz and  $f_{\text{max}}$  of 24 to 55 GHz (9–11), exhibit a limited  $P_{\text{out}}$  below 0.715 W/mm (12–14), which is much lower than the GaN counterpart.

A promising solution to the above challenge is combining the complementary properties of distinct UWBG materials through heterogeneous integration. To address the thermal limitation of  $\text{Ga}_2\text{O}_3$ , integration of  $\text{Ga}_2\text{O}_3$  thin films on a variety of substrates including Si (15, 16), SiC (15–19), GaN (20), and diamond (21–24) have been recently demonstrated. These integrations are primarily based on three approaches: (i) mechanical exfoliation and layer transfer (20–22, 24, 25), (ii) hydrogen (H) implantation–based ion cutting (15, 16, 18, 26), and (iii) wafer fusion bonding (17, 23, 27, 28). The  $\text{Ga}_2\text{O}_3$ -on-SiC rf transistors fabricated by ion implantation and bonding process have achieved a high  $P_{\text{out}}$  of 2.3 W/mm at  $f = 4$  GHz (19), about three times higher than the best report on  $\text{Ga}_2\text{O}_3$ -on- $\text{Ga}_2\text{O}_3$ .

However, the performance of  $\text{Ga}_2\text{O}_3$ -on-SiC rf transistors is still far from what the  $\text{Ga}_2\text{O}_3$  material can provide, mainly due to several challenges facing the current heterogeneous integration techniques. First, the flakes produced in mechanical exfoliation usually have a size limited to submicrometers and highly uncontrollable, preventing the fabrication of large-area devices and microwave integrated circuits. Second, the ion cutting technique usually requires H implantation across the active device layer and high-temperature annealing, which can degrade the channel material (29). Third, many bonding techniques require an interfacial amorphous layer, which usually has a poor  $k_T$ . Such a layer has been reported to generate an effective thermal boundary resistance up to 60  $\text{m}^2\text{K}/\text{GW}$  (16, 17), accounting for up to 20% of the device's total thermal resistance ( $R_T$ ). Last, the  $E_C$  of many host substrates (e.g., SiC) or interfacial layer is much lower than the channel material, leading to premature breakdown.

In this work, we develop a distinct heterogeneous integration technique that combines mechanical exfoliation, arrayed transfer,

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and wafer-level direct bonding. The Ga<sub>2</sub>O<sub>3</sub> films are cleaved from the edge of a Ga<sub>2</sub>O<sub>3</sub> substrate, ensuring a good uniformity of film size. These films are then transferred onto a substrate and placed in an array, followed by a wafer-level room-temperature bonding that reduces the thickness nonuniformity of the arrayed films. This method obviates the ion implantation, interfacial oxide, and high-temperature annealing required in many conventional heterogeneous integration approaches. The relatively good uniformity in geometries and thickness effectively upscales the total size of the exfoliated film arrays to the wafer scale, enabling the fabrication of large-area electronics such as interconnected devices and integrated circuits.

In addition, different from the Si and SiC substrates used in prior Ga<sub>2</sub>O<sub>3</sub> integration studies, we select the AlN substrate, which offers a high  $k_T$  of  $\sim 3$  W/(cm·K) and a high  $E_c$  up to 10 MV/cm (30) as well as a favorable band alignment to Ga<sub>2</sub>O<sub>3</sub>. Because of the ultralow electron affinity (0.6 eV) of AlN (30), a 3.4-eV high barrier forms at the Ga<sub>2</sub>O<sub>3</sub>/AlN interface, which is 2.5 eV higher than the Ga<sub>2</sub>O<sub>3</sub>-SiC interface. This barrier can enhance electron confinement in the thin Ga<sub>2</sub>O<sub>3</sub> channel and favors the gate scaling in rf transistors. Leveraging these process and material innovations, the fabricated Ga<sub>2</sub>O<sub>3</sub>-on-AlN rf transistor sets performance records for  $f_{\max}$ ,  $P_{\text{out}}$ , and power-added efficiency (PAE) in UWBG rf devices. The average electric field and noise level is among the best in rf devices reported in all material systems, verifying the high material quality in this hetero-UWBG platform.

## RESULTS AND DISCUSSION

### Heterogeneous integration and material characterization

Figure 1A illustrates the heterogeneous integration process developed in this work. The monoclinic  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is the most thermally stable phase of Ga<sub>2</sub>O<sub>3</sub>, and the single-crystal  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate are available up to 6-inch in the industry (31).  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has a large lattice constant of 12.2 Å along the (100) orientation, allowing the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin film to be easily cleaved and transferred on the blue tape. Distinct from the planar exfoliation widely adopted in prior works, here we exfoliate Ga<sub>2</sub>O<sub>3</sub> thin films from the edge of a 2-inch (-201) n-Ga<sub>2</sub>O<sub>3</sub> substrate grown via the edge-defined film-fed growth (EFG). The substrate has an n-type doping concentration ( $N_D$ ) of  $8 \times 10^{18}$  cm<sup>-3</sup> and a thickness of 500  $\mu$ m. As the width of exfoliated film is determined by the substrate thickness, a consistent geometry around 5000  $\mu$ m by 500  $\mu$ m are produced in the repeated exfoliation. Subsequently, these exfoliated belts are placed in an array with a uniform belt-to-belt spacing, with the total array size scalable to the wafer level.

After the array formation, the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layer needs to be thinned down from tens of micrometers to below 500 nm for rf device fabrication. This is realized by multiple rounds of wafer-scale direct bonding at room temperature, which guarantees uniform bonding force across the wafer; the process details are elaborated in Materials and Methods. After reaching the target film thickness,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin films are transferred from the carrier blue tape to a single-crystal 1-inch AlN substrate by a final bonding with a higher force and longer time. Figure 1B shows the optical microscopic images of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> belt transferred onto the AlN wafer. Figure 1C shows the thickness mapping of the 120  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> belts across the wafer, revealing an average thickness of 428 nm with an SD of 123 nm. Photos of the key steps of this process are presented in fig. S1. Note that the Ga<sub>2</sub>O<sub>3</sub> belt thickness uniformity may be further increased by the chemical-

mechanical-planarization (CMP) process or choosing a thicker Ga<sub>2</sub>O<sub>3</sub> crystal ingot, which can provide a more uniform Ga<sub>2</sub>O<sub>3</sub> belt.

Table S1 of the Supplementary Materials compares this approach with three prior methods for heterogeneous integration—Scotch tape-based exfoliation, ion cutting, and fusion bonding. Here, the implantation-free, interfacial oxide-free approach with wafer-level scalability can potentially offer superior electrical and thermal properties for rf power devices. It can also be widely applicable to other van der Waals materials for heterogeneous integration. To showcase this applicability, we also fabricate Ga<sub>2</sub>O<sub>3</sub> arrayed belts on the Si/SiO<sub>2</sub> substrate and SiC substrate by the same process, which will be used as control samples in electrical and thermal characterizations.

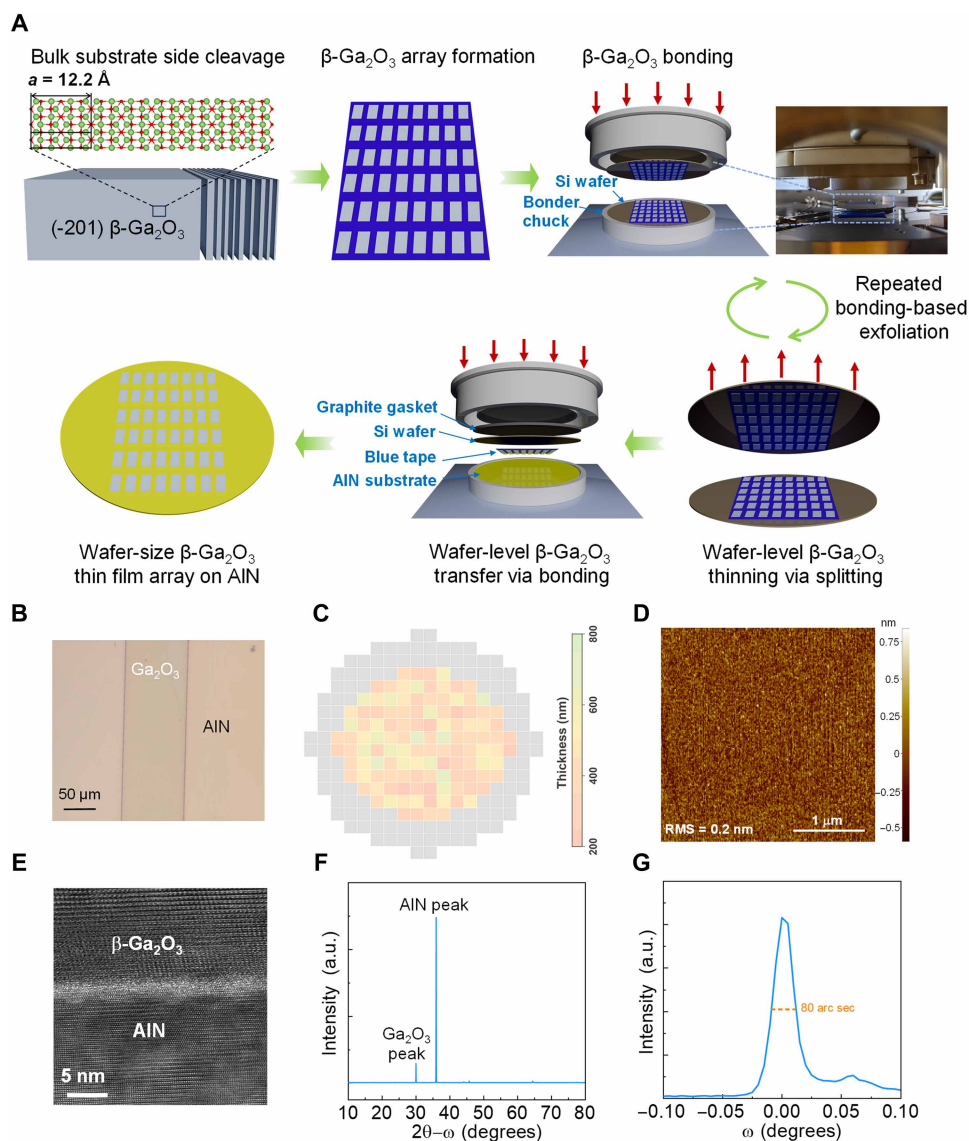
As shown in Fig. 1D, the surface root mean square (RMS) roughness of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface is 0.2 nm. Figure 1E shows the high-resolution transmission electron microscopy (HRTEM) image of the bonded AlN/Ga<sub>2</sub>O<sub>3</sub> interface. The abrupt interface further confirms the absence of an interfacial dielectric layer. The Al, N, Ga, and O elements are confirmed by the energy-dispersive x-ray spectroscopy (EDX) mapping at the interface, as presented in fig. S2. As shown in Fig. 1F, x-ray diffraction (XRD) characterization of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> on AlN only reveals a sharp Ga<sub>2</sub>O<sub>3</sub> peak and AlN peak, suggesting the absence of an interfacial material. Figure 1G shows the high-resolution rocking curve of the bonded  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> on AlN reveals a narrow full width at half maximum (FWHM) of 80 arc sec, verifying the high quality of the transferred  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

### Device fabrication and thermal characterization

A mesa-shaped test device is first used to compare the voltage blocking capabilities of the fabricated Ga<sub>2</sub>O<sub>3</sub>-on-SiC and Ga<sub>2</sub>O<sub>3</sub>-on-AlN wafers (Fig. 2A). The  $BV$  between two electrodes with a spacing of 4  $\mu$ m increases from 475 V in Ga<sub>2</sub>O<sub>3</sub>-on-SiC to 1230 V in Ga<sub>2</sub>O<sub>3</sub>-on-AlN, rendering a three times higher average electric field up to 3 MV/cm. This comparison illustrates the enhanced voltage blocking capabilities of the full-UWBG Ga<sub>2</sub>O<sub>3</sub>-on-AlN platform benefiting from the high  $E_c$  of the AlN substrate.

In addition to a higher breakdown field, the AlN substrate also enables superior electron confinement in the Ga<sub>2</sub>O<sub>3</sub> channel. Figure 2B compares the band alignment diagram of the Ga<sub>2</sub>O<sub>3</sub>/SiC and Ga<sub>2</sub>O<sub>3</sub>/AlN heterojunctions. Benefiting from the low electron affinity of AlN, the Ga<sub>2</sub>O<sub>3</sub>/AlN junction provides a conduction band discontinuity of 3.4 eV, which is 2.5 eV higher than the Ga<sub>2</sub>O<sub>3</sub>/SiC junction. This high-potential back barrier can effectively suppress the channel carrier spill over and enhance the gate control over channel electrostatics. Such an enhanced gate control further allows for downscaling the gate length and increasing the channel doping, which improves  $f_T/f_{\max}$  and on-state current, respectively.

Figure 2C shows the three-dimensional schematic of the T-gate rf transistor fabricated on the Ga<sub>2</sub>O<sub>3</sub>-on-AlN wafer. A high  $N_D$  of  $8 \times 10^{18}$  cm<sup>-3</sup>, which is the  $N_D$  of the n<sup>+</sup>-Ga<sub>2</sub>O<sub>3</sub> substrate in the host wafer, is adopted for the n-Ga<sub>2</sub>O<sub>3</sub> channel. A recessed T-gate reduces the channel thickness below the gate, which suppresses the short-channel effect (SCE), and forms a field plate structure in the gate-to-drain access region, which enhances the device  $BV$ . Top-view and cross-sectional scanning electron microscopy (SEM) images of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf power metal oxide semiconductor field-effect transistor (MOSFET) are displayed as Fig. 2D, with the fabrication process detailed in the Materials and Methods section. Devices with various gate length ( $L_G$ ) and gate-to-drain distance ( $L_{GD}$ ) are fabricated. Devices with a  $L_G/L_{GD}/L_{GS} = 300/700/400$  nm are used for rf

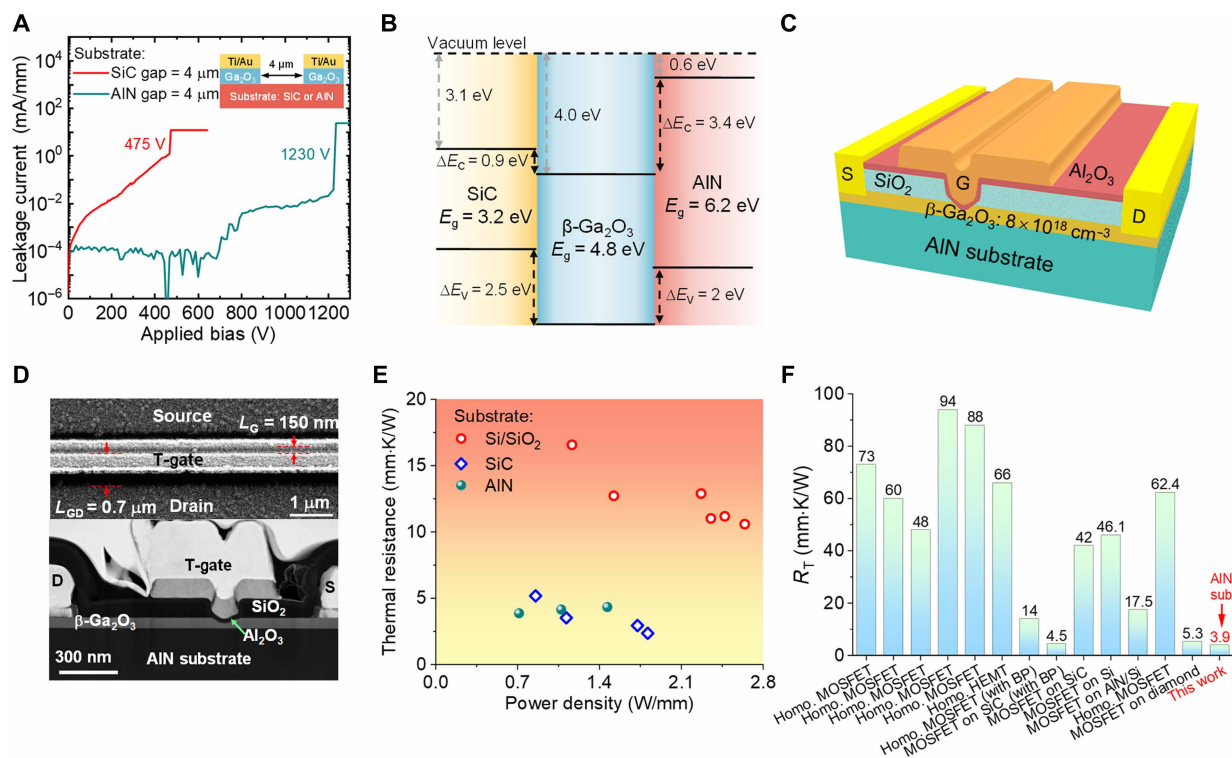


**Fig. 1. Heterogeneous integration process and material characterization.** (A) Illustration of the  $\text{Ga}_2\text{O}_3/\text{AlN}$  heterogeneous integration process. The  $\beta\text{-Ga}_2\text{O}_3$  belt or film with uniform geometry is cleaved from the substrate edge and then manually transferred onto the blue tape to form an array. The thickness of  $\beta\text{-Ga}_2\text{O}_3$  films on blue tape is reduced by multiple wafer-level bonding process until the thickness reaches around 500 nm. The graphite/Si/ $\beta\text{-Ga}_2\text{O}_3$ /AlN stack is formed and loaded into the bonding chamber under a 3-hour bonding process to transfer the wafer-size  $\beta\text{-Ga}_2\text{O}_3$  film array onto the AlN substrate. (B) Top-view optical microscopic image of part of a single  $\beta\text{-Ga}_2\text{O}_3$  film on the AlN substrate. (C) Thickness mapping of 120  $\beta\text{-Ga}_2\text{O}_3$  films in a wafer-size array after being transferred onto the 1-inch AlN substrate. (D) Atomic force microscopy (AFM) image of the surface of  $\beta\text{-Ga}_2\text{O}_3$  film transferred on the AlN substrate, revealing an atomic flat surface with an RMS roughness of 0.2 nm. (E) Zoomed-in and HRTEM image at the atomic interface between the  $\beta\text{-Ga}_2\text{O}_3$  channel and AlN substrate. (F) XRD scan characteristics of  $\beta\text{-Ga}_2\text{O}_3$  on AlN. a.u., arbitrary units. (G) High-resolution rocking curve of transferred and bonded  $\beta\text{-Ga}_2\text{O}_3$  with an FWHM of 80 arc sec.

power, noise, and linearity characterizations, whereas devices with a further scaled  $L_G = 150$  nm and  $L_{GD} = 700$  nm are used for the microwave noise measurements. Additional devices with a long  $L_G$  of 1 and 30  $\mu\text{m}$  are used for thermal resistance ( $R_T$ ) and channel mobility measurements, respectively. From the transfer characteristic of the long-channel device, the electron mobility and density in the recessed  $\text{Ga}_2\text{O}_3$  channel is extracted to be  $\sim 80$   $\text{cm}^2/\text{Vs}$  and  $1 \times 10^{13} \sim 1.9 \times 10^{13}$   $\text{cm}^{-2}$ , respectively, as shown in fig. S3.

The  $R_T$  of the fabricated  $\text{Ga}_2\text{O}_3$ -on-AlN,  $\text{Ga}_2\text{O}_3$ -on-Si/SiO<sub>2</sub> and  $\text{Ga}_2\text{O}_3$ -on-SiC devices are measured by a transient thermal

reflectance method, with the details described in the Materials and Methods section. As shown in Fig. 2E, the  $R_T$  of the  $\text{Ga}_2\text{O}_3$ -on-AlN device is measured to be 3.9  $\text{mm}\cdot\text{K}/\text{W}$  across a wide range of  $P_{\text{out}}$ , which is similar to the  $R_T$  of  $\text{Ga}_2\text{O}_3$ -on-SiC device and over three times lower than that of the  $\text{Ga}_2\text{O}_3$ -on-Si/SiO<sub>2</sub> device. Compared with other homogeneous or heterogeneously integrated  $\text{Ga}_2\text{O}_3$  transistors reported in the literature (17, 26, 32–38), our  $\text{Ga}_2\text{O}_3$ -on-AlN device demonstrates one of the lowest  $R_T$ , as shown in Fig. 2F. This performance is ascribed to the ultrathin  $\text{Ga}_2\text{O}_3$  layer, high- $k_T$  substrate, and the absence of the low- $k_T$  interfacial bonding layer.



**Fig. 2. Electrical and thermal properties of the hetero-UWBG platform and device design.** (A) Leakage current characteristics between two mesa structures fabricated on the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> on the AlN sample and the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> on the SiC sample, revealing a 2.5 times higher breakdown voltage in the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> on the AlN sample. (B) Band alignment of SiC,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, and AlN, where a large conduction band discontinuity of 3.4 eV is presented between  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and AlN. (C) Cross-sectional schematic image of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf power MOSFETs on the AlN substrate. (D) Top-view SEM and cross-sectional TEM images of a T-gate shaped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf power MOSFET with  $L_G = 150$  nm and a gated channel thickness of 30 nm. (E) Extracted thermal resistance ( $R_T$ ) versus dc power density of identical-geometry Ga<sub>2</sub>O<sub>3</sub> MOSFETs fabricated on SiO<sub>2</sub>/Si, SiC, and AlN substrates; the same heterogeneous integration process is applied to three substrates. (F)  $R_T$  benchmark for this work and other reported Ga<sub>2</sub>O<sub>3</sub> transistors on a variety of substrates. Data from refs. (17, 26, 32–38).

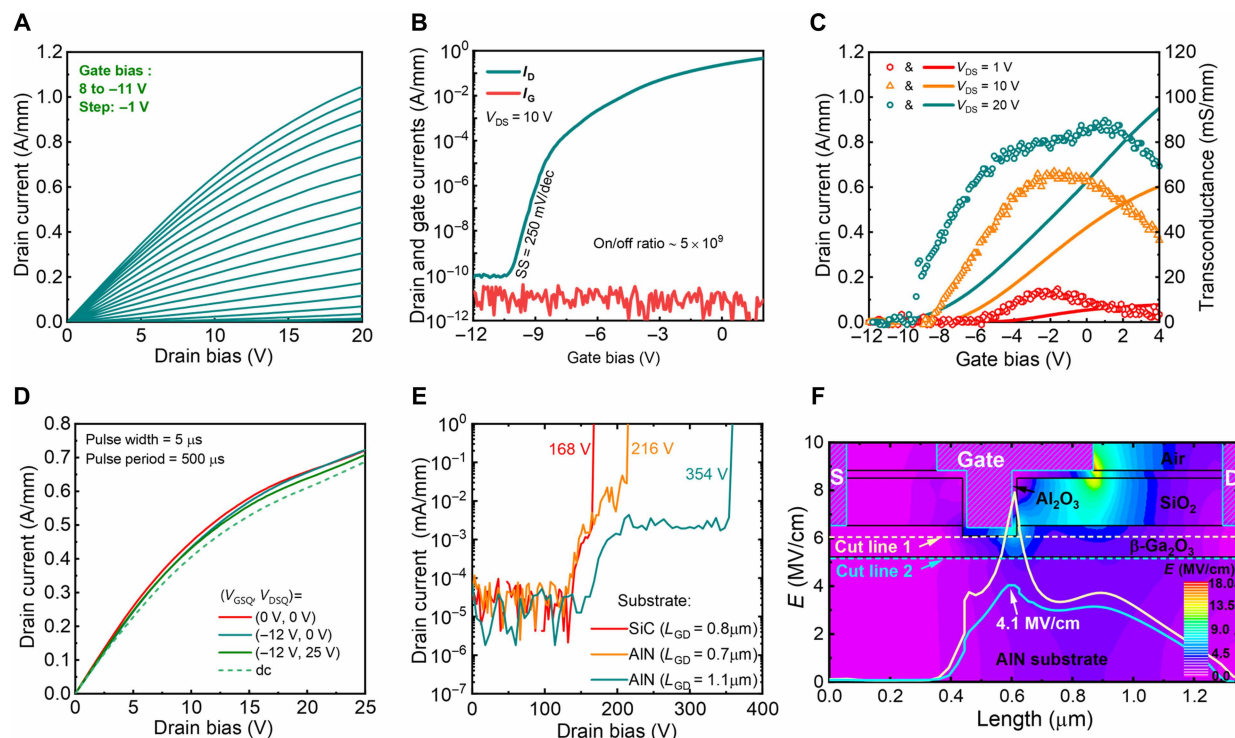
## Device characterization

Figure 3A shows the output characteristics ( $I_D$ - $V_{DS}$ ) of a representative Ga<sub>2</sub>O<sub>3</sub>-on-AlN rf power MOSFET, revealing a maximum  $I_D$  of 1.05 A/mm. Log-scale transfer characteristic ( $I_D$ - $V_{GS}$ - $I_G$ ) at  $V_{DS} = 10$  V is displayed in Fig. 3B, showing a subthreshold slope (SS) of 250 mV/dec and high on/off ratio of  $5 \times 10^9$ . Linear-scale  $I_D$ - $V_{GS}$ - $g_m$  (transconductance) characteristics are shown in Fig. 3C at a  $V_{DS}$  of 1/10/20 V, revealing a maximum  $g_{m,max}$  of 90 mS/mm extracted at  $V_{DS} = 20$  V. Benefited from the excellent gate control and channel electron confinement (fig. S4), the  $g_m$  remains 80% of the peak value across a wide  $V_{GS}$  range of 8.7 V (i.e.,  $V_{GS}$  from  $-5.1$  to 3.6 V), suggesting a high linearity.

Pulse  $I$ - $V$  measurement is widely used to characterize device dynamic characteristics and identify possible degradation induced by carrier trapping. Figure 3D presents the gate-lag and drain-lag pulse  $I_D$ - $V_{DS}$  measurements at three different quiescent bias points ( $V_{GSQ}$ ,  $V_{DSQ}$ ) = (0 V, 0 V), ( $-12$  V, 0 V), and ( $-12$  V, 25 V), which represent the cold channel, gate pulse, and drain pulse scenarios, respectively. These measurements are performed at a pulse period of 5  $\mu$ s, duty cycle of 1%, and  $V_{GS} = 0$  V. Compared with dc characteristics, the pulsed characteristics under three conditions show nearly no dispersion up to a high  $V_{DS} = 25$  V, validating the minimal carrier trapping in the device structure and the suppression of the SHE (standard hydrogen electrode). As a comparison, a nearly identical Ga<sub>2</sub>O<sub>3</sub> device is fabricated on a Ga<sub>2</sub>O<sub>3</sub>-on-SiC wafer that is produced by the

H-implanted ion cutting (15), which is found to suffer from considerable current collapse in pulse  $I$ - $V$  measurement, with the details illustrated in fig. S5. This comparison manifests the advantage of the implantation-free integration process on achieving superior device dynamic characteristics.

Three-terminal off-state breakdown characteristics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf power MOSFETs fabricated on SiC and AlN substrates are shown in Fig. 3E. Ga<sub>2</sub>O<sub>3</sub>-on-AlN devices achieve a  $BV$  of 216 and 354 V for a  $L_{GD} = 0.7$  and 1.1  $\mu$ m, respectively, rendering an averaged breakdown field ( $E_{ave}$ ) of  $\sim 3$  MV/cm. The faster increase in off-state drain current observed between  $V_{DS} = 150$  and 200 V is most likely attributed to field-enhanced leakage mediated by carrier traps within the heavily doped Ga<sub>2</sub>O<sub>3</sub> and at the AlN/Ga<sub>2</sub>O<sub>3</sub> interface. Under a certain high voltage bias, the intense electric field in this region promotes emission from those traps via mechanisms such as Poole-Frenkel conduction, leading to increased leakage before catastrophic breakdown. A similar trap-mediated current hump has also been reported in power devices based on other materials such as gallium nitride (39). Further minimization of these defects includes piranha surface treatments to repair the bonded interface and annealing treatments to heal the heavily doped Ga<sub>2</sub>O<sub>3</sub>. In contrast, Ga<sub>2</sub>O<sub>3</sub>-on-SiC devices only achieve a  $BV = 168$  V at a  $L_{GD} = 0.8$   $\mu$ m, corresponding to an  $E_{ave}$  of 2 MV/cm. The enhanced  $BV$  is further explained by physics-based technology computer-aided design (TCAD) simulations. The simulation models are described in the Materials and



**Fig. 3. dc characteristics of the Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET.** (A) Linear-scale  $I_D$ - $V_{DS}$  of a representative Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET with  $L_G = 300$  nm. (B) Log-scale  $I_D$ - $V_{GS}$ - $I_G$  characteristics at  $V_{DS} = 10$  V and (C) linear-scale  $I_D$ - $V_{GS}$ - $g_m$  characteristics at  $V_{DS} = 1/10/20$  V of the same device. (D) Pulsed  $I_D$ - $V_{DS}$  characteristics of the device under three quasi-static bias conditions with 5- $\mu$ s pulse width, 1% duty cycle, and  $V_{GS} = 0$  V. (E) Three-terminal off-state leakage current and breakdown characteristics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs fabricated on SiC and AlN substrates. (F) Simulated electric field contour within the Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET structure at a device breakdown voltage of 216 V, as well as the electric field profiles along the two cutlines in the Ga<sub>2</sub>O<sub>3</sub> channel and AlN substrate. Although the breakdown occurs in Ga<sub>2</sub>O<sub>3</sub>, a high field of 4.1 MV/cm is present in the AlN substrate; if such a substrate field cannot be withstood by the substrate material, premature breakdown will occur in the substrate.

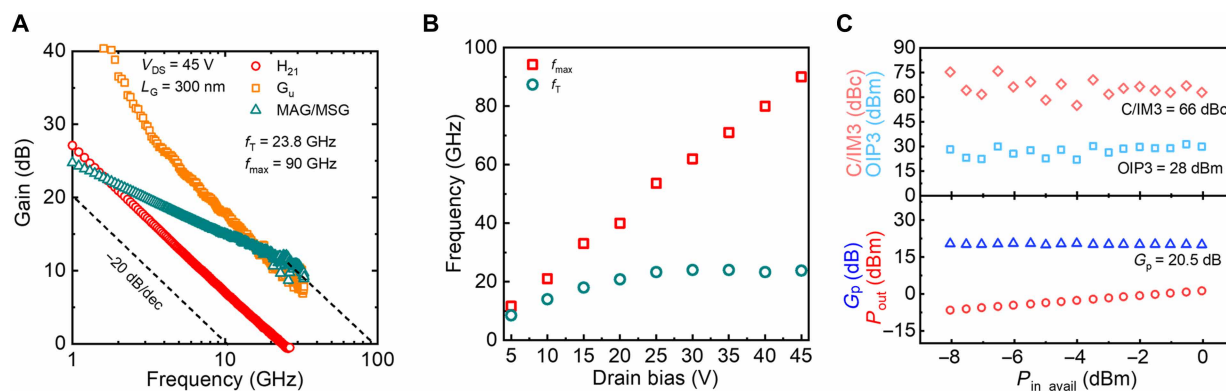
Methods section. The simulated electric field contour and extracted field profile along two cutlines are presented in Fig. 3F and fig. S6 for Ga<sub>2</sub>O<sub>3</sub>-on-AlN and Ga<sub>2</sub>O<sub>3</sub>-on-SiC devices, respectively. The simulation reveals that the  $BV$  of Ga<sub>2</sub>O<sub>3</sub>-on-SiC device is limited by the peak electric field in the SiC substrate. In Ga<sub>2</sub>O<sub>3</sub>-on-AlN devices, the substrate electric field is much lower than the  $E_C$  of AlN, thereby eliminating the premature substrate breakdown and allowing device to exploit the high  $E_C$  of Ga<sub>2</sub>O<sub>3</sub> in the channel region.

Small-signal rf characteristics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf MOSFET with  $L_G = 300$  nm is shown in Fig. 4A, when the device is biased at  $V_{DS} = 45$  V and  $V_{GS} = 0$  V. Standard off-wafer line-reflect-reflect-match (LRRM) calibration and pad-only parasitic on an on-wafer open structure are used to de-embed the as measured S-parameters. The  $f_T$  is determined to be 23.8 GHz, and a  $f_{max}$  of 90 GHz is determined by a conservative  $-20$  dB/dec extrapolation slope from the maximum available gain/maximum stable gain (MAG/MSG). The  $f_T \times V_{DS}$  is determined to be  $\sim 1$  THz-V. The  $f_T/f_{max}$  dependence on the  $V_{DS}$  is displayed in Fig. 4B. The  $f_T$  increases with  $V_{DS}$  and saturates at  $V_{DS} = 25\text{--}30$  V, which is ascribed to the acceleration of electron velocity by electric field and the subsequent saturation. The  $f_{max}$  also increases with  $V_{DS}$  due to the reduced gate to drain capacitance because of the enhanced depletion. This can be understood by the analytical model  $f_{max} = 0.5f_T/(2\pi f_T \times R_g \times C_{gd} + R_g \times g_{ds})^{0.5}$ , where  $C_{gd}$  and  $g_{ds}$  are gates to drain depletion capacitance and output conductance, respectively (40). The enhanced  $f_T/f_{max}$  at high  $V_{DS}$  benefits the amplifiers in achieving a higher gain. The  $f_T/f_{max}$  dependence on

$V_{GS}$  is summarized in fig. S7. Because of the flat  $g_m$ , both  $f_T$  and  $f_{max}$  show weak dependence on  $V_{GS}$ , suggesting a wide gate drive window for high-frequency operation.

The microwave noise performance of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET with  $L_G = 300$  nm is summarized in section S9 of the Supplementary Materials. The minimal noise figure ( $NF_{min}$ ) is extracted to be  $\sim 1.1$  dB at  $f = 8$  GHz. By further scaling the  $L_G$  to 150 nm at a  $V_{DS} = 20$  V, the  $NF_{min}$  is reduced to  $\sim 0.48$  dB at  $f = 8$  GHz, as shown in fig. S8. This  $NF_{min}$  reduction is ascribed to the higher carrier velocity underneath the gate and much lower  $L_G$ , which can be understood by the relation  $NF_{min} \sim f \times (I_D L_G / E_C)^{0.5} \times (v_{sat})^{-1} \times (R_S + R_G)^{0.5}$ , with the relation derivation illustrated in section S10 of the Supplementary Materials, where the  $R_S$  and  $R_G$  are the source and gate resistance, respectively (40). The optimal noise reflection coefficient  $|\Gamma_{opt}|$  and phase angle  $\angle \Gamma_{opt}$  are displayed in fig. S10. The  $|\Gamma_{opt}|$  and  $\angle \Gamma_{opt}$  are measured to be 0.8 and  $24^\circ$  at  $f = 8$  GHz, respectively. The as-measured noise parameters for representative device are shown in fig. S11. The  $NF_{min}$  is found to decrease at increased  $V_{DS}$  due to higher  $g_m$  and electron velocity.

The linearity performance of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf power MOSFET at  $V_{DS} = 15$  V is characterized by two-tone load-pull input power ( $P_{in}$ ) sweeps at  $f = 2$  GHz. Figure 4C shows the measured output third-order intercept point (OIP3) and power gain ( $G_a$ ) versus the  $P_{in}$ . Benefited from the flat  $g_m$  at high  $V_{DS}$ , a high OIP3 of 28 dBm and  $G_a = 20.5$  dB are extracted. This reports the linearity performance in rf power MOSFETs based on either UWBG semiconductors or oxide semiconductors.



**Fig. 4. Small-signal rf characteristics and linearity characteristics of the Ga<sub>2</sub>O<sub>3</sub>-on-AIN MOSFET.** (A) Small-signal gain characteristics of a Ga<sub>2</sub>O<sub>3</sub>-on-AIN MOSFET with  $L_G = 300$  nm when biased at  $V_{DS} = 45$  V and at the  $V_{GS}$  corresponding to the peak  $g_m$  and (B) extracted  $f_T$  and  $f_{max}$  versus  $V_{DS}$ . A  $f_{max} = 90$  GHz is extracted. (C) Two-tone load-pull  $P_{in}$  sweeps at  $f = 2$  GHz to study the linearity of a device at  $V_{DS} = 15$  V. A high linearity with OIP3 = 28 dBm is extracted.

Figure 5A shows the large-signal and class-AB load-pull characteristics of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> rf MOSFET measured at  $f = 2$  GHz and  $V_{DS} = 30$  V. The input and output are matched, and the input signal is under pulse condition with a pulse width of 100  $\mu$ s and duty cycle of 10%. By sweeping the  $P_{in}$  from 12 to 23 dBm, the  $P_{out}$  and PAE first increases and then saturates. Maximum  $P_{out} = 4.6$  W/mm and PAE = 50.5% are achieved. The dependence of  $P_{out}$  and PAE on  $V_{DS}$  is summarized in Fig. 5B, revealing a  $P_{out}$  growing with  $V_{DS}$  with a relatively constant PAE. By further increasing  $V_{DS}$  to 50 V, the measured  $P_{out}$  remains saturated at around 4 W/mm. This  $P_{out}$  saturation is probably attributed to the current collapse under high  $V_{DS}$  bias induced by the traps located at the Ga<sub>2</sub>O<sub>3</sub>/AIN and Ga<sub>2</sub>O<sub>3</sub>/passivation layer interfaces. Further process refinement, such as piranha solution treatment and annealing that have been reported to be effective in interface trap minimization (41), could be explored to improve  $P_{out}$ . Last, the C-band (6 GHz) load-pull measurement result of a device at  $V_{DS} = 45$  V is displayed as Fig. 5C, revealing a  $P_{out} = 4.1$  W/mm. Similar  $P_{out}$  and PAE versus  $V_{DS}$  trends at 6 GHz are identical to that of 2 GHz, as shown in Fig. 5D. These results demonstrate high  $P_{out}$  and PAE performance under a wide range of power and frequency in large-signal operation.

### Performance benchmarking and conclusion

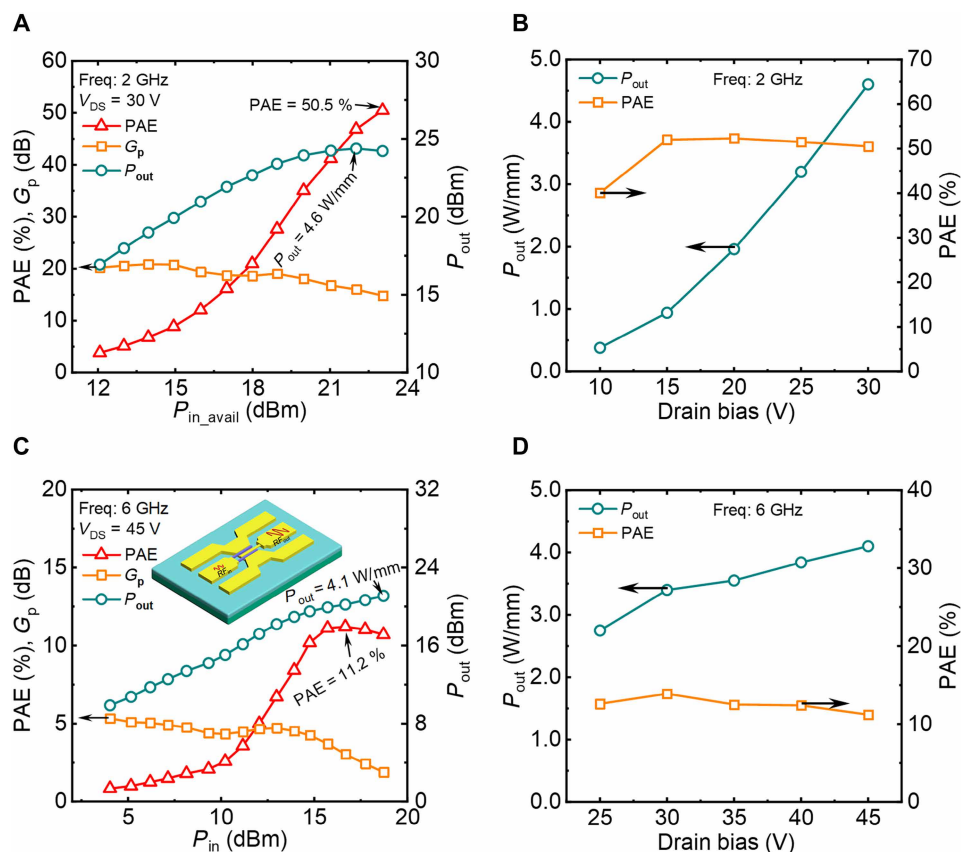
Among the UWBG rf power transistors reported in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (6, 13, 14, 18, 19, 42–45), high Al-composition Al<sub>x</sub>Ga<sub>1-x</sub>N ( $x \geq 50\%$ ) (46), and diamond (47–53), the Ga<sub>2</sub>O<sub>3</sub>-on-AIN transistor fabricated in this work presents the highest  $P_{out}$  and PAE (Fig. 6A). At 2 GHz, the  $P_{out}$  and PAE is six- and threefold higher than the best reports in Ga<sub>2</sub>O<sub>3</sub> transistors on the native substrate (13), respectively, as well as 1.5- and twofold higher than Ga<sub>2</sub>O<sub>3</sub>-on-SiC devices (19, 45). The  $P_{out}$  advantage over Ga<sub>2</sub>O<sub>3</sub>-on-SiC devices (19, 45) expands to 2–4 times at the higher frequency of 4–6 GHz. It should be noted that the  $P_{out}$  performance of Ga<sub>2</sub>O<sub>3</sub> rf transistors still lags behind that of GaN high-electron-mobility transistors (HEMTs) (54–59), primarily due to the still-maturing material and device process technologies considering the early stage of development. Whereas the introduction of heterogeneous integration has enabled substantial advances in the Ga<sub>2</sub>O<sub>3</sub> rf FET,  $P_{out}$  improvement from 0.8 to over 4 W/mm with PAE increased from <20 to 50%. In addition, despite an inferior  $P_{out}$ , the Ga<sub>2</sub>O<sub>3</sub> rf FET has shown a higher average electric field

than that in GaN HEMTs (usually around 1 MV/cm). Moving forward, we believe that the rf performance of hetero-UWBG devices can be further advanced along two pathways: (i) interface engineering to suppress the interfacial dielectric layer formation and reduce interfacial trap density and (ii) device optimizations to downscale gate, reduce ohmic contact resistance, and adopt multidimensional architectures such as FinFETs and multichannel designs (60).

In addition to UWBG semiconductors,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices also belong to another device category—oxide rf transistors, which are widely used in back-end-of-line (BEOL) and small-signal applications (61–66). Here, we benchmark the small-signal performance of our device with representative GaN rf transistors (57, 58, 67–71) and the state-of-the-art oxide rf transistors reported in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (6, 11–14, 18, 19, 42–45, 72, 73), In<sub>2</sub>O<sub>3</sub> (61, 62), ITO (indium tin oxide) (63, 64), IGZO (indium gallium zinc oxide) (65), and IZO (indium zinc oxide) (66) for the trade-off between  $f_{max}$  and  $f_T \times V_{DS}$ , as shown in Fig. 6B. Our Ga<sub>2</sub>O<sub>3</sub>-on-AIN rf transistor has reached a record-high  $f_T \times V_{DS} = 1$  THz·V and  $f_{max} = 90$  GHz, respectively.

Last, to showcase the potential of Ga<sub>2</sub>O<sub>3</sub>-on-AIN rf MOSFET in not only high-power but also low-noise amplifiers, the device is benchmarked with state-of-the-art low-noise X-band transistors reported in GaAs, InP, GaN, and diamond, as shown in fig. S12. The  $NF_{min} = 0.48$  dB is one of the lowest values among these X-band transistors, validating the high quality in materials and interfaces in the heterogeneously integrated Ga<sub>2</sub>O<sub>3</sub>-on-AIN structure.

In summary, this work presents a Ga<sub>2</sub>O<sub>3</sub>-on-AIN heterogeneously integrated platform for rf power devices, which can leverage the complementary electrical and thermal properties of multiple UWBG materials. The integration method combines exfoliated transfer and wafer-scale bonding, obviating the ion implantation and interfacial oxide required in many conventional methods, at the same time enabling a uniform geometry of the arrayed thin films with the total size scalable to the wafer level. The Ga<sub>2</sub>O<sub>3</sub>-on-AIN rf transistor leverages the high potential barrier offered by the AIN/Ga<sub>2</sub>O<sub>3</sub> junction to realize tight gate control and gate length scalability in a highly doped Ga<sub>2</sub>O<sub>3</sub> channel. In addition, the high  $E_C$  of the AIN substrate eliminates the premature substrate breakdown. These synergistic advances in the material, process, and device enable impressive frequency and power performance, including an average electric field over 3 MV/cm, a  $f_T/f_{max}$  of 23.8/90 GHz, a  $P_{out}$  of 4.1 to 4.6 W/mm



**Fig. 5. Large-signal rf characteristics of the Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET.** (A) Large-signal performance of a Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET with  $L_G/L_{GD}/L_G = 400/700/300$  nm and  $W_G = 2 \times 30$   $\mu$ m and the (B) extracted  $P_{out}$  and PAE dependence on  $V_{DS}$ . The device is biased at class-AB condition with a frequency of 2 GHz, pulse width of 100  $\mu$ s, and duty cycle of 10%. A record  $P_{out} = 4.6$  W/mm at 2 GHz and PAE = 50.5% are achieved. (C) Large-signal class-AB performance of a Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET with  $L_G/L_{GD}/L_G = 400/700/300$  nm and  $W_G = 2 \times 15$   $\mu$ m, with a power sweep at  $f = 6$  GHz and  $V_{DS} = 45$  V. Inset: Schematic of a Ga<sub>2</sub>O<sub>3</sub>-on-AlN MOSFET for an amplifier with rf signal amplification (D)  $P_{out}$  and PAE dependence on  $V_{DS}$  from 25 to 45 V at  $f = 6$  GHz. A  $P_{out} = 4.1$  W/mm at 6 GHz is extracted.

at 2 to 6 GHz, and a  $NF_{min}$  of 0.48 dB at 8 GHz, with the  $P_{out}$  being the highest in all UWBG rf devices and the noise among the one of the lowest in all representative X-band rf devices. These results suggest great potential of the heterogeneous UWBG platform for high-frequency, high-power, and low-noise rf electronics.

## MATERIALS AND METHODS

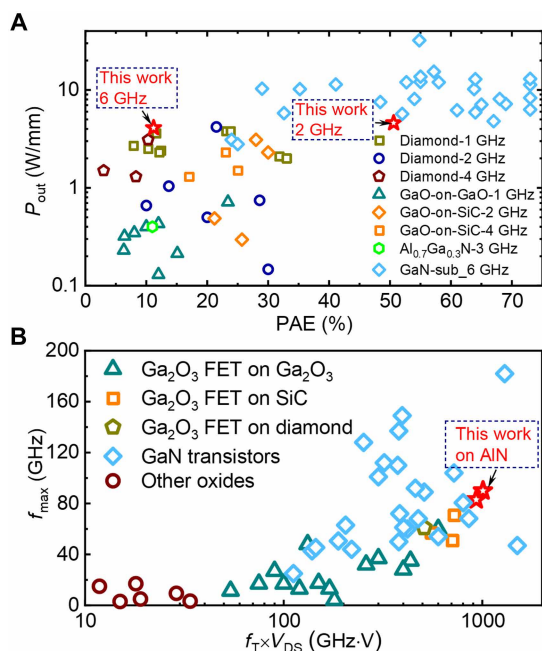
### Heterogeneous integration via exfoliation, layer transfer, and bonding

The (-201)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and Al-face AlN substrates are grown by edge-defined melt-grown and high-temperature high-pressure physical vapor transport (PVT) methods, respectively. The (-201)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (5 mm by 5 mm by 0.5 mm) and AlN (1 inch) substrates are both pretreated by piranha solution followed by buffered oxide etch (BOE) etch and water rinse. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> cleaved edge is manually bonded to the blue tape and forms an array. The initial thickness of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> belts is  $\sim 10$   $\mu$ m. The thickness of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> belts or films on blue tape is reduced by multiple bonding processes as repeated peeling and re-bonding to fresh tape progressively remove sublayers through weak interfacial adhesion at cleavage planes. The ambient condition is high-purity nitrogen environment to avoid

pollution. Thickness reduction per cycle ( $\sim 20$  to 30%) is monitored via cross-sectional SEM. When the thickness is reduced to  $\sim 500$  nm, the blue tape is placed above a Si carrier wafer and graphite gasket with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> side untouched. The AlN substrate is mounted at the top and then placed upside down into the bonding chamber. Room-temperature bonding with duration of 3 hours at a force of 3375 N is implemented by the SUSS MicroTec semiautomatic wafer bonder (SB6-8GEN2). The final thickness of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> films on the AlN substrate is around 400 nm.

### Fabrication of UWBG Ga<sub>2</sub>O<sub>3</sub>-on-AlN rf power MOSFETs

Device full fabrication processes are summarized in fig. S13. After dry etching the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin film, the final Ga<sub>2</sub>O<sub>3</sub> thickness is reduced to  $\sim 60$  nm and another piranha treatment is implemented to smooth the surface and partially repair the surface damage. Mesa isolation is realized by BCl<sub>3</sub>/Ar dry etching. The low-resistance alloyed ohmic contact is formed by evaporating Ti/Au (60/120 nm) followed by rapid thermal annealing at 450°C for 2 min. The contact resistance is measured to be 0.45  $\Omega$ -mm. A 100-nm SiO<sub>2</sub> layer is deposited on the surface by plasma-enhanced chemical vapor deposition (PECVD) at 200°C. The channel recess region is formed by electron-beam lithography (EBL), which is followed by inductively



**Fig. 6. Benchmark of the rf metrics for the Ga<sub>2</sub>O<sub>3</sub>-on-AIN MOSFET against the state-of-the-art rf transistors.** (A)  $P_{out}$  versus PAE of rf transistors reported in various UWBG material platforms, including diamond, Ga<sub>2</sub>O<sub>3</sub>-on-Ga<sub>2</sub>O<sub>3</sub>, Ga<sub>2</sub>O<sub>3</sub>-on-SiC, Al<sub>0.7</sub>Ga<sub>0.3</sub>N, and representative GaN rf transistors, reported at a frequency from 1 to 6 GHz. Data from refs. (6, 13, 14, 18, 19, 42–59). (B)  $f_{max}$  versus  $f_T \times V_{DS}$  of the best data reported in rf transistors based on various oxide materials, including Ga<sub>2</sub>O<sub>3</sub>, In<sub>2</sub>O<sub>3</sub>, ITO, IGZO, and IZO, and representative GaN rf transistors. Data from refs. (6, 11–14, 18, 19, 42–45, 57, 58, 61–73). The device with  $L_G/W_G/L_{GD} = 0.3/2 \times 30/0.7 \mu\text{m}$  has  $f_T = 23.3/23.8$  GHz at  $V_{DS} = 40/45$  V and  $BV = 216$  V.

coupled plasma reactive ion etching (ICP-RIE) of the SiO<sub>2</sub> layer and ~30 nm of β-Ga<sub>2</sub>O<sub>3</sub> to minimize the SCE and improve  $f_{max}$  as well as power gain. Another piranha treatment for 30 s is used to repair the etch damage and smoothen recess channel. The Al<sub>2</sub>O<sub>3</sub> gate dielectric is formed by atomic layer deposition (ALD) with a thickness of 20 nm at a temperature of 300°C. The T-gate is formed by EBL and Ni/Au (50/350 nm) deposition and lift-off process. Source and drain ground-signal-ground pads were formed by etching the SiO<sub>2</sub> layer. Identical Ga<sub>2</sub>O<sub>3</sub> devices are fabricated on SiC and Si/SiO<sub>2</sub> substrates for comparison.

### Device characterizations

The dc  $I$ - $V$  and  $C$ - $V$  characteristics were measured by the Keithley 4200 semiconductor analyzer systems and a Signatone probe station. Thermal resistance characterizations were performed by a transient thermal reflectance equipment with a 532-nm green light-emitting diode light source. The top surface of the gate electrode pad is gold as the thermorefectance coefficient of gold at this wavelength is sufficiently high to enable accurate measurements. The thermorefectance coefficient of gold was determined to be  $\sim 2.0 \times 10^{-4} \text{ K}^{-1}$ , which is consistent with other reports (74, 75). The schematic of a transient thermal reflectance setup was displayed in fig. S14. The S-parameter small-signal measurements were performed with an Agilent PNA-X N5245B network analyzer, and large signal measurements were performed with a Maury load pull system and Cascade probes. Microwave noise characterizations were performed using a Focus

Microwaves noise measurement system. The two-tone linearity performance was evaluated using the Maury Microwave's on-wafer load-pull measurement system, in which the two tones ( $f_1, f_2$ ) were centered on 2 GHz ( $f_0$ ) with a tone spacing of 10 MHz. The linearity, noise, and load-pull characterizations setup were described in figs. S15 to S17.

### Device simulation models and parameters

In the TCAD simulation, the main physical models include the Lombardi model, Fermi-Dirac model, Shockley-Read-Hall model, Chynoweth model, and parallel electric field dependence model. The THERMCONTACT statement is adopted to specify the thermal boundary condition. The β-Ga<sub>2</sub>O<sub>3</sub> impact ionization parameters of the Chynoweth model are based on the values reported in refs. (76, 77). Details of these models are provided in the ATLAS user manual (78). Important simulation models and parameters are summarized in table S2 of the Supplementary Materials. Basic material parameters used in simulation are summarized in table S3 of the Supplementary Materials.

### Supplementary Materials

This PDF file includes:

Supplementary Text

Figs. S1 to S17

Tables S1 to S3

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## Heterogeneous integration of ultrawide bandgap semiconductors for radio frequency power devices

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