The Critical Role of Charge Balance on the Memory Characteristics of Ferroelectric Field-Effect Transistors

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***Abstract*— Ferroelectric field-effect transistors (Fe-FETs) with ferroelectric hafnium oxide (FE HfO_2) as the gate insulator are being extensively explored as a promising device candidate for non-volatile memory application. FE HfO_2 exhibits long retention over ten years, high endurance over 10^{12} cycles, high speed with subnanosecond polarization switching, and high remnant polarization of 10–30 μC/cm^2. However, the performance of Fe-FETs is known to be much worse than FE HfO_2 capacitors, which is not completely understood. In this work, we developed a comprehensive Fe-FET model based on a charge balance framework. The role of charge balance and the impact of leakage-assist-switching mechanism on the memory characteristics of Fe-FETs with Metal/Ferroelectric/Dielectric/Semiconductor (M/FE/DE/S) gate-stack is studied. It is found that the ferroelectric/dielectric (FE/DE) interface and DE layer instead of FE layer is critical to determine the memory characteristics of Fe-FETs, and experimental Fe-FETs can be well explained by this model, where the discrepancy between FE capacitors and Fe-FETs are successfully understood.**

***Index Terms*— Charge balance, ferroelectric field-effect transistor (Fe-FET), ferroelectric hafnium oxide (FE HfO2), ferroelectric/dielectric (FE/DE) stack,**

I. Introduction

FERROELECTRIC field-effect transistors (Fe-FETs) with ferroelectric hafnium oxide (FE HfO_2) [1]–[7] as the gate insulator are being extensively explored as a promising device candidate for nonvolatile memory applications, such as 3-D NAND memory application [8]–[11] because of the one-transistor configuration. The emerging of such tremendous interest in FE HfO_2 based Fe-FETs is because of the discovery of complementary metal-oxide-semiconductor (CMOS) compatible ferroelectricity in Si-doped HfO_2, hafnium zirconium oxide (HZO), and so on. First, the fabrication process of FE HfO_2 is fully CMOS compatible. Its process based on atomic layer deposition (ALD) also enables the capability for 3-D integration such as in the 3-D vertical NAND memory. Second, the thickness of FE HfO_2 can be scaled down to sub-5 nm [12]–[14], so that the operation voltage of FE HfO_2 devices can be as low as few volts, which is much smaller than flash memory devices. The lateral dimension of FE HfO_2 devices can also be scaled to advanced technology nodes due to the ultrathin thickness [5], [6]. Third and more importantly, FE HfO_2 has a large coercive field (E_C) of $\sim$1 MV/cm, which is about one–two orders of magnitude larger than conventional FE materials, such as strontium bismuth tantalite (SBT) or lead zirconium titanate (PZT), leading to a stronger immunity to depolarization effect, so that more than ten-year retention time is achieved on FE HfO_2 based Fe-FETs [3], [15], [16]. Such long retention characteristics have overcome the major obstacle of Fe-FETs based on conventional ferroelectric (FE) materials. In addition, the polarization switching time of FE HfO_2 can be as low as sub-1 ns [3], [17]–[22], which is limited by the lateral domain wall propagation, so that Fe-FETs operate faster in smaller devices, which also contribute the fast operation of ultrascaled and high-density FE HfO_2 Fe-FETs based FE memories.

High-performance FE HfO_2 based metal/FE/metal (M/FE/M) capacitors have been demonstrated with long retention over ten years [3], high endurance over 10^{12} cycles [23], high speed with subnanosecond polarization switching [3], [17]–[22], and remnant polarization (P_R) of 10–30 μC/cm^2 [14]. It is naturally expected that Fe-FET with FE HfO_2 as gate insulator would also have a long retention time, high endurance, and large memory window (MW) due to the long retention, high endurance, and high E_C and P_R from FE HfO_2. However, FE HfO_2 based Fe-FETs usually cannot achieve the high memory performance predicted by the material properties of FE HfO_2. In fact, endurance on the level of only 10^6 [5], [7], [17], or below is commonly observed on Fe-FETs with an FE

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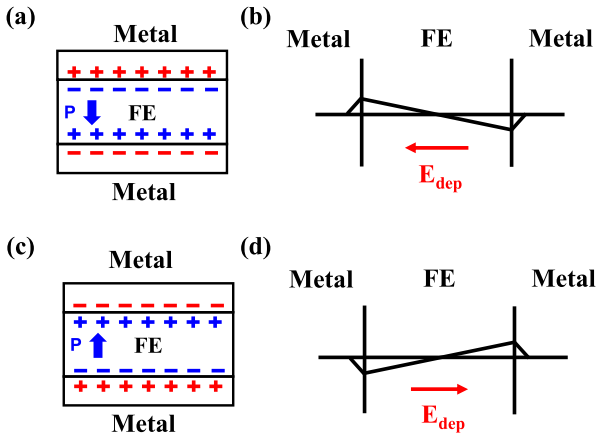

Fig. 1. (a) Charge and (b) potential distribution in M/FE/M capacitor in polarization down state with no external electric field. (c) Charge and (d) potential distribution in M/FE/M capacitor in polarization up state with no external electric field. The depolarization field is induced by the screening length in metal electrodes, which is usually negligible if FE layer is thick.

HfO_2 gate insulator. The MWs of Fe-FETs with an FE HfO_2 gate insulator from literature reports also have very large variations [24], something which is not fully understood. Therefore, the electron transport mechanisms in Fe-FETs and FE capacitors are fundamentally different. Some experimental evidence suggests the dielectric (DE) layer may be related to this phenomenon [25]. How to understand the discrepancy between FE capacitors and Fe-FETs and how to improve the MW and endurance of FE HfO_2 based Fe-FETs are crucial for FE HfO_2-based FE memory applications.

It is well known that FE HfO_2 has a high P_R of about 10–30 μC/cm^2 [14], which is far above the maximum charge density that can be supported by conventional insulators or semiconductors. Such high P_R leads to the accumulation of interfacial charge at FE/DE interface in the gate-stack of a Fe-FET [26]–[29], thereby charge balance can be achieved. All memory characteristics of Fe-FETs, such as MW, retention, endurance, speed, etc., are related to this fundamental polarization switching mechanism [28]. However, in the understanding and modeling of Fe-FETs, the charge accumulation at FE/DE interface is commonly ignored. In this work, we developed a comprehensive Fe-FET model based on this charge balance framework. The impact of charge balance and the leakage-assist-switching mechanism on the memory characteristics of Fe-FETs with Metal/FE/DE/Semiconductor (M/FE/DE/S) gate-stack is studied. It is found that the FE/DE interface and DE layer are critical to determining the memory characteristics of Fe-FETs, and experimental Fe-FETs can be well explained by this model. The new insights in this model can successfully understand the discrepancy between FE capacitors and Fe-FETs.

II. Difference Between FE Capacitors and Fe-FETs

The different electron transport mechanisms in Fe-FETs and FE capacitors are because of the different structures. FE capacitors discussed here have an M/FE/M structure as shown in Fig. 1. Fe-FETs have a transistor structure, where a DE layer, such as SiO_2, is usually necessary to improve the interface quality, as shown in Fig. 2. The gate-stack here is M/FE/DE/S structure. In an M/FE/M structure without an external electric field (E-field), the charge and potential distribution are determined by the FE polarization and the charge distribution on the metal electrode due to the existence of screening length, as shown in Fig. 1. The depolarization field (E_{dep}) is the electric field across the FE layer [30]. In an ideal case, E_{dep} is small due to the highly conductive metal electrode, which is negligible if the FE layer is thick. In an M/FE/DE/S structure without an external electric field, the charge and potential distributions are determined by the FE polarization and voltage drop across the DE layer and band bending of the semiconductor. Voltage drop on metal electrode here is negligible compared to on DE layer and semiconductor. As a result, E_{dep} in a Fe-FET is much larger than E_{dep} in an FE capacitor. Therefore, the FE capacitor has much better retention characteristics than Fe-FETs. FE HfO_2 has a large E_C so that E_{dep}/E_C is relatively small [16] even considering the M/FE/DE/S structure, so that long retention characteristics over ten years can still be achieved on FE HfO_2 based Fe-FETs.

Remnant polarization charge density in FE HfO_2 is about 10–30 μC/cm^2. For M/FE/M structure, such high charge density can be easily compensated by metal electrodes. However, on the M/FE/DE/S, charge balance conditions cannot be satisfied in the ideal case [24], [28]. First, the DE layer cannot support such high charge density without breakdown. For example, the charge density in Al_2O_3 at a breakdown electric field is about 7 μC/cm^2. Second, the maximum carrier density in common semiconductors is on the order of 10^{13}/cm^2, corresponding to a charge density of 1.6 μC/cm^2, which is far below the charge balance condition. In an ideal case without considering FE/DE interfacial charge, and because of the continuity of displacement field (D-field), the displacement field in FE layer (D_{FE}) must be equal to the displacement field in DE layer (D_{DE}), where

$$D_{\text{FE}} = P_{\text{FE}} + \epsilon_{\text{FE}} E_{\text{FE}} \tag{1}$$

$$D_{\text{DE}} = \epsilon_{\text{DE}} E_{\text{DE}}. \tag{2}$$

So that

$$P_{\text{FE}} + \epsilon_{\text{FE}} E_{\text{FE}} = \epsilon_{\text{DE}} E_{\text{DE}}. \tag{3}$$

Here, P_{FE} is the polarization induced by ferroelectricity, $P_{\text{FE}} = P_R$ in full polarization condition. E_{FE} and E_{DE} are the electric fields across the FE layer and DE layer, respectively. Here, it is assumed for simplicity that there are no bulk traps so that D-fields and E-fields are uniform across FE or DE layer; the essential physics does not change if adding the impact of bulk traps. Using SiO_2 as DE layer and $\epsilon_{\text{DE}} = 3.9$, E_{DE} can be estimated as about 30–90 MV/cm, which is far above the breakdown electric field (E_{BD}) of SiO_2. Therefore, to satisfy the charge balance condition, there must be charge injection to the FE/DE interface as interfacial charge (Q_{FEDE}) through a leakage-assist-switching mechanism during the FE polarization switching process in Fe-FET, as shown in

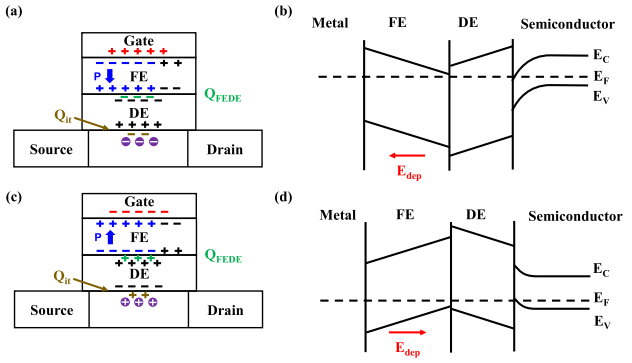

Fig. 2. (a) Charge distribution and (b) band diagram of M/FE/DE/S gate-stack in polarization down state with no external electric field. (c) Charge distribution and (d) band diagram of M/FE/DE/S gate-stack in polarization up state with no external electric field. The depolarization field is induced by the voltage drop across DE layer and band bending of semiconductor. In (a) and (c), black $\pm$ represents the dielectric polarization charge, while blue $\pm$ represents the FE polarization charge.

Fig. 2(a) and (c). Note that Q_{FEDE} contributes to the reduction of E_{dep} as will be discussed in greater detail in Section III, leading to the reduction of the voltage drop across FE, DE, and semiconductor layers as shown in Fig. 2(b) and (d). The continuity equation becomes

$$P_{\text{FE}} + \epsilon_{\text{FE}} E_{\text{FE}} = \epsilon_{\text{DE}} E_{\text{DE}} + Q_{\text{FEDE}}. \tag{4}$$

Thus, E_{DE} below E_{BD} can be achieved.

At DE and semiconductor interface, the continuity equation becomes

$$\epsilon_{\text{DE}} E_{\text{DE}} = Q_{\text{ch}} + Q_{\text{sc}} + Q_{\text{it}} \tag{5}$$

where Q_{ch} is the channel carrier density, Q_{sc} is the charge density in the space charge region, and Q_{it} is the interfacial charge at DE and semiconductor interface. Therefore, to obtain charge balance in Fe-FET in both polarization up and down states, we need both negative charges and positive charges, such as electrons and holes in the channel region for charge balance, which may result in partial polarization switching in the FE layer.

Therefore, the differences between FE capacitor and Fe-FETs are mainly because charge balance in Fe-FETs cannot be achieved without introducing nonideal interfacial charges.

III. Impact of Charge Balance on Fe-FET Operation

In Section II, the necessity of introducing Q_{FEDE} is discussed. In this section, we will further show by a simple derivation that the memory characteristics of Fe-FETs considering FE/DE interfacial charge are fundamentally different from without considering Q_{FEDE}. Memory characteristics such as MW, endurance, retention, etc., are determined by the DE layer instead of the FE layer as commonly understood.

A. Memory Window

The MW of a Fe-FET is defined as the threshold voltage (V_T) difference between polarization up and polarization down states. The threshold voltage of a Fe-FET without considering FE polarization (V_{T0}) [31] is the same as conventional metal-oxide-semiconductor FET (MOSFET), which can be written as

$$V_{T0} = \Phi_{\text{ms}} + 2\Psi_B + \frac{\sqrt{4\epsilon_S q N_A \Psi_B}}{C_{\text{ox}}} \tag{6}$$

where ϕ_{ms} is the work function difference between metal gate and semiconductor, Ψ_B is the Fermi level from intrinsic Fermi level, ϵ_S is the dielectric constant of semiconductor, N_A is doping concentration, C_{ox} is the oxide capacitance, q is the elementary charge. C_{ox} is the capacitance of the FE layer (C_{FE}) and the capacitance of the DE layer (C_{DE}) connected in series. V_{T0} may also depend on the substrate voltage, channel thickness, etc., in a fully depleted device and other device structures, but is only used as a reference V_T and does not affect the derivation on the equations of memory characteristics.

If considering the FE polarization and FE/DE interfacial charge, the threshold voltage of a Fe-FET is

$$V_T = V_{T0} + \frac{P_{\text{FE}} - Q_{\text{FEDE}}}{C_{\text{FE}}}. \tag{7}$$

Here, P_{FE} is the FE polarization and is positive in polarization up state, which may not reach full polarization to P_R. The interfacial charge at FE/DE interface (Q_{FEDE}) always has the same sign as P_{FE} due to a leakage-assist-switching mechanism. The derivation of (7) follows the same procedure as V_T with the impact of oxide fixed charge in [31]. Therefore, assuming a symmetric polarization switching, MW can be expressed as (P_{FE} here is the positive one)

$$\text{MW} = \frac{2(P_{\text{FE}} - Q_{\text{FEDE}})}{C_{\text{FE}}}. \tag{8}$$

In an ideal case without Q_{FEDE}, if $P_{\text{FE}} = P_R$ and Q_{FEDE} is 0, and assuming the thickness of FE layer (t_{FE}) is 10 nm with ϵ_{FE} of 20 and P_R is 20 μC/cm^2, MW of a typical FE HfO_2 based Fe-FET is expected to be 22 V, which is too large to be realistic. Therefore, Q_{FEDE} has to be introduced in the model of Fe-FET, which further confirms the validity of the leakage-assist-switching mechanism.

To properly determine the Q_{FEDE}, according to the continuity equation required by charge balance in (4), Q_{FEDE} can be approximately written as

$$Q_{\text{FEDE}} = -\epsilon_{\text{DE}} E_{\text{eff}} + P_{\text{FE}}. \tag{9}$$

Here, FE polarization is fairly assumed to be much larger than the DE components so that the DE components can be ignored. E_{eff} is the E_{DE} at sufficiently high gate bias when polarization switching is triggered.

According to the leakage assistant switching mechanism [28] in Fig. 3, the polarization switching process in an FE/DE capacitor or Fe-FET can be described as follows. Assuming initial FE polarization is up, to switch down the FE polarization, a high positive voltage is required. At this time, E_{FE} is above the coercive field (E_C), so that the FE polarization switching starts. During this process, the switched polarization reaches a certain high value, so that E_{DE} is high enough that charge injection to FE/DE interface through DE

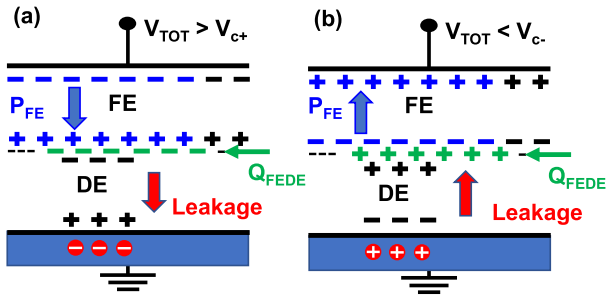

Fig. 3. Leakage-assist-switching in an FE/DE stack in polarization (a) down and (b) up states.

layer starts. This electric field is defined as E_{eff}. To fully switch the FE polarization (assuming P_R of 10 μC/cm^2) in the time scale of 1 μs, the current density of the charge injection is on the order of 10 A/cm^2. Such high current density is close to the breakdown current density of a typical DE material such as SiO_2 or Al_2O_3. Therefore, E_{eff} must be close to the breakdown electric field of the DE layer, such as 10 MV/cm for SiO_2 so that E_{eff} of 5 MV/cm is estimated. E_{eff} may change according to different materials and bulk trap density of the material. And E_{eff} can be regarded as an effective electric field that the DE layer becomes leaky so that charge injection to the FE/DE interface becomes possible. This E_{eff} is related to the strength of the DE layer and the degradation of the DE layer will result in the reduction of E_{eff}.

Therefore, considering (8) and (9), MW can be written as

$$\text{MW} = 2\frac{\epsilon_{\text{DE}} E_{\text{eff}}}{C_{\text{FE}}}. \tag{10}$$

In this case, assuming t_{FE} of 10 nm, ϵ_{DE} of 3.9, ϵ_{FE} of 20, and E_{eff} of 5 MV/cm, MW can be estimated as 2.0 V, which is very close to the experimentally reported values.

The above discussions are based on the fact that P_{FE} is larger than $\epsilon_{\text{DE}} E_{\text{eff}}$ so that a leakage-assist-switching process must exist. However, P_{FE} may not always reach full polarization or high polarization charge density. For example, if the gate voltage is not high enough, only partial polarization switching may be obtained, leading to a small MW. Note that to achieve high P_{FE}, both positive and negative charges are required for charge balance according to (5). In the semiconductor channel, high positive and negative charge density may not exist together, so that full polarization switching may not be achieved, which may also lead to a small MW.

In this case, if P_{FE} is smaller than $\epsilon_{\text{DE}} E_{\text{eff}}$, Q_{FEDE} is 0 and MW becomes

$$\text{MW} = \frac{2P_{\text{FE}}}{C_{\text{FE}}}. \tag{11}$$

Here, according to the above new insights, we want to emphasize that there are two key points to achieve a large MW on a Fe-FET. First, the quality of the DE layer is critical to enhancing the MW. A low-quality interfacial layer may lead to the diminishing of MW because the DE layer cannot hold charge. Second, to have both high positive and negative charge density, for example, high hole and electron density in the semiconductor channel is important for charge balance. Narrow bandgap materials such as Ge [20], [32] and Si may be more suitable for Fe-FETs. AlGaN/GaN heterojunction, where 2-D electron gas formed at its interface, is not suitable for making a Fe-FET because no inversion hole or positive charged layer from heavily doped ions can be formed to support FE polarization switch in AlGaN/GaN heterojunction [24], [33].

B. Endurance

An important indication from the above model is to understand the endurance characteristics of FE HfO_2-based Fe-FETs. FE HfO_2-based M/FE/M capacitors have been demonstrated with high endurance over 10^{12} cycles while endurance on the level of only 10^6 or even below is commonly observed on Fe-FETs with FE HfO_2 gate insulator. This phenomenon can be successfully explained by the above model. According to (10), MW of Fe-FET degrades during the endurance measurement because E_{eff} becomes smaller. The physics of E_{eff} degradation is simply because E_{eff} by definition is the electric field that DE layer becomes leaky so that charge injection into FE/DE interface becomes possible. Thus, E_{eff} must be close to the breakdown electric field of the DE layer. The multiple cycles of operation near breakdown can easily make the DE layer leakier so that E_{eff} becomes smaller. This happens before the FE layer degrades. Therefore, the endurance characteristic of a Fe-FET is determined by the DE layer instead of the FE layer. This is fundamentally different from an M/FE/M capacitor.

Therefore, to improve the endurance characteristics, there are two possible approaches. First is to develop an FE thin film with an FE polarization density of less than a few μC/cm^2, so that the DE layer does not operate near breakdown. For example, $CuInP_2S_6$ has a low P_R of 2–4 μC/cm^2 [34]. The reduction of Hf composition in FE HZO can also reduce the P_R of the FE layer. The P_R is also reduced rapidly once FE HZO thickness is smaller than 4 nm [14]. However, to improve the endurance performance by reducing P_R, the decrease of MW is unavoidable according to (11), which also results in the reduction of E_{dep} and the improvement of retention performance. Therefore, to balance MW, retention and endurance performance has to be considered in the design of Fe-FETs. The second one is to develop Fe-FETs without DE layer. The control of D_{it} becomes critical for this approach because D_{it} may also screen the FE polarization which leads to the reduction of MW and endurance performance. A back-gate Fe-FET with oxide semiconductor channel [35]–[37] is preferred since no native interfacial oxide layer is needed.

C. Retention

The retention characteristics are determined by E_{dep} and charge trapping across the DE layer, which both lead to the drift of V_T and loss of MW. More than ten years of retention time has been successfully demonstrated on FE HfO_2-based Fe-FETs. The high retention performance is also related to the charge accumulation at FE/DE interface.

According to the definition of E_{dep} (i.e., $E_{\text{dep}} t_{\text{FE}} + E_{\text{DE}} t_{\text{DE}} = 0$), (4) and (9), and a M/FE/DE/M structure for

simplicity of discussion, E_{dep} can be written as

$$E_{dep} = \frac{P_{FE} - Q_{FEDE}}{\epsilon_{FE} + \epsilon_{DE}\frac{t_{FE}}{t_{DE}}} \quad (12)$$

$$E_{dep} \cong \frac{E_{eff}}{\frac{\epsilon_{FE}}{\epsilon_{DE}} + \frac{t_{FE}}{t_{DE}}}. \quad (13)$$

As we can see from (12), if assuming t_{FE} of 10 nm, t_{DE} of 1 nm, ϵ_{DE} of 3.9, ϵ_{FE} of 20, and P_R of 20 μC/cm^2, without considering Q_{FEDE}, E_{dep} is about 3.8 MV/cm, which is above E_C of FE HfO_2 ($\sim$1 MV/cm), and it is not stable. If considering Q_{FEDE}, according to (12b), E_{dep} is 0.3 MV/cm, which is below E_C. To increase ϵ_{FE} for higher DE constant and increase the ratio of t_{FE} and t_{DE} can further reduce E_{dep} to improve the retention characteristics.

D. Impact of 2-D and 3-D Electrostatics

The above discussions are based on a 1-D model, but the real Fe-FETs are planar devices with 2-D electrostatic potential distribution or 3-D devices, such as FinFETs or gate-all-around (GAA) FETs, with 3-D electrostatic potential distribution. The impact of 2-D or 3-D electrostatics is crucial to Fe-FET operation in certain device structures.

For example, in silicon Fe-FETs with an n-type channel (p-doped), to switch down the FE polarization, a high positive gate voltage is applied, so that an electron inversion layer is formed. The high-density electron inversion layer terminates the electric field so that the electrostatic potential distribution is similar to the 1-D case like a M/FE/DE/M structure as shown in Fig. 3(a). To switch up the FE polarization, a high negative gate voltage is applied, so that a hole accumulation layer is formed. The electrostatic potential distribution is also similar to the 1-D case as shown in Fig. 3(b). Therefore, if with both sufficient positive charges and negative charges, Fe-FET operation can be well explained by the above 1-D model.

However, if without the existence of both positive and negative charges, such as a GaN Fe-FET [24], [33], [38] with electrons formed at AlGaN/GaN polar semiconductor interface, Fe-FET switching is not possible due to the lack of holes. There is a large voltage drop across the semiconductor, in this case, also resulting in an insufficient electric field across the FE layer. This case was verified by numerical simulation in [24]. Another example is in Fe-FETs with floating body structure [35], [39], [40], there is no well-defined body potential. If without mobile electrons and holes together, the electrostatic potential cannot be approximated as 1-D in the OFF-state, so FE polarization switching near the source/drain region is much easier due to a stronger electric field across the FE layer near the source drain. Thus, for Fe-FETs with floating body structures, the performance of short channel devices is expected to be better than long channel devices. Therefore, device scaling can contribute to improving the memory performance of Fe-FETs.

IV. Conclusion

In summary, we have developed a comprehensive Fe-FET model based on the charge balance framework. The impact of charge balance and the leakage-assist-switching mechanism on the memory characteristics of Fe-FETs with M/FE/DE/S gate-stack is studied and the discrepancy between the memory performance of FE capacitors and Fe-FETs are successfully understood. It is found that the FE/DE interface and DE layer are critical to determining the memory characteristics of Fe-FETs. The MW, retention, and endurance characteristics of FE HfO_2-based Fe-FET are determined by DE layer instead of FE layer as usually understood.

To further improve the memory performance of Fe-FETs, according to the new insights in this model, the following two potential approaches are provided.

1) To reduce the remnant polarization of the FE layer down to below a few μC/cm^2, so that FE operation does not involve a leakage-assist-switching process. For example, FE HZO with a reduced Hf composition or ultrathin FE HZO.
2) To remove the DE layer and use a M/FE/S structure, such as employing a back-gate Fe-FET with an oxide semiconductor channel. But a high-quality FE and semiconductor interface is still needed in this case.

References

[1] H. Ishiwara, "Current status and prospects of FET-type ferroelectric memories," *FED J.*, vol. 11, pp. 27–40, 2000, doi: 10.1109/DRC.1999.806306.

[2] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, no. 10, Sep. 2011, Art. no. 102903, doi: 10.1063/1.3634052.

[3] J. Müller, T. S. Boscke, U. Schroder, R. Hoffmann, T. Mikolajick, and L. Frey, "Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO_2," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 185–187, Jan. 2012, doi: 10.1109/LED.2011.2177435.

[4] J. Müller *et al.*, "Ferroelectricity in simple binary ZrO_2 and HfO_2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, Aug. 2012, doi: 10.1021/nl302049k.

[5] J. Muller *et al.*, "Ferroelectricity in HfO_2 enables nonvolatile data storage in 28 nm HKMG," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2012, pp. 25–26, doi: 10.1109/VLSIT.2012.6242443.

[6] S. Dunkel *et al.*, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond," in *IEDM Tech. Dig.*, Dec. 2017, pp. 485–488.

[7] K. Ni *et al.*, "Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: 10.1109/TED.2018.2829122.

[8] K. Florent *et al.*, "First demonstration of vertically stacked ferroelectric al doped HfO_2 devices for NAND applications," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T158–T159, doi: 10.23919/VLSIT.2017.7998162.

[9] K. Florent *et al.*, "Vertical ferroelectric HfO_2 FET based on 3-D NAND architecture: Towards dense low-power memory," in *IEDM Tech. Dig.*, Dec. 2018, pp. 43–66, doi: 10.1109/IEDM.2018.8614710.

[10] M.-K. Kim, I.-J. Kim, and J.-S. Lee, "CMOS-compatible ferroelectric NAND flash memory for high-density, low-power, and high-speed three-dimensional memory," *Sci. Adv.*, vol. 7, no. 3, Jan. 2021, Art. no. eabe1341, doi: 10.1126/sciadv.abe1341.

[11] H. W. Park, J. Lee, and C. S. Hwang, "Review of ferroelectric field-effect transistors for three-dimensional storage applications," *Nano Sel.*, vol. 2, pp. 1–21, Jan. 2021, doi: 10.1002/nano.202000281.

[12] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwang, "Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature," *Appl. Phys. Lett.*, vol. 102, no. 24, Jun. 2013, Art. no. 242905, doi: 10.1063/1.4811483.

[13] X. Tian, S. Shibayama, T. Nishimura, T. Yajima, S. Migita, and A. Toriumi, "Evolution of ferroelectric HfO_2 in ultrathin region down to 3 nm," *Appl. Phys. Lett.*, vol. 112, Art. no. 102902, Mar. 2018, doi: 10.1063/1.5017094.

[14] X. Lyu, M. Si, X. Sun, M. A. Capano, H. Wang, and P. D. Ye, "Ferroelectric and anti-ferroelectric hafnium zirconium oxide: Scaling limit, switching speed and record high polarization density," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. T44–T45, doi: 10.23919/VLSIT.2019.8776548.

[15] H. Ishiwara, "FeFET and ferroelectric random access memories," *J. Nanosci. Nanotechnol.*, vol. 12, no. 10, pp. 7619–7627, 2012, doi: 10.1093/acprof:oso/9780199584123.003.0012.

[16] N. Gong and T.-P. Ma, "Why is FE–HfO_2 more suitable than PZT or SBT for scaled nonvolatile 1-T memory cell? A retention perspective," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1123–1126, Sep. 2016, doi: 10.1109/LED.2016.2593627.

[17] E. Yurchuk *et al.*, "Impact of scaling on the performance of HfO_2-based ferroelectric field effect transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3699–3706, Nov. 2014, doi: 10.1109/TED.2014.2354833.

[18] K. Karda, C. Mouli, and M. A. Alam, "Switching dynamics and hot atom damage in Landau switches," *IEEE Electron Device Lett.*, vol. 37, no. 6, pp. 801–804, Jun. 2016, doi: 10.1109/LED.2016.2562007.

[19] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Switching dynamics of ferroelectric Zr-doped HfO_2," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1780–1783, Nov. 2018, doi: 10.1109/LED.2018.2872124.

[20] W. Chung, M. Si, P. R. Shrestha, J. P. Campbell, K. P. Cheung, and P. D. Ye, "First direct experimental studies of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric polarization switching down to 100-picosecond in sub-60 mV/dec germanium ferroelectric nanowire FETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 89–90, doi: 10.1109/VLSIT.2018.8510652.

[21] X. Lyu, M. Si, P. R. Shrestha, K. P. Cheung, and P. D. Ye, "First direct measurement of sub-nanosecond polarization switching in ferroelectric hafnium zirconium oxide," in *IEDM Tech. Dig.*, Dec. 2019, pp. 342–345, doi: 10.1109/IEDM19573.2019.8993509.

[22] M. Si *et al.*, "Ultrafast measurements of polarization switching dynamics on ferroelectric and anti-ferroelectric hafnium zirconium oxide," *Appl. Phys. Lett.*, vol. 115, no. 7, Aug. 2019, Art. no. 072107, doi: 10.1063/1.5098786.

[23] Y. C. Chiu, C. H. Cheng, C. Y. Chang, M. H. Lee, H. H. Hsu, and S. S. Yen, "Low power 1T DRAM/NVM versatile memory featuring steep sub-60-mV/decade operation, fast 20-ns speed, and robust 85°C-extrapolated 10^{16} endurance," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2015, pp. T184–T185, doi: 10.1109/VLSIT.2015.7223671.

[24] M. Si, Z. Lin, J. Noh, J. Li, W. Chung, and P. D. Ye, "The impact of channel semiconductor on the memory characteristics of ferroelectric field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 846–849, 2020, doi: 10.1109/JEDS.2020.3012901.

[25] E. Yurchuk *et al.*, "Origin of the endurance degradation in the novel HfO_2-based 1T ferroelectric non-volatile memories," in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2014, pp. 2E.5.1–2E.5.5, doi: 10.1109/IRPS.2014.6860603.

[26] T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?" *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002, doi: 10.1109/LED.2002.1015207.

[27] Y. J. Kim *et al.*, "Interfacial charge-induced polarization switching in Al_2O_3/Pb(Zr,Ti)O_3 bi-layer," *J. Appl. Phys.*, vol. 118, no. 22, Dec. 2015, Art. no. 224105, doi: 10.1063/1.4937544.

[28] M. Si, X. Lyu, and P. D. Ye, "Ferroelectric polarization switching of hafnium zirconium oxide in a ferroelectric/dielectric stack," *ACS Appl. Electron. Mater.*, vol. 1, no. 5, pp. 745–751, May 2019, doi: 10.1021/acsaelm.9b00092.

[29] K. Toprasertpong, M. Takenaka, and S. Takagi, "Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and Hall techniques: Revealing FeFET operation," in *IEDM Tech. Dig.*, Dec. 2019, pp. 570–573.

[30] R. R. Mehta, B. D. Silverman, and J. T. Jacobs, "Depolarization fields in thin ferroelectric films," *J. Appl. Phys.*, vol. 44, no. 8, pp. 3379–3385, 1973, doi: 10.1063/1.1662770.

[31] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.

[32] W. Chung, M. Si, and P. D. Ye, "First demonstration of Ge ferroelectric nanowire FET as synaptic device for online learning in neural network with high number of conductance state and G_{max}/G_{min}," in *IEDM Tech. Dig.*, Dec. 2018, pp. 344–347, doi: 10.1109/IEDM.2018.8614516.

[33] C. H. Wu *et al.*, "High vth enhancement mode GaN power devices with high ID, max using hybrid ferroelectric charge trap gate stack," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T60–T61, doi: 10.23919/VLSIT.2017.7998201.

[34] M. Si, P.-Y. Liao, G. Qiu, Y. Duan, and P. D. Ye, "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure," *ACS Nano*, vol. 12, no. 7, pp. 6700–6705, Jul. 2018, doi: 10.1021/acsnano.8b01810.

[35] M. Si *et al.*, "Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating," *ACS Nano*, vol. 14, no. 9, pp. 11542–11547, Sep. 2020, doi: 10.1021/acsnano.0c03978.

[36] M. Si, A. Charnas, Z. Lin, and P. D. Ye, "Enhancement-mode atomic-layer-deposited In_2O_3 transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1075–1080, Mar. 2021, doi: 10.1109/TED.2021.3053229.

[37] M. Si, Z. Lin, A. Charnas, and P. D. Ye, "Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V," *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 184–187, Feb. 2021, doi: 10.1109/LED.2020.3043430.

[38] C. Wu *et al.*, "$Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric gate HEMTs with large threshold voltage tuning range," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 337–340, Mar. 2020, doi: 10.1109/LED.2020.2965330.

[39] S. Dutta *et al.*, "Monolithic 3D integration of high endurance multi-bit ferroelectric FET for accelerating compute-in-memory," in *IEDM Tech. Dig.*, Dec. 2020, pp. 801–804, doi: 10.1109/IEDM13553.2020.9371974.

[40] A. A. Sharma *et al.*, "High speed memory operation in channel-last, back-gated ferroelectric transistors," in *IEDM Tech. Dig.*, Dec. 2020, pp. 391–394, doi: 10.1109/IEDM13553.2020.9371940.