Impact of Channel Material, Interface Quality, and Polarization on Memory Window of Interfacial Layer-Free FeFET With Oxide Semiconductor

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***Abstract*— This study systematically investigates the modulation of the memory window (MW) in interfacial layer (IL)-free and $Hf_xZr_{1-x}O_2$ (HZO)-based ferroelectric field-effect transistors (FeFETs) with oxide channel by engineering oxide semiconductor materials, annealing processes, and polarization in HZO. Our findings reveal that the MW in such an FeFET is predominantly governed by the positive charge supply capability of the semiconductor layer and the interface properties between the ferroelectric (FE) layer and the semiconductor. Specifically, higher doping concentrations in the channel material and less interface trapping are shown to enhance the MW. In contrast, polarization shows limited effect. These results provide critical insights into the underlying mechanisms of MW optimization in FeFETs with oxide semiconductor channels.**

***Index Terms*— FE field-effect transistor (FeFET), Ferroelectric $Hf_xZr_{1-x}O_2$ (Fe-HZO), metal FE semiconductor (MFS) structure, oxide semiconductor.**

I. Introduction

HZO-BASED ferroelectric field-effect transistors (FeFETs) with oxide semiconductor channel (OS)-FeFET, such as In_2O_3 (InO), ZnO, and indium–gallium–zinc oxide (IGZO), have garnered significant attention in recent years due to their promising potential for achieving superior endurance performance and compatibility with monolithic 3-D integration [1], [2], [3], [4]. Compared with conventional Si-FeFETs, which require an interfacial layer (IL) between Si and FE layer [5], [6], [7], [8], [9], OS-FeFETs may enable IL-free operation owing to the inherent compatibility of oxide–oxide interfaces, thereby eliminating charge trapping-induced endurance degradation from subnanometer ILs [10], [11], [12], [13], [14], [15]. This is promising to solve the problem of interface degradation in endurance cycling and to improve endurance performance which is the key limit for Si-FeFET. Up to date, HZO-based OS-FeFETs with remarkable endurance exceeding 10^9 cycles [16], [17] and feasibility for 3-D integration [18], [19] have been demonstrated. For example, Chen et al. [17] achieved $>10^{10}$ endurance by optimizing the FE/OS interface, scaling IGZO thickness, and designing a dual-composition channel, with a memory window (MW) >1 V on 300-mm wafers. Feng et al. [18] reported the first 3-D vertical FE NOR memory with back-end-of-line (BEOL)-compatible processing, featuring a novel side-fin structure that achieved $>10^6$ ON/OFF ratio and 4-V MW. Lin et al. [19] demonstrated 3-D vertical all-oxide transistors using thick degenerated atomic layer deposition (ALD) InO as both gate electrode and source/drain contacts, achieving $>10^5$ ON/OFF ratio, and robust endurance ($>10^{12}$ cycles) in FeFET configuration with 1.85-V MW. However, these properties were obtained in OS-FeFET structures with an IL or with metal capping during HZO crystallization and removing the metal after that. Satisfying properties have rarely been demonstrated in a real IL-free FeFET due to severely limited MW [20].

These issues have been more or less discussed in literatures about OS-FeFET reported so far. For example, Si et al. [21] have pointed out the necessity of IL for getting enough MW in both the OS-FeFETs and Si-FeFETs by physically modeling of charge balance [22]. Tian et al. [13] improved the stability of MW by introducing nitrogen-incorporated SiON IL and regulating Hf:Zr ratio with near-zero MW

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loss. Mo et al. [2] demonstrated that 3-D nanowire FeFETs achieve the large MW due to electric field concentration via Gauss's law, while reducing channel length, diameter, and IGZO thickness enhances MW by strengthening electrostatic coupling and voltage division effects. Yoo et al. [23] achieved a record-high MW of 17.8 V in IGZO FeFETs by introducing an oxygen-deficient intermediate channel and a gate interlayer, enabling full-loop polarization switching. In some papers, MW modulation has also been achieved through engineering device architectures and inducing antiferroelectric (AFE) layer. Mo et al. [24] simulated a double-gate IL-free IGZO-FeFET with controllable MW by fixing the body potential using the top gate. Wang et al. [25] achieved precise tuning of MW from clockwise hysteresis to over beyond twice the coercive voltage in FeFETs with an internal floating gate through controlled scaling of area ratio. Our previous work demonstrated that IL-free FeFETs with IGZO fail to achieve MW due to insufficient positive charge compensation and this issue could be solved by replacing FE-HZO with AFE-HZO [20]. Therefore, key issues arise as follows: 1) what are the intrinsic physics determining the MW in OS-FeFET and 2) how the MW in an OS-FeFET could have been engineered.

Despite the many experimental modulation of MW in FeFET by incorporating IL or engineering structure, a comprehensive understanding of above key issue remains unclear: how do various factors including channel material, quality of interface between the FE layer and channel, and polarization in FE layer intrinsically affect the MW of OS-FeFET? This issue is particularly pronounced in OS-FeFET characterized by an inherent scarcity of holes in the channel, which critically disrupts charge compensation for polarization switching in FE layer. To study this issue, using the real IL-free OS-FeFET structures simply, this work presents a comprehensive experimental and theoretical investigation into MW modulation by different channel materials (InO, ZnO, IGZO), annealing processes and passivation layer on channel. Our findings provide new insights into the interplay between the positive charge supply capability of the channel, charge trapping/detrapping at the interface between the FE layer and channel, and the remanent polarization (P_r) of HZO, revealing mechanisms that dictate MW behavior. This study advances the understanding of MW control in HZO-based FeFETs and offers guidance for optimizing device performance in future memory applications.

II. Experiment

Fig. 1. illustrates the fabrication process and structural configuration of FE capacitors and OS-FeFETs. The process begins with the deposition of a 30-nm tungsten (W) layer via magnetron sputtering on a SiO_2/Si substrate, serving as the bottom/gate electrode. Subsequently, a 10-nm $Hf_{0.5}Zr_{0.5}O_2$ thin film is grown by thermal ALD at 250 °C, using tetrakis (dimethylamido) hafnium (TDMA-Hf) and tetrakis (dimethylamido) zirconium (TDMA-Zr) as metal precursors and deionized water (DIW) as the oxygen source. The semiconductor layer, either 15-nm ZnO or 5-nm InO, is deposited on the HZO layer via thermal ALD at 175 °C and 225 °C with

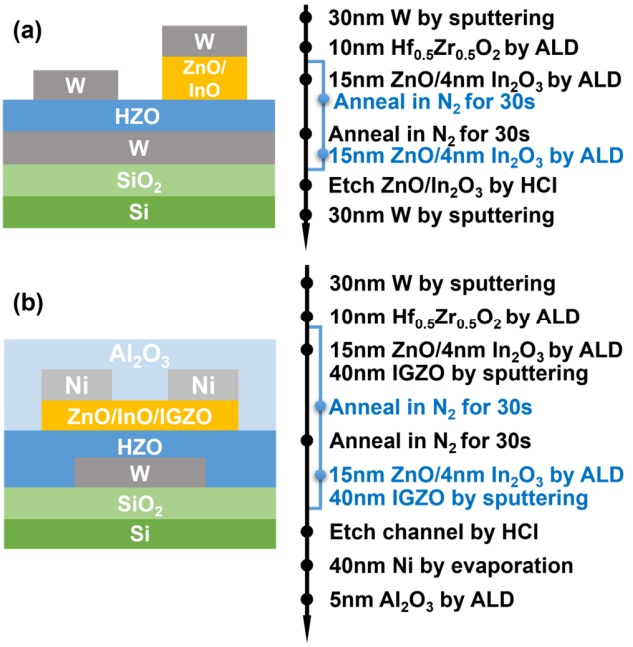

Fig. 1. Structure and process flow of (a) FE capacitors and (b) FeFET devices in the present work. Two kinds of semiconductor materials and two kinds of annealing processes were used.

diethylzinc (DEZn) and trimethylindium (TMIn) as metal precursors. While 40-nm IGZO layer is deposited by magnetron sputtering. Rapid thermal annealing (RTA) is performed either after HZO layer deposition (postdeposition annealing, PDA) or after OS layer deposition (postchannel annealing, PCA) at 450 °C∼550 °C for 30 s in a nitrogen (N_2) atmosphere. For FE-capacitor fabrication, the OS layers are selectively etched by dilute hydrochloric acid, followed by the deposition of a 30-nm W top electrode by magnetron sputtering. Notably, the etching rate of OS by HCl is much quicker than that of HZO because HZO was crystallized, and a selective etching could be obtained. For FeFET devices, source and drain electrodes are formed by thermal evaporation of 40-nm nickel (Ni). In addition, a subset of the transistors incorporate a 5-nm Al_2O_3 passivation layer on the OS layer, which was deposited by thermal ALD at 100 °C using trimethylaluminum (TMA) as the aluminum precursor.

To investigate crystal phase of HZO films and enhance signal legibility, the X-ray diffraction (XRD) was used with grazing-incidence mode (GIXRD) [26]. The polarization–voltage (P–V) hysteresis loops of capacitors were characterized under a bipolar voltage sweep of ±3 V with a frequency of 10 kHz. And the transfer characteristic curves of FeFETs were measured with a source–drain voltage (V_{DS}) of 0.1 V and a gate voltage (V_{GS}) of ±3 V, sweeping in 50-mV steps by the semiconductor parameter analyzer (Keithley 4200).

III. Experimental Results

A. Effect of Semiconductor and Annealing Process on P_r

The effects of the OS material and annealing process on P_r of FE-HZO layer were first considered. Fig. 2 shows the P–V and GIXRD characteristics of HZO/OS capacitors in

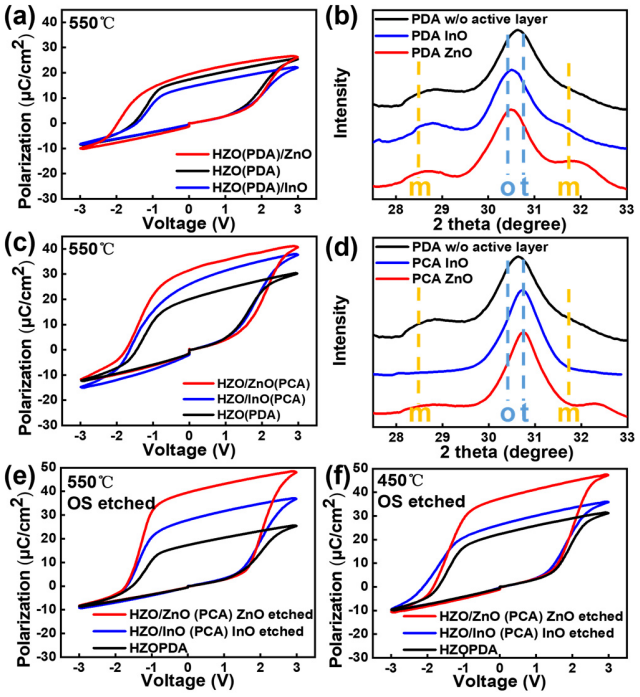

Fig. 2. *P*–*V* loops and GIXRD results of HZO/InO and HZO/ZnO capacitors. (a) and (b) PDA and (c) and (d) PCA respectively. *P*–*V* loops under PCA temperature of (e) 550 °C and (f) 450 °C with channel materials removed before sputtering of top electrode.

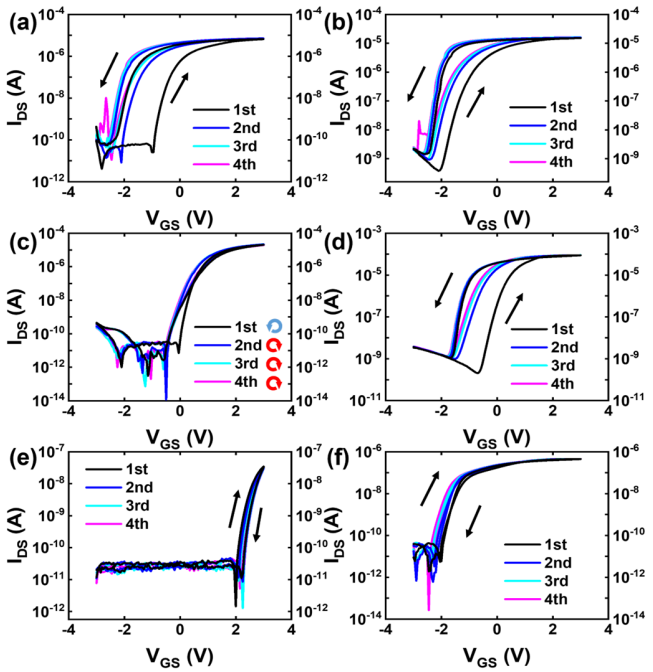

Fig. 3. I_{DS}–V_{GS} characteristics of FeFET for (a) InO with PDA, (b) InO with PCA, (c) ZnO with PDA, (d) ZnO with PCA, (e) IGZO with PDA, and (f) IGZO with PCA before passivation. Notably, the hysteresis loop in (c) exhibits a reversed directionality, as explicitly indicated in the legend.

both PDA and PCA cases. The results of samples without OS layer were also compared. In case of PDA, the *P*–*V* characteristics and crystalline structures of HZO/InO and HZO/ZnO samples are similar [Fig. 2(a) and (b)]. They are also similar to those of HZO sample without OS layer. This is understandable as the polarization is not affected by the process after PDA obviously. The slight difference in P_r may arise from the difference in voltage dropped on OS layer. In contrast, the *P*–*V* results of HZO/InO and HZO/ZnO capacitors with PCA demonstrate obvious difference [Fig. 2(c)]. P_r of HZO/ZnO capacitors is larger than that of HZO/InO ones and both are larger than that of HZO capacitors with PDA. Meanwhile, GIXRD results show that the formation of the monoclinic-phase decrease is suppressed in HZO with PCA [Fig. 2(d)]. Note that the OS layer divides a part of voltage applied on HZO/OS capacitor, so that the voltage drop on HZO is not fair for comparing P_r value between HZO/InO and HZO/ZnO samples. To eliminate this effect, an additional set of capacitors were prepared by completely removing the OS layer via hydrochloric acid etching after the PCA process, followed by deposition of top electrodes. Interestingly, the HZO film with ZnO capping in PCA exhibited an obviously higher P_r than the film with InO capping [Fig. 2(e) and (f)]. And such a difference is larger with higher PCA temperature. This difference is considered to be likely attributed to different strain values induced by different OS layers during annealing [20], [27].

B. Effect of OS Channel and Annealing Process on MW

Next, the MW characteristics of OS-FeFETs fabricated with different annealing processes and OS materials are systematically investigated. The I_{DS}–V_{GS} characteristics of samples with three kinds of OS material and with both PDA and PCA are illustrated in Fig. 3. All the FeFETs with InO- and ZnO-channel demonstrate pronounced counterclockwise hysteresis during the first cycle of voltage sweeping. However, the MW is reduced in subsequent cycles rapidly. Interestingly, an obvious MW is always maintained in InO-FeFET with both PDA and PCA process as well as in ZnO-FeFET with PCA, while it disappears in ZnO-FeFET with PDA where the hysteresis loop transitions from counterclockwise to clockwise after the first sweep cycle. Furthermore, IGZO-FeFETs exhibit no detectable counterclockwise hysteresis observed throughout multiple measurement cycles.

It has been proposed that the large MW in the first cycle may result from polarization changing in the initial defect/domain reconfiguration [28], [29], [30]. Therefore, the stabilized MW values after the first cycle should be considered for more accurate comparison and analysis quantitatively. Fig. 4 summarizes the MWs extracted at a drain current of 1×10^{-6} A in the first to forth sweeping cycles for three kinds of OS-FeFETs with PDA and PCA. Interestingly, the annealing process shows a critical effect on MW. OS-FeFETs with the PCA process exhibit a larger MW compared with those with PDA in both InO and ZnO cases. Since both ZnO- and IGZO-FeFETs with PDA show clockwise hysteresis in the I_{DS}–V_{GS} characteristics which is probably due to interface charge trapping [31], we consider that the PCA process improves the interface quality between the FE layer and OS channel by suppressing interface traps. In addition, under the same annealing process, InO FeFETs demonstrate a larger MW compared with ZnO devices, despite the fact that P_r in

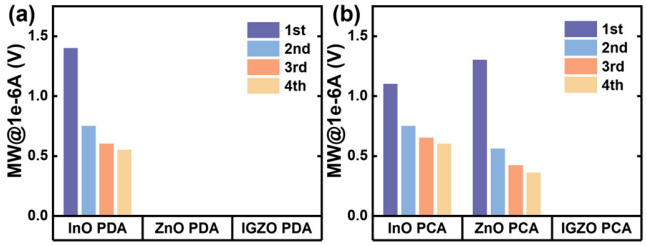

Fig. 4. MW of FeFET for (a) PDA and (b) PCA annealing process in the first four I_{DS}–V_{GS} tests before passivation.

HZO/ZnO capacitor with PCA is significantly higher than that in InO one. These results clearly demonstrate that both OS material and annealing process are significant for controlling MW in FeFET rather than P_r value in HZO layer.

C. Effect of Passivation Layer on MW

In addition, the effect of a 5-nm Al_2O_3 passivation layer, which is deposited on the channel layers at 100 °C, on the I_{DS}–V_{GS} characteristics of these OS-FeFETs was also investigated. The relatively low deposition temperature here is to prevent the secondary annealing of the device during passivation, which may induce a drastic change in the oxygen vacancy concentration of the channel. Such a passivation layer has been generally used for protecting the device from ambient exposure [32], [33], [34], minimizing threshold voltage (V_{th}) drift to ensure stable MW. Fig. 5 shows the I_{DS}–V_{GS} curves of the above OS-FeFETs with passivation layer. Compared with aforementioned samples, it is observed that there is no obvious change in MW after deposition of Al_2O_3. The MWs extracted in the first to forth sweeping cycles are also summarized in Fig. 6. The impact of OS material and annealing process on MW keeps the same with that of devices without passivation. While all the absolute values of MW decreased slightly. This is maybe due to an effect of passivation layer on the positive charge supplying, as the channel layer is relatively thin. It is noteworthy that the IGZO PDA sample exhibits a normally OFF behavior in Figs. 3(e) and 5(e), whereas the IGZO PCA sample shows a negative threshold voltage as shown in Figs. 3(f) and 5(f). This phenomenon may be attributed to interfacial negative charges introduced during the sputtering process, which are subsequently eliminated by PCA through thermal remediation.

IV. Discussion

Finally, the issues why and how MW is controlled by OS material and interface quality rather than P_r in FE layer are discussed. Theoretically, in an ideal FeFET with no defects at interface and/or in dielectric and with sufficient compensation charge in channel for full polarization switching, the MW is obtained [20], [22]

$$\mathrm{MW} = 2P_r/C_{FE} \tag{1}$$

where P_r is the residual polarization and C_{FE} is the capacitance of FE layer of unit area. In this case, MW is mainly controlled by P_r with full polarization switching. In actual case, however,

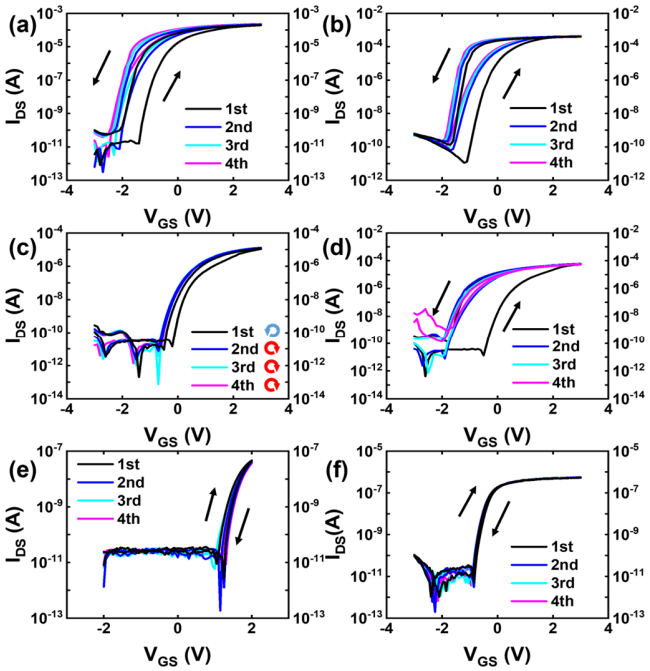

Fig. 5. I_{DS}–V_{GS} characteristics of FeFET for (a) InO with PDA, (b) InO with PCA, (c) ZnO with PDA, (d) ZnO with PCA, (e) IGZO with PDA, and (f) IGZO with PCA after passivation. Notably, the hysteresis loop in (c) exhibits a reversed directionality, as explicitly indicated in the legend.

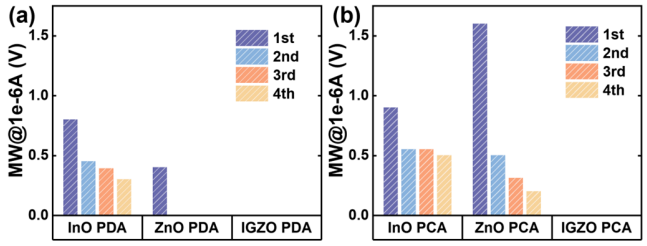

Fig. 6. MW of FeFET for (a) PDA and (b) PCA annealing process in the first four I_{DS}–V_{GS} tests after passivation.

polarization switching needs both positive and negative compensation charges from channel or interface between the FE and channel layer. Thin OS film, however, can supply enough negative charge by free electrons but cannot do sufficient positive charges due to lack of free holes. Supplying of the positive space charges, generally originated from positively charged oxygen vacancies (V_O^{2+}) as schematically shown in Fig. 7, needs a large potential drop on OS layer which involves negative feedback [35], [36]. Moreover, high quality of interface could also not supply enough positive charges. As a result, only limited domains determined by the total amount of positive charges from channel and interface can be switched, contributing to MW. Meanwhile, the charge trapping/detrapping at the defects in HZO, channel, or at the interface will induce a clockwise hysteresis. In some cases, mobile-ionic effect also results in counterclockwise hysteresis, affecting the actual MW estimation in experiments as reported [37], [38].

Here, for simplicity, we ignore the ionic effect and assume all the charge trapping/detrapping effects which induce

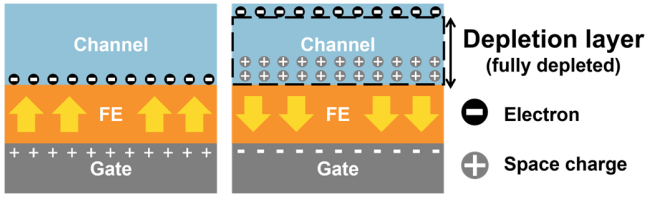

Fig. 7. Schematics of charge compensation in FeFET with oxide semiconductor. Sufficient free electrons can be supplied but positive charges are limited.

clockwise hysteresis as an effective effect at the interface. Then the actual MW′ becomes

$$\mathrm{MW}' = (\Delta P_{\mathrm{FE}} - 2Q')/C_{\mathrm{FE}} \tag{2}$$

where ΔP_{FE} is actually switched polarization in HZO, Q' represents the effective trapping/detrapping charge at the interface, and factor 2 originates from the dual-sweep in transfer characteristic measurement. Since ΔP_{FE} is determined by the positive compensation charges from interface (Q^*) and from space charges in channel (Q_{S}), it can be described as

$$Q^* + Q_{\mathrm{S}} = Q^* + qN_{\mathrm{D}}W_{\mathrm{D}} = \Delta P_{\mathrm{FE}}/2 + \epsilon_0\epsilon_{\mathrm{FE}}E_{\mathrm{FE}} \tag{3}$$

where N_{D} is the doping concentration of the semiconductor material, W_{D} is the depletion width, and E_{FE} is the electric field across the FE layer. Note that Q^* here may be overlapped with Q' partly but they should be different in total.

Combining (2) and (3), it is understandable that OS material with larger doping concentration and thickness can provide more space charges, hence resulting in a larger MW. It is known that the electron concentration in InO ($\sim 10^{20}$) [39], [40] is much larger than that in ZnO ($\sim 10^{18}$) [41], [42], [43] and that in IGZO ($\sim 10^{17}$) is smallest [44], [45] among three kinds of OS materials. The screening length decreases with increasing doping concentration, resulting in stronger electric fields across the FE film which enable more complete polarization switching [46], [47]. So, the largest MW is obtained in InO-FeFETs though the InO layer is thinnest. And no MW is done in IGZO-FeFETs due to much fewer space charges. Meanwhile, annealing process such as PCA is benefit to suppress interface traps and hence the clockwise hysteresis can be reduced. Therefore, the MW of devices with PCA is larger than that with PDA. It is worth noting that the MW will be enhanced if more positive charges can be supplied from IL tunneling [48], [49] or from metal introducing and removing at the interface between the FE and channel layer as reported [20]. And P_{r} in the FE layer will show an effect if sufficient positive charges can be supplied for full polarization switching.

V. Conclusion

In this study, we have systematically investigated the dominant factors influencing the MW in IL-free OS-FeFETs. Our experimental and theoretical analyses reveal that the MW is primarily governed by the positive charge supply capability of the OS layer and the interface properties between the FE layer and the semiconductor rather than P_{r} of the HZO layer. Higher doping concentrations of channel material could supply more positive space charges and hence enhance the MW. Meanwhile, although PCA process could both improve P_{r} in FE layer and suppress the interface charge trapping/detrapping, its benefit to MW lies in the later effect. These findings provide valuable insights for the design and optimization of HZO-based OS-FeFETs, emphasizing the need to engineer the positive charge supply at the interface and within the channel to achieve enhanced memory performance.

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