First Experimental Demonstration of Robust HZO/β-Ga_2O_3 Ferroelectric Field-Effect Transistors as Synaptic Devices for Artificial Intelligence Applications in a High-Temperature Environment

Jinhyun Noh, Hagyoul Bae, *Member, IEEE*, Junkang Li, Yandong Luo, Yiming Qu, Tae Joon Park, Mengwei Si, Xuegang Chen, Adam R. Charnas, Wonil Chung, Xiaochen Peng, *Graduate Student Member, IEEE*, Shriram Ramanathan, Shimeng Yu, *Senior Member, IEEE*, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— We have experimentally demonstrated robust beta-gallium oxide (β-Ga_2O_3) ferroelectric (FE) field-effect transistors (FeFETs) on a sapphire substrate operated up to 400 °C. Atomic layer deposited (ALD) $Hf_{0.5}Zr_{0.5}O_2$ [hafnium zirconium oxide (HZO)] is used as the FE dielectric. The HZO/β-Ga_2O_3 FeFETs are studied for their synaptic behavior applications at elevated temperatures. The devices show distinguishable polarization switching operation with the output conductance quasi-linearly controlled by the number of input pulses on the FE gate. In a simulation, on-chip learning accuracy reaches 94% at elevated temperatures using the Modified National Institute of Standards and Technology (MNIST) data set with a simple two-layer multilayer perceptron (MLP) network. These ultra wide bandgap semiconductor devices have the potential to fill the need for harsh environment neuromorphic applications.**

***Index Terms*— Beta-gallium oxide (β-Ga_2O_3), ferroelectric (FE), ferroelectric field-effect transistor (FeFET), hafnium zirconium oxide (HZO), high temperature, neuromorphic, on-chip learning, synaptic.**

I. Introduction

ELECTRONIC devices in harsh environments, mainly at high temperatures, are required for electronic warfare, command, control, communications, computing, surveillance, and reconnaissance in defense, and aerospace applications [1], [2]. At higher temperatures, the intrinsic carrier concentration (n_i) of semiconductors is no longer negligible, and the behavior of lightly doped regions in devices can become dominated by intrinsic carriers, resulting in device malfunction [3]. The wider the bandgap has, the lower n_i of the semiconductor is. That is why wide bandgap semiconductors are excellent candidates for those applications where the high-temperature operation is required.

Monolithic beta-gallium oxide (β-Ga_2O_3) is one of the emerging ultrawide bandgap semiconductors for power electronics. β-Ga_2O_3 provides a variety of advantages including its ultrawide bandgap of 4.8-4.9 eV, high breakdown electric field of 8 MV/cm, the high electron mobility of 100–150 $cm^2/V{\cdot}s$, and sustainability for high-temperature operation [4]. The availability of a native bulk substrate through melt-grown growth makes β-Ga_2O_3 cost-effective compared to SiC and GaN in practical applications [5]. Although β-Ga_2O_3 is mainly suitable for high-power applications, it is worth exploring its potential for low-power digital-like applications due to its robustness in harsh environments. Electronic devices used for rapid automation and intelligent decision-making in harsh environments are required in defense and aerospace applications. Neuromorphic artificial intelligence (AI) systems that can operate stably in harsh environments can be potentially realized by using ultrawide bandgap β-Ga_2O_3.

Manuscript received December 14, 2020; revised February 24, 2021; accepted March 4, 2021. Date of publication March 19, 2021; date of current version April 22, 2021. This work was supported in part by the Office of Naval Research's Naval Enterprise Partnership Teaming with Universities for National Excellence under Grant N00014-15-1-2833 and in part by Applications and Systems-Driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT), one of six centers in Joint University Microelectronics Program (JUMP), as Semiconductor Research Corporation (SRC) Program sponsored by Defense Advanced Research Projects Agency (DARPA). The work of Hagyoul Bae was supported in part by a Fellowship from NRF Korea. The work of Tae Joon Park and Shriram Ramanathan was supported by Energy Frontier Research Centers (EFRC) funded by the U.S. Department of Energy (DOE), Office of Science, Basic Energy Sciences (BES), under Award DE-SC0019273. The review of this article was arranged by Editor A. M. P. Anantram. *(Jinhyun Noh and Hagyoul Bae contributed equally to this work.) (Corresponding author: Peide D. Ye.)*

Jinhyun Noh, Hagyoul Bae, Junkang Li, Yiming Qu, Mengwei Si, Adam R. Charnas, Wonil Chung, and Peide D. Ye are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA, and also with the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Yandong Luo, Xiaochen Peng, and Shimeng Yu are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Tae Joon Park, Xuegang Chen, and Shriram Ramanathan are with the School of Materials Engineering, Purdue University, West Lafayette, IN 47907 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3064783.

Digital Object Identifier 10.1109/TED.2021.3064783

Meanwhile, hafnium zirconium oxide (HZO) is strongly ferroelectric (FE) at high temperatures. The Curie temperature for HZO is estimated to be beyond 1000 °C by temperature-dependent ferroelectricity measurement and modeling. Its compatibility with Si CMOS processing makes HZO one of the most widely studied FE materials for negative capacitance field-effect transistors (FETs), FeFETs, and nonvolatile memory [6]–[13]. Our previous work on HZO/β-Ga_2O_3 integration [14], β-Ga_2O_3 on high thermal conductivity (κ) substrates [15], and radiation hardness studies of β-Ga_2O_3 [16] provide a foundation to propose harsh environment neuromorphic AI applications.

In this work, we have successfully demonstrated HZO/β-Ga_2O_3 FeFETs as a promising building block for future synaptic devices that can operate at high temperatures. Specifically, the HZO/β-Ga_2O_3 FeFETs on sapphire substrates have robust electrical performances with profound polarization switching characteristics, steep subthreshold slope (SS), and high ON-current (I_{ON})/OFF-current (I_{OFF}) ratio even at high temperatures up to 400 °C. As a synaptic device, the conductance of the fabricated HZO/β-Ga_2O_3 FeFET can be quasi-linearly controlled by the number of pulses on the FE gate even at elevated temperatures. On-chip learning accuracy as high as 94% is demonstrated for the Modified National Institute of Standards and Technology (MNIST) based on the robust electrical performance of HZO/β-Ga_2O_3 FeFETs.

II. Device Fabrication

For the fabrication of the top-gate HZO/β-Ga_2O_3 FeFETs, Sn-doped β-Ga_2O_3 wafers (Tamura Corporation) were chosen. The doping concentration was measured at 2.7×10^{18} cm^{-3} by capacitance–voltage ($C-V$) measurement [17]. After cleaving the β-Ga_2O_3 bulk substrate into smaller pieces, mechanical exfoliation or the scotch tape method, which is widely used in 2-D materials research, was iterated ~15 times in order to achieve thin nanomembrane flakes. The exfoliated β-Ga_2O_3 nanomembrane flakes were transferred to a solvent-cleaned sapphire substrate. The sample was soaked in acetone for more than 20 min again to remove tape residues.

Before the source and drain formation, an FE HZO gate-stack of 1nm Al_2O_3/20 nm $Hf_{0.5}Zr_{0.5}O_2$/1 nm Al_2O_3 was deposited by atomic layer deposited (ALD) at 200 °C using TDMAHf ($([CH_3)_2N]_4Hf$), TDMAZr ($([CH_3)_2N]_4Zr$), TMA ($(CH_3)_3Al$), and H_2O as Hf, Zr, Al, and O precursors, respectively. The Hf:Zr ratio was decided to 1:1 because the FE hysteresis loop was strongest in this case [8]. The 1-nm amorphous Al_2O_3 layer on the bottom of the stack was applied to achieve better interface quality, and the top Al_2O_3 was deposited to avoid degradation of HZO by reaction with other contamination sources, such as moisture in the air [14]. After deposition, the sample was annealed in nitrogen ambient for 1 min at 500 °C using rapid thermal annealing (RTA) process in order to enhance the ferroelectricity.

Source and drain regions were patterned by electron-beam lithography (EBL) using a JEOL JBX-8100FS. ZEP 520A was used as the e-beam resist. Because of the presence of gate dielectric HZO, dry etching with BCl_3/Ar was performed after the source and drain regions were defined.

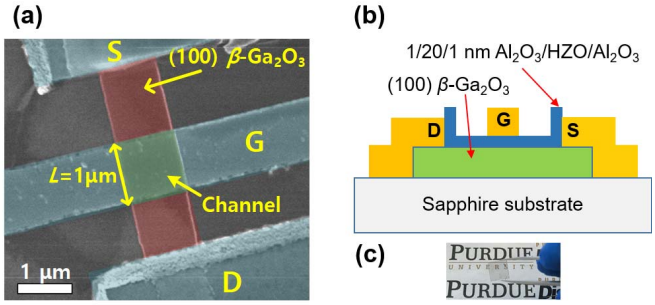

Fig. 1. (a) SEM image of a fabricated device with gate length (L_G) of 1 μm. (b) Cross-sectional schematic and (c) photograph of the fabricated HZO/β-Ga_2O_3 FE-FETs on a sapphire substrate.

Before metallization, an Ar plasma bombardment with radio frequency power of 100 W was applied to improve the contact resistance by generating oxygen vacancies to enhance the n-type surface of β-Ga_2O_3 flakes [18]. A Ti/Al/Au (15/60/50 nm) metal stack was deposited using an e-beam evaporation and liftoff process.

Finally, Ni/Au (50/50 nm) gate metal was formed using EBL, e-beam evaporation, and liftoff process, the same as the source and drain formation. After the whole fabrication, the devices were annealed at 400 °C in nitrogen ambient for 30 min to improve the source and drain contact resistance [19]. Fig. 1(a) shows a scanning electron microscopy (SEM) image of a top-gate HZO/β-Ga_2O_3 FeFET. Fig. 1(b) and (c) shows the cross-sectional schematic and a photograph of the HZO/β-Ga_2O_3 FeFETs on a sapphire substrate.

In order to check the ferroelectricity of HZO, TiN/HZO/TiN (30/20/30 nm) metal-FE-metal capacitors were fabricated and characterized. As shown in the polarization–voltage (P–V) measurement in Fig. 2(a), clear FE hysteresis loops are achieved at temperatures up to 400 °C. Fig. 2(b) shows transmission electron microscopy (TEM) analysis and energy-dispersive X-ray spectroscopy (EDS) element mapping for the HZO layer. Grain sizes ranging from 4 to 20 nm were found from the high-resolution TEM images. Taking the average grain size to be 10 nm gives 7000 grains in a device with a 1-μm channel length and a 0.7-μm channel width. The EDS analysis confirms the presence of uniformly distributed Hf, Zr, and O. Remnant polarization (P_r) versus temperature is shown in Fig. 2(c). P_r starts to decrease slightly above 300 °C, but the Curie temperature is still far above 400 °C. Coercive voltages (V_c) versus temperature is shown in Fig. 2(d), showing that V_c is almost constant with temperature increase. Fig. 2(e) shows the good retention performance of a fabricated FE HZO capacitor at a range of temperatures from 20 °C to 200 °C.

III. Experimental Results and Discussion

A. Robust Operation Under High Temperatures (up to 400 °C)

The transfer and output characteristics at various temperatures from 20 °C to 400 °C of a representative depletion-mode top-gate HZO/β-Ga_2O_3 FeFET with channel thickness of ~180 nm, source-to-drain distance (L_{SD}) of 2 μm, and gate length (L_G) of 1 μm are shown in Fig. 3(a) and (b). Most of the high gate voltage is used to deplete the β-Ga_2O_3

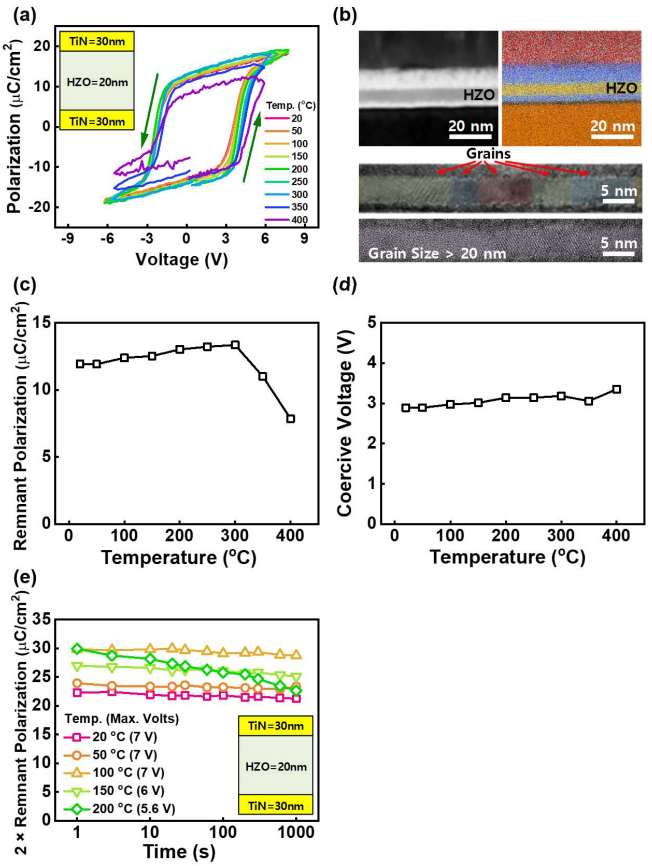

Fig. 2. (a) Temperature-dependent $P-V$ hysteresis loops of an FE TiN/HZO/TiN capacitor with HZO thickness of 20 nm and Hf:Zr = 1:1. (b) TEM image and EDS analysis of FE gate-stack similar to (a). (c) Remnant polarization and (d) coercive voltage-temperature characteristics. (e) Temperature-dependent retention test of an FE TiN/20 nm HZO/TiN capacitor.

channel instead of only biasing on FE dielectric in the device. All drain current (I_D)–gate-to-source voltage (V_{GS}) transfer curves have counterclockwise hysteretic characteristics with good polarization switching behaviors at the drain-to-source voltage (V_{DS}) = 1, 5, and 9 V. The negative hysteresis loop is caused by the ferroelectricity of the HZO layer. FE materials have a spontaneous electric polarization, which can be reversed by external electric fields. When a positive setup voltage is applied, dipoles inside HZO align in the direction of the electric field, and as a result, negative charges accumulate in the channel. This is why, when V_{GS} is swept from positive to a negative voltage, the device shows a higher current and conductance. On the other hand, when a sufficient negative voltage is applied, negative charges accumulated in the channel will be depleted when FE polarization flips. Instead of the steady-state setup voltage, if short-time positive or negative pulses are applied, the conductance of the channel will be changed only gradually since the HZO will be only partially polarized. These conductance stages can be used for weighted states in memory for neuromorphic device applications. In short, the FE window is an important performance metric of FeFETs. As shown in Fig. 3(b), I_D at high V_{DS} increases a little with increased temperature due to increased thermionic emission currents in contacts.

For further analysis, electrical parameters at various temperatures are compared in Fig. 4. The FE memory window is sustained at least over 4 V at temperatures up to 400 °C, as shown in Fig. 4(a). The memory window shows a V_{DS} dependence because, in the high drain bias regime, the higher electric field caused by the high gate-to-drain bias induces more charge trapping, which compensates for the FE hysteresis loop. Fig. 4(b) shows the I_{ON}/I_{OFF} ratio and SS, i.e., key device performance metrics, over a wide range of temperatures from 20 °C to 400 °C. As shown in the I_D–V_{GS} transfer curves in Fig. 3(a), I_{OFF} does not increase significantly at high temperatures. As the temperature increases, the I_{ON}/I_{OFF} ratio is slightly degraded because of a ~30% reduction in I_{ON} due to the degradation of channel mobility caused by phonon scattering at high temperatures. For a fair comparison to see the effect of high temperatures on the channel, all I_{ON}'s are extracted at V_{GS} equal to the threshold voltage (V_T)+ 3 V. In spite of a reduction in I_{ON}, the I_{ON}/I_{OFF} ratio is sustained around 1×10^6 at 400 °C. Due to the FE switching, FeFETs have steep SS under 60 mV/decade. Fig. 4(b) shows the minimum SS over the range of temperatures tested, which remains around 50 mV/decade due to the FE switching of HZO and the robustness of the β-Ga_2O_3 channel at high temperatures. In conclusion, the key neuromorphic properties are sustained at high temperatures up to 400 °C, making HZO/β-Ga_2O_3 FeFETs a strong candidate for neuromorphic computing applications in harsh environments.

As depicted in Fig. 5(a), the device contacts were generally improved after a nitrogen annealing process at 400 °C for 30 min. Note that all device measurements in Fig. 3 were carried out after the annealing. Fig. 5(b) shows the β-Ga_2O_3 film thickness-dependent V_T characteristics in devices on a sapphire substrate. The physical thickness of β-Ga_2O_3 nanomembranes was determined by atomic force microscopy (AFM). This V_T versus thickness trend is expected due to the depletion-mode operation of these β-Ga_2O_3 FeFETs, in agreement with the literature [18]. Accordingly, we can reduce V_T for neuromorphic applications by controlling the physical thickness of β-Ga_2O_3 flakes.

B. Feasibility of Neuromorphic Device Applications

To study the feasibility of neuromorphic device applications, an 80-nm thin HZO/β-Ga_2O_3 FeFET with L_{SD} of 3.45 μm, L_G of 1 μm, the gate width (W) of 0.7 μm, and V_T of near 0 V was chosen for pulse measurements to characterize the gradual conductance change of the channel by short rectangular voltage pulses due to partial polarization. Fig. 6(a) shows representative I_D–V_{GS} characteristics for a synaptic device. The original I_D–V_{GS} curve was shifted using nongrounded source voltage (V_S) in order to use 0 V as the base voltage of pulses. V_{DS} was fixed to 1 V by applying drain voltage (V_D) as source voltage (V_S) + 1 V. Fig. 6(b) depicts a schematic of the applied pulses. Rectangular-type pulses ranging from 0 to 10 V and from 0 to −10 V for 300 ns were applied to the gate for potentiation and depression, respectively.

Fig. 7(a) shows a schematic view of the pseudo-crossbar array architecture with HZO/β-Ga_2O_3 FeFET synapses [20].

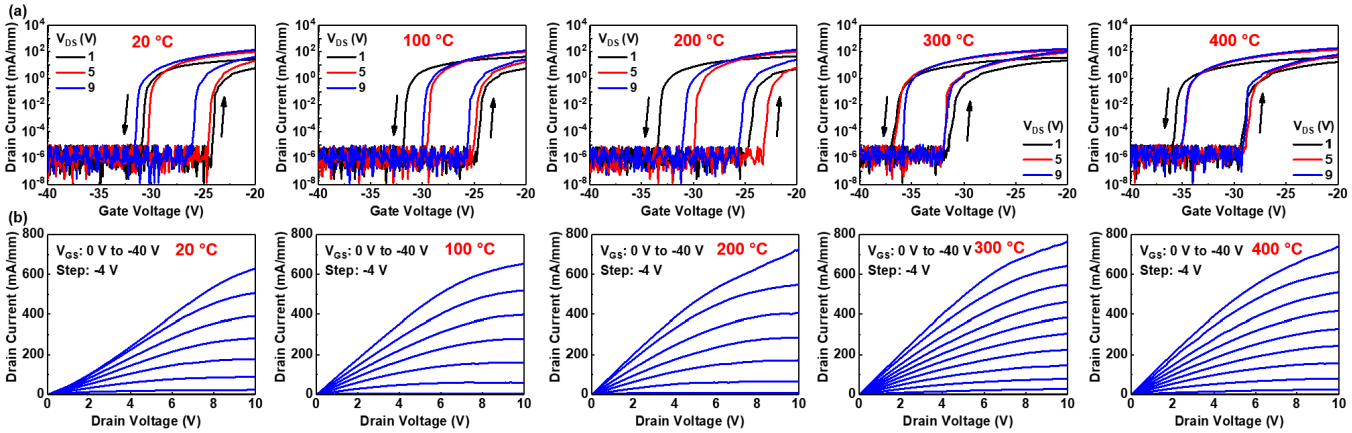

Fig. 3. Measured (a) I_D–V_{GS} with countercilockwise hysteresis loop and (b) I_D–V_{DS} characteristic curves of a fabricated HZO/β-Ga_2O_3 FET on a sapphire substrate at various temperatures up to 400 °C. ($L_g = 1\mu$m, $L_{SD} = 2\mu$m, and thickness: ~180 nm.) A gate voltage sweep range of $-40 \sim -10$ V is used for I_D–V_{GS} at 20 °C, 100 °C, and 200 °C, and $-50 \sim -20$ V is used for I_D–V_{GS} at 300 °C and 400 °C. Bulk and interface trap density could be changed at different temperatures since more deep traps inside the β-Ga_2O_3 band could be activated at high temperatures causing V_T to be shifted with temperature.

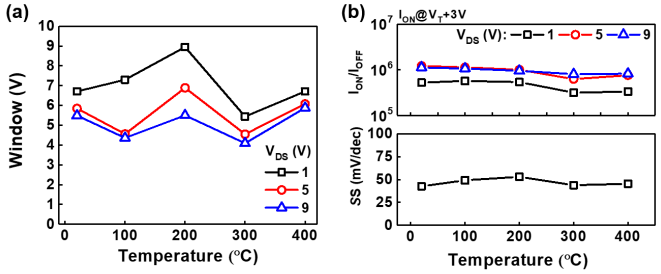

Fig. 4. (a) FE counterclockwise hysteresis memory window and (b) temperature dependence of I_{ON}/I_{OFF} ratio and SS of a fabricated HZO/β-Ga_2O_3 FET on a sapphire substrate at elevated temperatures of Fig. 3(a). All I_{on}'s are extracted at V_{GS} equal to $V_T + 3$ V. All SSs are taken from forward sweeps at $V_{GS} = 1$ V.

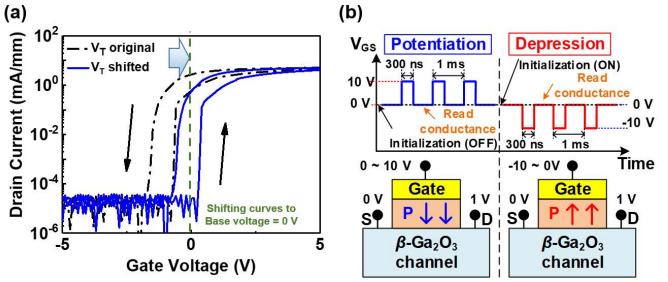

Fig. 6. (a) I_D–V_{GS} characteristics of the HZO/β-Ga_2O_3 FeFETs used for a synaptic device $V_{DS} = 1$ V. The original I_D–V_{GS} curve was shifted using nongrounded V_S in order to use 0 V as the base voltage of pulses. (b) Applied pulse cycle and read scheme in the HZO/β-Ga_2O_3 FeFETs for potentiation and depression.

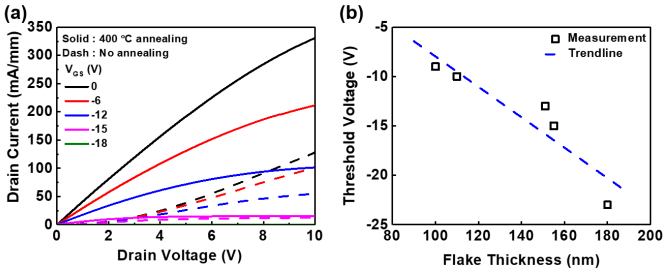

Fig. 5. (a) Measured output I_D–V_{DS} characteristics before and after extra thermal annealing (400 °C) and $L_g = 1$ μm. The device shown in (a) is different from that in Fig. 3 and Fig. 4. (b) V_T versus the β-Ga_2O_3 thickness on a sapphire substrate.

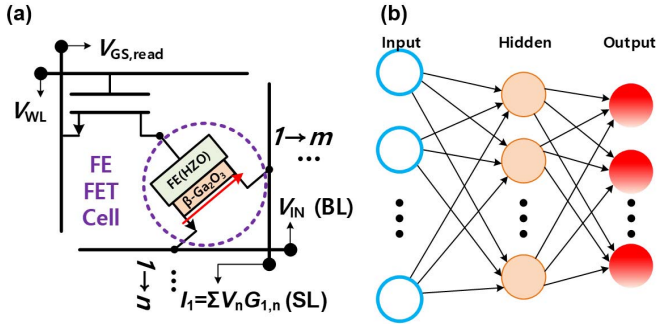

Fig. 7. (a) Schematic view of the concept of the pseudocrossbar array architecture with β-Ga_2O_3-based synapse. (b) Schematic configuration of the simulated neural network.

During programming, a high voltage is applied to the word line (WL), and the programming pulses are applied to the gate of the HZO/β-Ga_2O_3 FeFET. The channel conductance of the FeFET is programed by partial polarization switching. For neuromorphic applications, all the access transistors are turned on. The input vectors are binarized and applied to the horizontal bitline (BL) as the input voltage (V_{IN}) or 0 V, representing digits 1 and 0, respectively. An N-bit input is fed into the array in N cycles. The weighted sum is obtained as column current along the vertical source line (SL). The analog weighted sum current is converted into digital values by an analog-to-digital converter in the array periphery circuit. Shift and add are needed to get the weighted sum of input bit $N > 1$. Fig. 7(b) depicts the two-layer multilayer perceptron (MLP) network used for simulation, where the number of hidden neurons in the network is 100. On-chip learning of the MNIST data set is demonstrated with this MLP network using the extracted HZO/β-Ga_2O_3 FeFET parameters.

The conductance of the device increases or decreases quasi-linearly due to partial polarization switching induced by consecutive identical potentiation or depression pulses, as shown

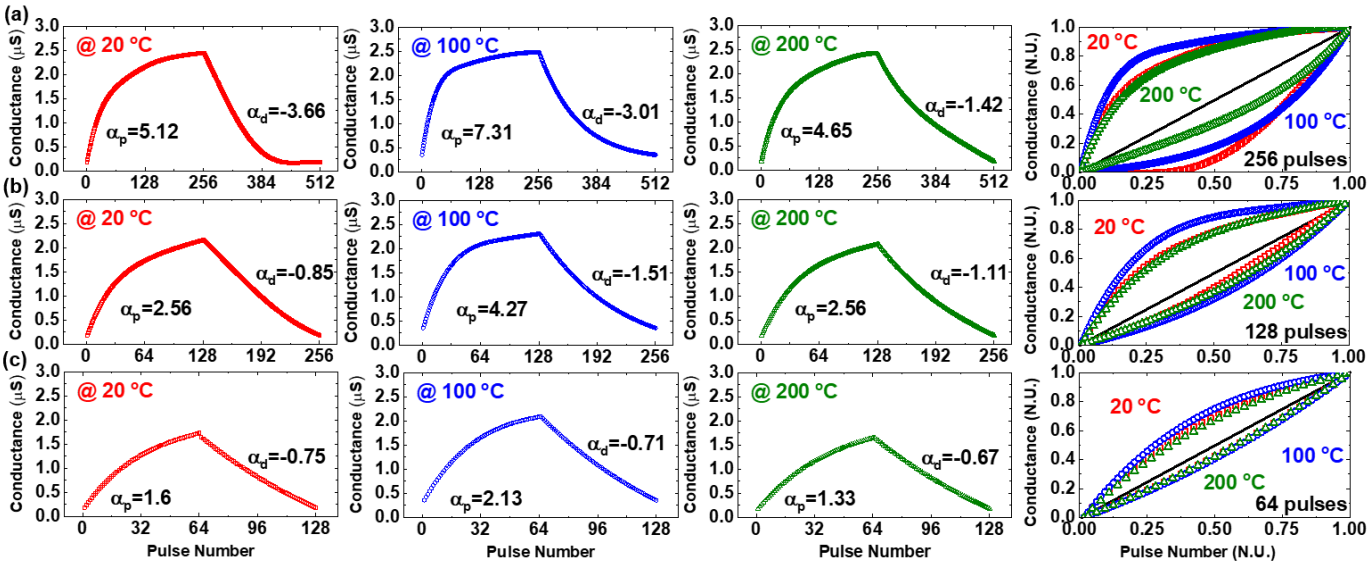

Fig. 8. Analog conductance modulation behavior as a function of the number of pulse cycles of (a) 256, (b) 128, and (c) 64 at a range of temperatures from 20 °C to 200 °C.

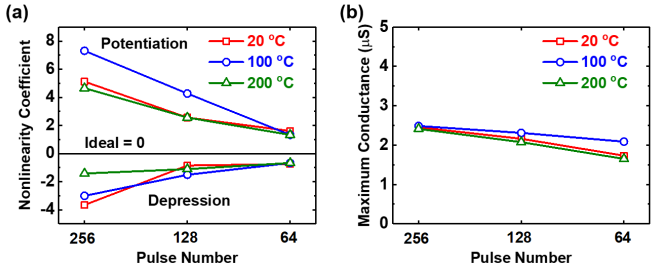

Fig. 9. (a) Nonlinearity coefficient and (b) maximum conductance level versus pulse number at temperatures of 20 °C, 100 °C, and 200 °C.

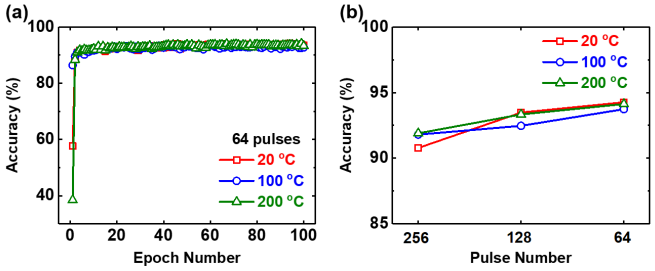

Fig. 10. (a) Accuracy versus epoch number of pulse cycles of 64 at a range of temperatures from 20 °C to 200 °C in a training simulation based on MLP+NeuroSimV3.0. (b) Accuracy versus pulse number at temperatures of 20 °C, 100 °C, and 200 °C.

in Fig. 8. Different nonlinearities of the conductance update curve are obtained with pulse numbers of 256, 128, and 64, as shown in Fig. 8(a)–(c), respectively. In the figure, α_p and α_d are the nonlinearity factors for potentiation and depression, respectively, which is calculated by fitting the experimental profiles to a reported model [21]. As the temperature increases from 20 °C to 200 °C, α_p and α_d are not degraded. Besides, only a slight change of the maximum conductance ($G_{\max}$) and the minimum conductance ($G_{\min}$) values is observed at high temperatures. In short, the ability of HZO/β-Ga_2O_3 FeFETs as synapse devices is checked at a wide range of temperatures from 20 °C to 200 °C. However, the pulse number strongly affects nonlinearity and $G_{\max}$. As pulse number decreases, nonlinearity is drastically improved, as shown in Fig. 9(a). However, $G_{\max}$ decreases, as shown in Fig. 9(b). Moreover, a lower pulse number means fewer levels of weighted current in the neuromorphic device. In other words, there is a tradeoff between nonlinearity and $G_{\max}$.

The on-chip learning and system-level benchmark were conducted in the MLP+NeuroSimV3.0 simulation framework with the two-layer MLP network mentioned previously [22]. The on-chip learning was trained using the adaptive momentum estimation (ADAM) algorithm to perform handwritten digit classification for the MNIST data set [23]–[25]. The training process using representative 64 pulse curves at various temperatures shows that the classification accuracy reaches its maximum level in a few epochs in Fig. 10(a). Fig. 10(b) shows a comparison of simulation results for on-chip learning accuracy at various temperatures and numbers of conductance states. The results indicate that HZO/β-Ga_2O_3 FeFETs should show a stable on-chip learning accuracy over a large range of temperatures. The 64-state programming scheme shows the best online accuracy because the training accuracy mainly depends on the nonlinearity factor.

A predicted system-level benchmark of the HZO/β-Ga_2O_3 FeFETs synapse is conducted at the 32-nm node at both device and circuit temperature of 100 °C, and the results are summarized in Table I. The device temperature of 100 °C includes nonlinearities that are extracted from pulse measurement at 100 °C. The MLP+NeuroSimV3.0 simulation framework supports from room temperature to 125 °C. Consequently, the simulation at 100 °C was picked for the benchmark. Previously reported synaptic devices based on resistive switching are also considered for comparison purposes. To make a fair comparison, the FeFET device is benchmarked under its original device size and the device size when scaled to a 32-nm node. The scaling trend of FeFET channel conductance

TABLE I
BENCHMARKING OF VARIOUS SYNAPTIC DEVICES

Device type	Ag:a-Si [26] (projected to 32 nm)	PCMO [27] (projected to 32 nm)	AlO_x/HfO_2 [28] (projected to 32 nm)	HZO/ β-Ga_2O_3 Fe-FET (original size, device: 100 °C, circuit: 100 °C) **This work**	HZO/ β-Ga_2O_3 Fe-FET (projected to 32 nm*, device: 100 °C, circuit: 100 °C) **This work**
# of conductance states	97	50	40	64	64
Nonlinearity (α_p/ α_d)	2.4/-4.88	3.68/-6.76	1.94/-0.61	2.13/-0.71	2.13/-0.71
R_{ON}	26 MΩ	23 MΩ	16.9 kΩ	478.5 kΩ	**2.20 MΩ**
G_{max}/G_{min} ratio	12.5	6.84	4.43	5.85	5.85
Weight increase pulse	3.2 V/300 µs	2 V/1 ms	0.9 V/100 µs	10 V/300 ns	10 V/300 ns
Weight decrease pulse	-2.8 V/300 µs	-2 V/1 ms	-1 V/100 µs	-10 V/300 ns	-10 V/300 ns
Cycle-to-cycle variation (σ)	3.5%	<1%	5%	**<0.5%**	**<0.5%**
On-chip learning accuracy	~90%	~90%	~91%	**~93.9%**	**~93.7%**
Area	6,292.3 μm^2	6,292.3 μm^2	21,846 μm^2	266,540 μm^2	6,814.8 μm^2
Latency (optimized)	22,402 s	16,545 s	679 s	11.40 s	11.11 s
Energy (optimized)	10.9 mJ	3.5 mJ	26.1 mJ	50.22 mJ	10.43 mJ

*This value requires experimental verifications

is assumed to follow that of regular complementary metal–oxide–semiconductor (CMOS) transistors, which is extracted from the predictive technology model (PTM) [29]. Both the amplitude and duration of the programming pulse are assumed not to change with device scaling. From the results in Table I, the HZO/β-Ga_2O_3 FeFETs have a good on-chip learning accuracy of 94% due to their relatively high linearity and small cycle to cycle variation (σ). With the original device size, the high programming voltage of 10 V and large gate capacitance of the FeFET lead to relatively high energy consumption. However, when the FeFET is scaled down to the 32-nm node, the energy consumption will be reduced due to the relatively large ON-state resistance (R_{ON}) and smaller gate capacitance, which is comparable to or even smaller than synaptic devices based on resistive-switching. The energy consumption can be further reduced if the programming voltage is reduced. Besides, the low programming pulsewidth (~100-ns level) of the FeFETs significantly reduces the latency for on-chip learning compared to the resistive switching-based synaptic devices with μs- or ms-level programming pulse widths. The temperature dependence between 20 °C and 200 °C is very weak. The results indicate that the demonstrated HZO/β-Ga_2O_3 FeFETs are competitive and encouraging for neuromorphic applications at high temperatures.

IV. CONCLUSION

In this work, robust HZO/β-Ga_2O_3 FeFETs on a sapphire substrate have been demonstrated at operating temperatures up to 400 °C. The FE memory window and other electrical properties, such as the SS and I_{ON}/I_{OFF} ratio of the fabricated FeFETs, were excellent and are sustained at temperatures up to 400 °C without severe degradation. Robust electrical performance enables synaptic device demonstration with an on-chip learning accuracy of 94% at elevated temperatures and offers the potential to use this novel device architecture as a building block for neuromorphic computing and AI applications exposed to harsh environments.

ACKNOWLEDGMENT

The authors acknowledge the XRD work by N. Draeger and K. Nardi of Lam Research and the TEM and EDS work by X. Sun and H. Wang of Purdue University.

REFERENCES

[1] M. R. Werner and W. R. Fahrner, "Review on materials, microsensors, systems and devices for high-temperature and harsh-environment applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 249–257, Apr. 2001, doi: 10.1109/41.915402.

[2] M. Mehregany, C. A. Zorman, N. Rajan, and C. Hung Wu, "Silicon carbide MEMS for harsh environments," *Proc. IEEE*, vol. 86, no. 8, pp. 1594–1609, Aug. 1998, doi: 10.1109/5.704265.

[3] J. Y. Tsao *et al.*, "Ultrawide-bandgap semiconductors: Research opportunities and challenges," *Adv. Electron. Mater.*, vol. 4, no. 1, Jan. 2018, Art. no. 1600501, doi: 10.1002/aelm.201600501.

[4] M. Higashiwaki *et al.*, "Recent progress in Ga_2O_3 power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, Jan. 2016, Art. no. 034001, doi: 10.1088/0268-1242/31/3/034001.

[5] M. Higashiwaki and G. H. Jessen, "Guest editorial: The dawn of gallium oxide microelectronics," *Appl. Phys. Lett.*, vol. 112, no. 6, Feb. 2018, Art. no. 060401, doi: 10.1063/1.5017845.

[6] M. Si *et al.*, "Steep-slope hysteresis-free negative capacitance MoS_2 transistors," *Nature Nanotechnol.*, vol. 13, no. 1, pp. 24–28, Jan. 2018, doi: 10.1038/s41565-017-0010-1.

[7] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S. K. Gupta, "Device-circuit analysis of ferroelectric FETs for low-power logic," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3092–3100, Aug. 2017, doi: 10.1109/TED.2017.2717929.

[8] X. Lyu, M. Si, X. Sun, M. A. Capano, H. Wang, and P. D. Ye, "Ferroelectric and anti-ferroelectric hafnium zirconium oxide: Scaling limit, switching speed and record high polarization density," in *Proc. Symp. VLSI Technol.*, Jun. 2019, doi: 10.23919/VLSIT.2019.8776548.

[9] J. Muller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, Dec. 2013, pp. 280–283, doi: 10.1109/IEDM.2013.6724605.

[10] W. Chung, M. Si, P. R. Shrestha, J. P. Campbell, K. P. Cheung, and P. D. Ye, "First direct experimental studies of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric polarization switching down to 100-picosecond in sub-60 mV/dec germanium ferroelectric nanowire FETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 89–90, doi: 10.1109/VLSIT.2018.8510652.

[11] K. Ni, X. Li, J. A. Smith, M. Jerry, and S. Datta, "Write disturb in ferroelectric FETs and its implication for 1T-FeFET AND memory arrays," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1656–1659, Nov. 2018, doi: 10.1109/LED.2018.2872347.

[12] M. Seo *et al.*, "First demonstration of a logic-process compatible junctionless ferroelectric FinFET synapse for neuromorphic applications," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1445–1448, Sep. 2018, doi: 10.1109/LED.2018.2852698.

[13] W. Chung, M. Si, and P. D. Ye, "First demonstration of Ge ferroelectric nanowire FET as synaptic device for online learning in neural network with high number of conductance state and G_{max}/G_{min}," in *IEDM Tech. Dig.*, Dec. 2018, pp. 344–347, doi: 10.1109/IEDM.2018.8614516.

[14] M. Si, L. Yang, H. Zhou, and P. D. Ye, "β-Ga_2O_3 nanomembrane negative capacitance field-effect transistors with steep subthreshold slope for wide band gap logic applications," *ACS Omega*, vol. 2, no. 10, pp. 7136–7140, 2017, doi: 10.1021/acsomega.7b01289.

[15] J. Noh *et al.*, "High performance β-Ga_2O_3 nano-membrane field effect transistors on a high thermal conductivity diamond substrate," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 914–918, 2019, doi: 10.1109/JEDS.2019.2933369.

[16] M. A. Bhuiyan *et al.*, "Charge trapping in Al_2O_3/β-Ga_2O_3-based MOS capacitors," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1022–1025, Jul. 2018, doi: 10.1109/LED.2018.2841899.

[17] H. Zhou, S. Alghamdi, M. Si, G. Qiu, and P. D. Ye, "Al_2O_3/β-Ga_2O_3(-201) interface improvement through piranha pretreatment and postdeposition annealing," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1411–1414, Nov. 2016, doi: 10.1109/LED.2016.2609202.

[18] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. D. Ye, "High-performance depletion/enhancement-ode β-Ga_2O_3 on insulator (GOOI) field-effect transistors with record drain currents of 600/450 mA/mm," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 103–106, Jan. 2017, doi: 10.1109/LED.2016.2635579.

[19] Y. Yao, R. F. Davis, and L. M. Porter, "Investigation of different metals as ohmic contacts to β-Ga_2O_3: Comparison and analysis of electrical behavior, morphology, and other physical properties," *J. Electron. Mater.*, vol. 46, no. 4, pp. 2053–2060, 2017, doi: 10.1007/s11664-016-5121-1.

[20] P.-Y. Chen, X. Peng, and S. Yu, "NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 12, pp. 3067–3080, Dec. 2018, doi: 10.1109/TCAD.2018.2789723.

[21] P.-Y. Chen, X. Peng, and S. Yu, "NeuroSim+: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures," in *IEDM Tech. Dig.*, Dec. 2017, pp. 135–138, doi: 10.1109/IEDM.2017.8268337.

[22] Y. Luo, X. Peng, and S. Yu, "MLP+NeuroSimV3.0: Improving on-chip learning performance with device to algorithm optimizations," in *Proc. Int. Conf. Neuromorphic Syst.*, Jul. 2019, pp. 1–7, doi: 10.1145/3354265.3354266.

[23] S. Yu, "Neuro-inspired computing with emerging nonvolatile memorys," *Proc. IEEE*, vol. 106, no. 2, pp. 260–285, Feb. 2018, doi: 10.1109/JPROC.2018.2790840.

[24] M. Jerry *et al.*, "Ferroelectric FET analog synapse for acceleration of deep neural network training," in *IEDM Tech. Dig.*, Dec. 2017, pp. 139–142, doi: 10.1109/IEDM.2017.8268338.

[25] S. Park *et al.*, "RRAM-based synapse for neuromorphic system with pattern recognition function," in *IEDM Tech. Dig.*, Dec. 2012, pp. 231–234, doi: 10.1109/IEDM.2012.6479016.

[26] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, Apr. 2010, doi: 10.1021/nl904092h.

[27] S. Park *et al.*, "Neuromorphic speech systems using advanced ReRAM-based synapse," in *IEDM Tech. Dig.*, Dec. 2013, pp. 625–628, doi: 10.1109/IEDM.2013.6724692.

[28] J. Woo *et al.*, "Improved synaptic behavior under identical pulses using AlO_x/HfO_2 bilayer RRAM array for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 994–997, Aug. 2016, doi: 10.1109/LED.2016.2582859.

[29] W. Zhao and Y. Cao, "Predictive technology model for nano-CMOS design exploration," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 3, no. 1, p. 1, Apr. 2007, doi: 10.1145/1229175.1229176.