Experimental Extraction of Ballisticity in Germanium Nanowire nMOSFETs

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***Abstract*— In this paper, we report the experimental extraction of ballistic transport parameters of high-performance Germanium Nanowire nMOSFETs (Ge NWTs) with lengths L_{NW} = 40–100 nm, width W_{NW} = 40 nm, and height H_{NW} = 10 nm using temperature-dependent measurements. The extracted contact resistivity (ρc) and sheet resistance (Rsh) imply that parasitic series resistance (R_{SD}) of fabricated Ge NWTs is affected by ρ_c of the metal-nGe ($3.42 \times 10^{-5}\ \Omega \cdot cm^2$ at 292 K), which decreases with the increase in temperature. Ballistic efficiency (BE) is found to be 22%–47% at 292 K depending on the dimension of the device. It decreases with increased temperature and increases with L_{NW} scaling down to 40 nm. The transition region with fluctuating BE is observed near L_{NW} = 50–60 nm, where the electron transport enters deeper into bthe allistic regime. BE is found to be sensitive to temperature and drops from 58% (170 K) to 37% (390 K) for L_{NW} = 40-nm Ge NWT. Therefore, in order to maintain the high ballisticity of the devices, it is important to optimize the device structure and eliminate the self-heating effect.**

***Index Terms*— Ballistic efficiency (BE), contact resistance, germanium, germanium-on-insulator (GeOI), nanowire, recessed channel, recessed source/drain (S/D).**

I. Introduction

As TRANSISTOR channel length and equivalent oxide thickness (EOT) scale down for higher performances, integration of high-mobility channels such as Germanium or III–V into Si CMOS platform have been extensively studied in various structures [1]–[10]. Recently, we have developed fabrication process that uses dry-etched recessed channel, precisely etched source, and drain region for higher performance Ge NMOS devices (from planar to FinFET and nanowire structures) on germanium-on-insulator (GeOI) substrate which led to the first demonstration of Ge nanowire CMOS circuits [1]–[3]. High-quality Ge nanowire NMOS transistors with nanowire length (L_{NW}) down to 40 nm were fabricated with recessed n-type source and drain (S/D) contact formation which reduces the Schottky barrier width and contact resistance. Along with the advent of devices maximizing the performances in the deep sub-100-nm regime, analysis of ballistic carrier transport has also become indispensable. Theoretical studies related to the transition from diffusive to ballistic carrier transport regimes were discussed actively as the device dimensions shrunk rapidly [11]–[14]. There are multiple research studies, both simulations and experiments, discussing ballistic transport properties of devices (planar to nanowires) based on Si [14]–[22], III–V [23], [24], or Ge [25]–[28]. However, due to difficulties in realizing high-performance Ge nMOS devices, ballistic parameter studies on the state-of-the-art Ge nanowire transistors were rarely reported, in particular *experimentally*. With smaller device dimensions, transistors enter quasi-ballistic regimes in which the carriers face less scattering and become more ballistic [11], [13], [14]. Nearing the ballistic limit, the backscattering coefficient (R) and ballistic efficiency (BE) approaches 0 and 1, respectively, and the ON-current (I_{Dsat}) becomes a function of injection velocity, not the carrier velocity in the channel [14] which imposes significant importance in studying the source to channel injection process.

The conceptual diagram of channel backscattering present in the short-channel device is illustrated in Fig. 1. Using Lundstrom's scattering theory of MOSFET [29] at high V_{DS}, carriers are modeled to be partially (R) reflected back into the source upon entering the channel region, leaving only 1-R

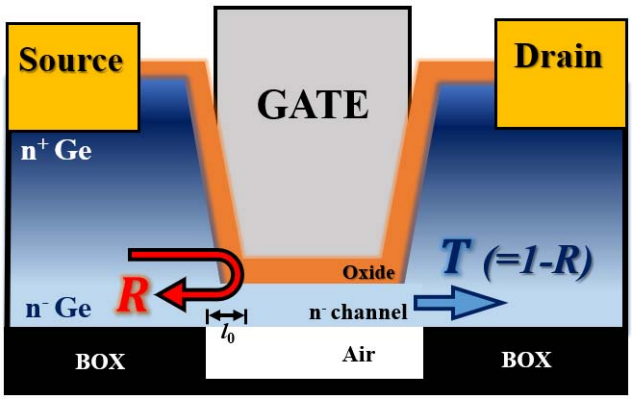

Fig. 1. Conceptual image of channel backscattering in the nanowire structure studied in this paper under carrier scattering model [29]. Carriers are reflected back into the source by a factor of R within the critical length (l_0) and a fraction of T is transmitted to the drain. R nears 0 as transistors approach higher ballisticity. Note that the bottom part of the Ge layer is doped with significantly lower concentration (few orders of magnitude) when compared to the source/drain contact area.

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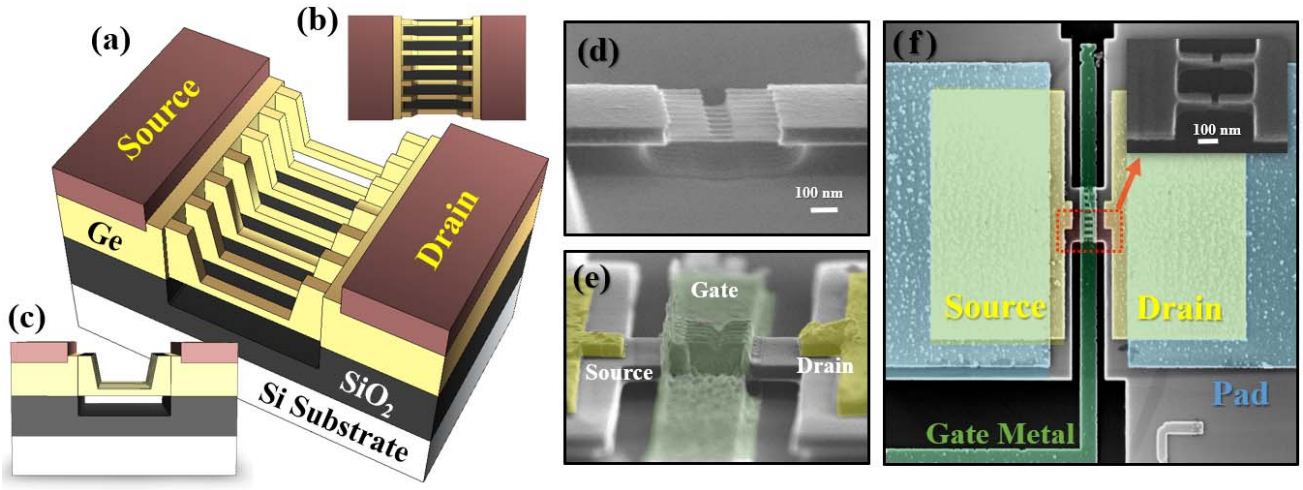

Fig. 2. (a) 3-D device structures of nanowire devices fabricated for BE measurement seen from (b) top and (c) front without gate metal. (d)–(f) SEM images of the fabricated nanowires taken from various angles. Gate–Source and Drain regions were colored differently. Nanowires (d) before and (e) after gate metallization are shown separately. Note that the nanowires are suspended in the air by etching away the SiO_2 underneath the nanowires.

portion, defined as transmission coefficient T, to be transmitted into the drain region. Carriers undergo high probability of reflection, losing its potential energy within this critical portion of the channel which is defined as the critical length l_0. It will be discussed more in Section III.

To extract ballisticity using definition-oriented method, several factors such as carrier degeneracy, charge density, injection velocity, source Fermi level, Fermi–Dirac integrals and appropriate effective masses for various equations need to be calculated [16], [29]. In fact, there are various approaches for estimation of ballisticity. The virtual source (VS) model can be fitted to the experimentally acquired data to directly determine various parameters such as the ballistic thermal velocity leading toward ballisticity estimation [30], [31]. This method does not require any temperature-dependent measurements throughout the extraction process, but the *CV* data should be first addressed for curve fitting. Another experimental methods that have been used for extraction of ballistic transport parameters is a temperature-dependent analysis of current–voltage ($I-V$) characteristics [17]–[21]. This method can be utilized to extract λ_0/l_0 ratio (λ_0: near-equilibrium mean-free-path) from temperature-dependent $I-V$ graphs which leads to channel backscattering coefficient R, transmission coefficient T and BE. It is noteworthy to state that this method does not require any *CV* measurements, such as split *CV*, which could be very challenging in nanoscale 3-D devices.

In this paper, temperature-dependent extraction method was employed for parameter analysis on accumulation-mode (AM) nGe NWTs with nanowire length $L_{\mathrm{NW}} = 40$–100 nm, width $W_{NW} = 40$ nm, and height $H_{\mathrm{NW}} = 10$ nm. Wide range of temperature (170–390 K) was used to extract the temperature-dependent parameters from the measured $I-V$ data.

II. Experiment

GeOI wafer from Soitec was used for the device fabrication. The thickness of the undoped Ge (100) layer on 400-nm SiO_2 is approximately 100 nm. After standard HF, acetone, methanol, and isopropanol wet cleaning of the wafer, source and drain regions were patterned and ion implantation (P, 5 $\times 10^{15}$ cm^{-2}, 15 keV) was done. The top 90 nm of Ge in the channel region was dry-etched with SF_6-based chemistry to define nanowire height (H_{NW}) of 10 nm. Multiple parallel nanowires were defined with electron-beam lithography and dry etching, forming seven wires in parallel per device. After the definition of nanowire dimensions, they were released from underlying SiO_2 through *partial* SiO_2 etching with 4% HF solution. The final nanowire length (L_{NW}) ranges from 40 to 100 nm and the width was fixed at 40 nm. Nanowires did not receive any thermal treatments after ion implantation up to this step to keep low doping concentration in the channel area ($\sim 1 \times 10^{16}$ cm^{-3}, bottom 10 nm of Ge layer) than the S/D regions ($> 1 \times 10^{19}$ cm^{-3}, the top part of the Ge layer). With this doping profile, there still exists an energy barrier between the highly doped source/drain region and the low-doped channel unlike uniformly highly doped junctionless transistors (JLFETs).

Gate oxide (Al_2O_3) was deposited using atomic layer deposition (ALD) system in two separate steps. 1-nm Al_2O_3 was first deposited, followed by postoxidation (O_2, 500 °C, 30 s) forming a thin GeO_x layer underneath Al_2O_3. This postoxidation was done in rapid thermal annealing (RTA) system which also serves as the activation of the implanted ions in the S/D regions. The additional 8-nm Al_2O_3 was deposited after postoxidation to achieve EOT of 5 nm in total.

After the formation of the gate-stack ($Ge/GeO_x/Al_2O_3$), the source and drain contact regions were etched precisely with the optimized condition using an inductively coupled plasma etching to form recessed S/D contacts that enable high-performance contact properties between n-type Ge and Ni, the S/D metal. The ohmic annealing was carried out (N_2, 250 °C, 30 s) and gate metal (Ni/Au) was patterned and deposited along with S/D contact pads. SEM images and 3-D device structure of the fabricated devices are presented in Fig. 2.

III. Extraction Method

The method used in this paper is extraction of ballisticity of a transistor through temperature-dependent $I-V$ measurement data [17], [18] that require measurement of several parameters from conventional output characteristic and transfer curves. Unlike the definition-oriented method mentioned earlier, this method only requires temperature-dependent $I-V$ data excluding any CV characterization

$$I_{\mathrm{Dsat}} = W \times Q_{\mathrm{sat}} \times v_{\mathrm{inj}} \times \frac{\lambda_0/l_0}{2+\lambda_0/l_0} \tag{1}$$

$$Q_{\mathrm{sat}} = C_{\mathrm{ox}} \times (V_G - V_{\mathrm{Tsat}} - I_{\mathrm{Dsat}} R_S). \tag{2}$$

Under Lundstrom's scattering theory model [29], [32], saturation drain current can be written as (1) with a critical length $l_0(\propto T)$, mean-free-path λ_0, and injection velocity v_{inj} $(\propto\sqrt{T})$, all of which are functions of temperature [32]. The critical length l_0 is a distance in which the carriers face potential drop by the amount of kinetic energy that it was originally injected with. Therefore, when the carriers travel into the channel further than the critical length, they are unable to return to the source due to lack of enough energy. The mean-free-path λ_0 can be expressed with injection velocity as in (3) and it stems from the Einstein relations [29]. Equation (2) can be used for our AM transistors considering similarities to its inversion mode counterpart [33]

$$\lambda_0 = \frac{2\mu k_B T}{v_{\mathrm{inj}}}. \tag{3}$$

The charge density in the channel at saturation (Q_{sat}) shown in (2) considers the series resistance (R_S) of the device since the nanowires inherently suffer from high access resistances from the contact area to the active channel region unlike planar contacts where contact areas lie adjacent to the channel. Our devices exhibit R_S that is strongly dependent on the barrier height and width of the nGe/metal contact interface [2] which would undoubtedly be temperature-dependent. Even without specific consideration of nGe/metal contact properties, R_S in nanowire is temperature-dependent [18], [34] and, therefore, differentiating (2) with T should result in (4) including several parameters defined in (5)

$$\frac{\mathrm{dQ_{sat}}}{\mathrm{dT}} = C_{\mathrm{ox}} \times \left(-\frac{\mathrm{dV_{Tsat}}}{\mathrm{dT}} - \frac{\mathrm{dI_{Dsat}}}{\mathrm{dT}} R_S - I_{\mathrm{Dsat}} \times \frac{\mathrm{dR_S}}{\mathrm{dT}}\right)$$

$$= C_{\mathrm{ox}} \times (-\eta - \alpha I_{\mathrm{Dsat}} R_S - \beta I_{\mathrm{Dsat}}) \tag{4}$$

$$\alpha = \frac{\mathrm{dI_{Dsat}/dT}}{I_{\mathrm{Dsat}}}, \beta = \frac{\mathrm{dR_S}}{\mathrm{dT}}, \eta = \frac{\mathrm{dV_{Tsat}}}{\mathrm{dT}}. \tag{5}$$

For AM transistors, V_{Tsat} in (2) can be understood as flat band voltage (V_{FB}) [35] since AM devices *turn on*when V_G exceeds V_{FB}. Therefore, (2) was used and temperature-dependent threshold voltage (η) was tracked from the measured $I-V$ data. The temperature-dependent percentage difference in saturation drain current (α), source series resistance (β), and threshold voltage (η) should be monitored with respect to temperature

$$\alpha = \frac{\frac{dI_{\mathrm{Dsat}}}{\mathrm{dT}}}{I_{\mathrm{Dsat}}} = \frac{1}{T}\left\{\frac{1}{2} - \frac{4}{\frac{\lambda_0}{l_0}+2}\right\} + \frac{-\eta - \alpha I_{\mathrm{Dsat}} R_S - \beta I_{\mathrm{Dsat}}}{V_G - V_{\mathrm{Tsat}} - I_{\mathrm{Dsat}} R_S} \tag{6}$$

$$\frac{\lambda_0}{l_0} = \frac{4}{\frac{1}{2} - T\left\{\alpha + \frac{\eta + I_{\mathrm{Dsat}}(\alpha R_S + \beta)}{V_G - V_{\mathrm{Tsat}} - I_{\mathrm{Dsat}} R_S}\right\}} - 2. \tag{7}$$

α can be further elaborated with ca ombination of parameters as shown in (6). It is noteworthy to mention that the mobility is assumed to be$\mu \propto T^{-1.5}$ [17], which implies dominant phonon scattering. As mentioned earlier, the doping concentration in the channel area (n-type, $\sim 1\times10^{16}$ cm^{-3}) is few orders lower than the source/drain areas (n-type, $\sim 1\times10^{19}$ cm^{-3}). Also, it is reported that Ge nMOSFET fabricated on GeOI wafer utilizing the exact same recessed channel, source and drain technique exhibits similar mobility trend [27]. If a different empirical exponent of σ is taken instead of -1.5, it would result in diffthe erent formula in (6) where 4 in the numerator is replaced with $1-2\sigma$

$$R = 1-T = \frac{l_0}{l_0+\lambda_0} = \frac{1}{1+\lambda_0/l_0} \tag{8}$$

$$\mathrm{BE_{sat}} = \frac{I_{\mathrm{DS(ON)}}}{I_{\mathrm{DS(ON,Ballistic)}}} = \frac{T}{2-T} = \frac{1-R}{1+R}. \tag{9}$$

Finally, the ratio of λ_0 over l_0 can be obtained from (7). The ratio is then used for calculation of BE since it can be written as in (8) and (9). The simplicity of this temperature-dependent extraction method lies in (7) and (9), bearing experimental BE_{sat} value without complex calculations and measurement of CV in nanoscale 3-D devices. The intuitive graphical explanation of the extracted channel backscattering coefficient R and transmission coefficient T are depicted in Fig. 1.

IV. Results and Discussion

The devices were analyzed under different temperatures at every 20 K interval from 170–390 K. Contact properties such as contact resistivity and sheet resistance were acquired from transmission length model (TLM) pattern that was simultaneously fabricated along with the devices. In order to extract various temperature-dependent parameters needed for the extraction of BE, I_D–V_G, and I_D–V_D graphs were acquired for each temperature with Keysight B1500A semiconductor device parameter analyzer and low-temperature probe station equipped with a liquid nitrogen source and a vacuum chamber.

A. Temperature-Dependent Current and Threshold Voltage

Figs. 3(a) and (b) and 4(a) show the temperature-dependent $I-V$ graphs measured from one of the AM n-Ge nanowire transistors with length of 50 nm, width of 40 nm, and height of 10 nm. Similarly, measurements were done on other lengths ranging from 40 to 100 nm to analyze the length dependence.

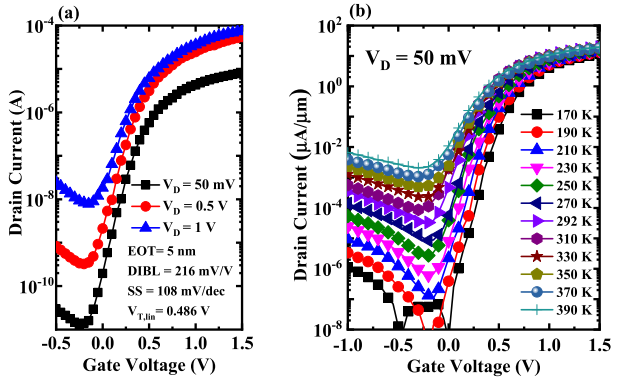

Fig. 3. (a) Transfer (I_D–V_G) curve. (b) Temperature-dependent transfer curve at low field (V_D = 50 mV) of AM nGe nanowire transistor with length 50 nm, width 40 nm, and height 10 nm (EOT = 5 nm).

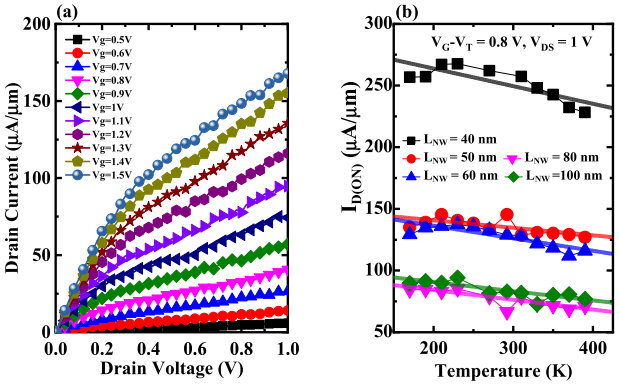

Fig. 4. (a) Output characteristic curve (I_D–V_D) of AM nGe nanowire transistors with length 50 nm, width 40 nm, and height 10 nm (EOT = 5 nm). (b) Linear-fit temperature dependent on-current [$I_{D(ON)}$] for extraction of α.

The ON-currents [$I_{DS(ON)}$], which were extracted at same gate overdrive voltage of $V_G - V_{T,lin} = 0.8$ V and $V_D = 1$ V, is shown in Fig. 4(b). $I_{DS(ON)}$ is seen to decreases with the increase of temperature and the slopes were linearly fit to extract α. Threshold voltages at both low (V_{Tlin}, $V_{DS} = 50$ mV) and high fields (V_{Tsat}, $V_{DS} = 1$ V) were extracted for each temperature, and DIBL could be calculated as well [Fig. 5(a)]. The slope of V_{Tsat} shown in Fig. 5(a) represents η as defined in (5). $\alpha = -5.555 \times 10^{-4}$ K^{-1} and $\eta = -0.00166$ V/K were extracted for $L_{NW} = 50$ nm, $W_{NW} = 40$-nm device.

B. Temperature-Dependent Series Resistance

Source/drain series resistance R_{SD}, which is incorporated into (2) as its effect on precise analysis of BE, is crucial [21]. The fact that access lengths from S/D area to the channel region in our devices differ for different L_{NW} precludes us from using the conventional channel resistance method (CRM, $R_{measured}$ vs. L) since it assumes identical R_S for all L_{NW}. Therefore, the total resistance (R_{TOT}) from transfer curves was fit for S/D resistance asymptotically [Fig. 6(a)] at each temperature. At high charge density, the channel resistance approaches to negligible value while the only effective resistance remaining in the total resistance is the series resistance. R_S ($R_S = R_D = R_{SD}/2$) were fit linearly and the acquired

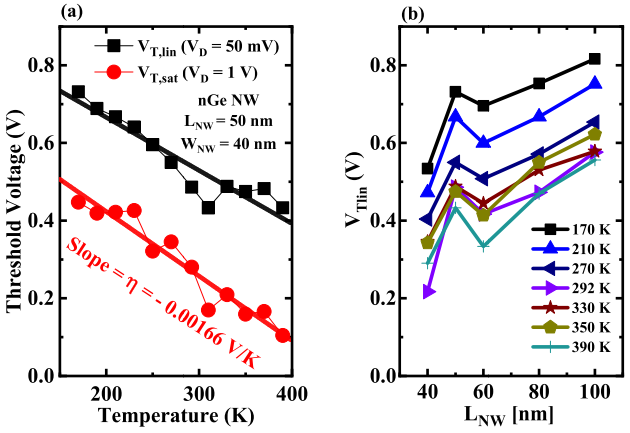

Fig. 5. (a) Temperature-dependent $V_{T,lin}$ and $V_{T,sat}$ extracted from Fig. 3(b). Higher temperature reduces the V_T, giving negative $\eta = dV_{T,sat}/dT$. (b) Temperature-dependent $V_{T,lin}$ of devices with different lengths.

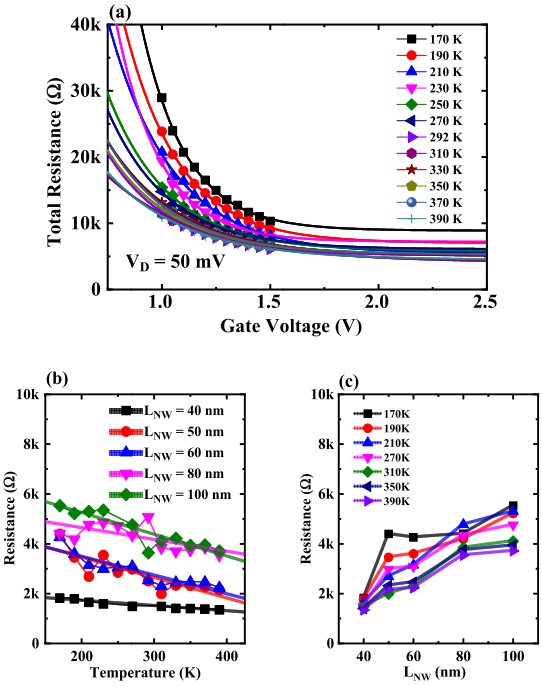

Fig. 6. (a) Extraction of parasitic series resistance (R_{SD}) using asymptotical curve fitting of $R_{TOT} \triangleright = V_D/I_D = 50$ mV/I_D). (b) Source resistance (R_{SD}/2) as a function of temperature (slope = $\beta = dR_S/dT$). R_S decreases with temperature due to decreasing R_C [Fig. 7(c)]. (c) R_S as a function of L_{NW}. Nonidentical S/D extension result in different R_S with L_{NW}.

parameter β was -8.19 Ω/K. R_S increases with L_{NW} as depicted in Fig. 6(b) and (c).

C. Temperature-Dependent Contact Properties

Sheet resistance (R_{sh}), contact resistance (R_C), and contact resistivity (ρ_C) were also studied with temperature-dependent TLM [Fig. 7(a)–(c)]. Fig. 7(a) shows that R_{sh} increases while R_C shows opposite trend with respect to the temperature. Since our Ni-nGe interface includes the typical Schottky barrier, R_C is expected to exhibit opposite trend with respect to temperature from R_{sh}. Overall, R_S shows a negative trend with

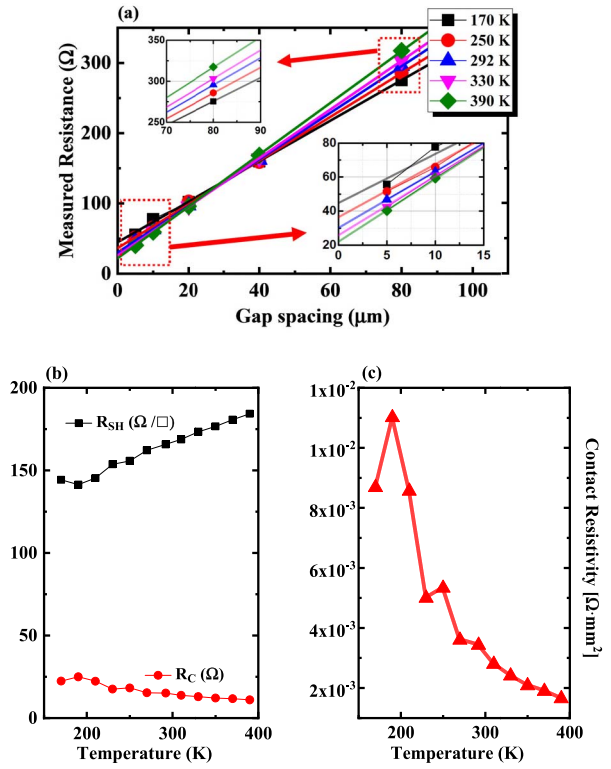

Fig. 7. (a) Temperature-dependent resistance measured from TLM pattern. Pattern width is 50 μm. (b) Temperature-dependent sheet resistance (R_{sh}) and contact resistance of Ni-nGe S/D. (c) Calculated contact resistivity (ρ_C) of Ni-nGe contact.

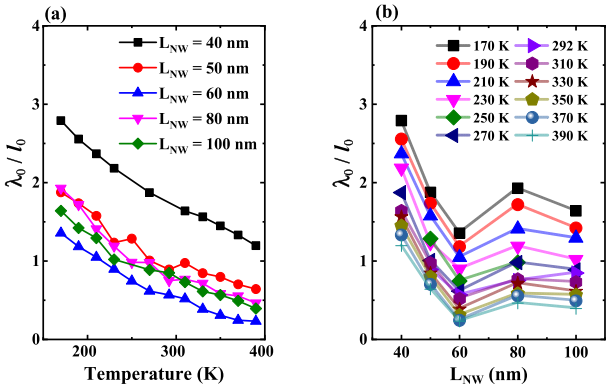

Fig. 8. Experimentally calculated λ_0/l_0 ratios as a function of (a) temperature and (b) nanowire length (L_{NW}). λ_0/l_0 ratio decreases with increase in temperature or L_{NW}.

temperature, which coincides with extracted contact resistivity (ρ_C) shown in Fig. 7(c), which suggests that device's parasitic series resistance is still in fact influenced by the inherent Fermi-level-pinning-caused Schottky barrier present at Ni-nGe interface in recessed S/D regions.

D. Extracted Ballistic Efficiency

Finally, λ_0/l_0 ratio, R and BE were extracted as a function of temperature and L_{NW} (Figs. 8–10) using (7) and (8). BE ranges from 0.10 to 0.58 within the whole range of device dimensions (L_{NW}) and temperatures. The maximum

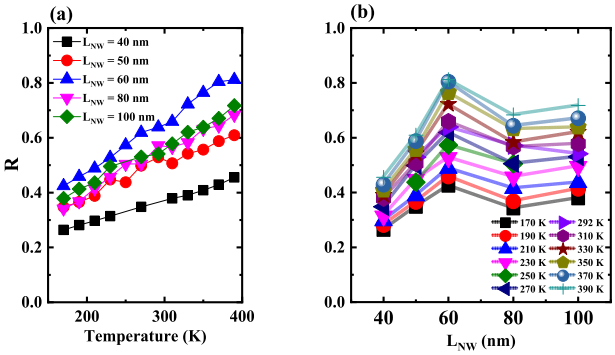

Fig. 9. Extracted channel backscattering coefficient [$R = 1/(1 + \lambda_0/l_0)$ as a function of (a) temperature and (b) nanowire length (L_{NW}). With extracted R, $BE_{sat} = (1 - R)/(1 + R) = T/(2 - T)$ can be extracted.

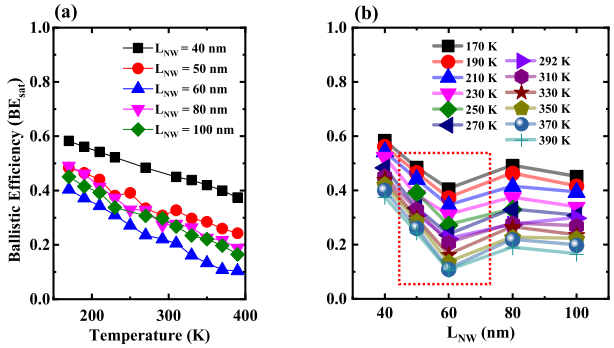

Fig. 10. (a) Temperature-dependent saturation ballistic efficiency (BE_{sat}) extracted using λ_0/l_0 ratio in Fig. 8(a) and (b). (b) L_{NW} dependence of BE_{sat}. Although transition region is visible (red dotted box), all devices with L_{NW} of 40 nm exhibit higher BE_{sat} than those with L_{NW} of 80 or 100 nm.

BE of 0.582 was extracted from $L_{NW} = 40$ nm at 170 K. At room temperature (292 K), BE values were found to be 0.22–0.47 depending on the device dimension (L_{NW}). Similar to prior reports on ballistic transport of silicon NWTs, transition region at which the carriers enter higher ballistic transport regime from drift-diffusion dominant transport ($L_{NW} >$ 100 nm) can be found in our results as well [Fig. 10(b)] [18]. It is plausible to expect BE to monotonically increase as L_{NW} scales down; however, there exists a region where λ_0/l_0 ratio (and thus BE) deviates from such trend. It can be understood to be due to competing factors between ballistic transport and typically large parasitic R_{SD} of nanowires [21]. It might seem agreeable from (1) and (2) that overestimation of R_{SD} would lead to higher BE. However, (6) suggests that higher R_{SD} lowers λ_0/l_0 ratio (noting all α, β, and η are negative) and, therefore, lowers the BE [22].

It is clearly seen from Fig. 10(b) that as channel length is scaled down to 40 nm, BE increases again exiting the transition region and the device reaches the highest ballisticity of 47% at room temperature. Note that (1)–(9) elaborated in Section III do not perfectly include all the possible complex temperature-dependent factors and mechanisms that could disturb the ballistic carrier transport in these nGe NWTs, requiring more extensive investigation. Although the whole problem is quite complex, the main goal of this work has been achieved to *experimentally* investigate ballisticity of

TABLE I
BENCHMARK ON REPORTED BALLISTIC PARAMETERS OF VARIOUS CHANNEL MATERIALS AND STRUCTURES

Reference	Device	L_{CH} [nm]	BE_{sat}	Extraction Method
M.-J. Chen et al., IEDM 2002 [17]	n-Si bulk MOSFET	75 ~ 180	0.29 ~ 0.50	Temperature (233 ~ 348 K)
Y. Tian et al., IEDM 2007 [15]	n-Si GAA nanowire	130	0.31	Temperature (approx.220 ~ 320 K)
K.-W. Ang et al., SSE 2007 [20]	(SiC S/D strained) n-Si SOI MOSFET	(approx.) 70 ~ 300	(approx.) 0.38 ~ 0.50	Temperature (298 ~ 433 K)
R. Wang et al., IEDM 2008 [18]	n-Si GAA Nanowire	34 ~ 84	0.45 ~ 0.65	Temperature
V. Barral et al., TED 2009 [40]	n-Si FDSOI MOSFET	30 ~ 10000	0 ~ 0.49	Capacitance & I_D
A. Majumdar et. al., TED 2014 [30]	n-Si ETSOI	25 ~ 50	0.58 ~ 0.70	Virtual Source Model
S. Chuang et al., Nano letters 2013 [24]	n-InAs nanowire	60	0.8	Calculation of conductance
W. Guo et al., IEDM 2014 [28]	n-Ge FinFET	14 ~ 40	(approx.) 0.45 ~ 0.85	Monte Carlo Simulation
R. Cheng et al., EDL 2017 [27]	n-Ge Planar	50 ~ 100	0.40 ~ 0.62	Temperature
This work	**n-Ge Nanowire**	**40 ~ 100**	**0.37 ~ 0.58** (L_{CH} = 40 nm, 390 ~ 170 K) **0.22 ~ 0.47** (292 K)	Temperature (170 ~ 390 K)

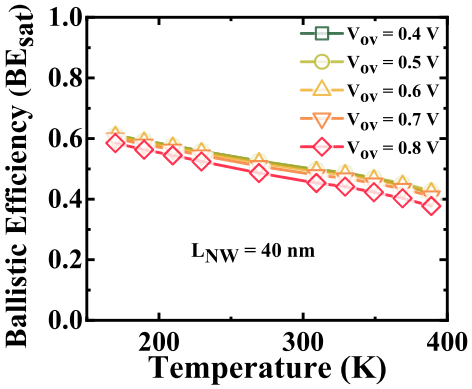

Fig. 11. BE of L_{NW} = 40-nm device extracted from various over-drive voltages ($V_{OV} = V_G - V_{T,lin}$). Although on-currents suffer more from nonideal effects at higher V_G, ballisticity show negligible fluctuation.

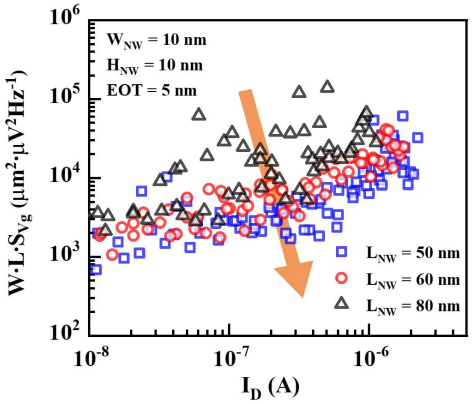

Fig. 12. Input gate noise ($S_{Vg} = S_{Id}/g_m^2$) normalized by channel area ($W_{NW} \cdot L_{NW}$). Decreasing 1/f noise with L_{NW} implies less mobility fluctuation due to high BE [31], [32].

high-mobility, non-Si nano-devices, specifically Germanium nMOS nanowire devices. The extracted BE (0.47) of Ge NMOS nanowire device with a channel length of 40-nm coincides with the Monte Carlo simulation results on Ge nFinFET, which showed approximately 0.46 [28].

The effect of temperature on BE can be also observed in Fig. 10. The higher temperature degrades the ballisticity, lowering BE down to 0.10–0.37 (depending on L_{NW}, 390 K) which is significantly lower than at 292 K (0.22–0.47). It can be interpreted that higher temperature causes more severe reflection at the source–end of the channel causing a higher portion of carriers to be backscattered. Such trend suggests that the self-heating effect of suspended nanowire devices could deteriorate the ideal ballistic transport in our devices. Since our devices using similar fabrication processes were confirmed to exhibit significant self-heating [36], the effect of increased temperature due to self-heating should be already embedded in the extracted BE results. In addition, pulsed I–V extraction method can be further utilized to exclude the self-heating effect on BE [27]. The self-heating is expected to be more prominent at lower temperature due to enhanced ON-current implying that the maximum BE extracted at 170 K could be even higher if self-heating was not present during the extraction process. Further studies on self-heating's effect on BE could be very insightful in understanding the carrier transport in nanoscale devices.

Nonideal effects that could be embedded into the current are not only limited to self-heating effects. In using this method, as seen from the flow of equations, one of the most important parameters is I_{ON} since the key step is to calculate the percentage difference in the current at different temperatures, α. As seen from (1) and (2), drain current and channel charge start from basic and simple parameters such as C_{ox}, threshold voltage, series resistance, and device dimension. Secondary nonideal effects such as: 1) enhanced current due to DIBL and its dependence on various voltage sources (V_D or V_G), device dimensions, or temperatures; 2) effects of trapping; 3) floating body effects; and 4) modulation of the Schottky barriers at contacts are not included. These could either enhance or degrade the I_{ON}. Although addressing all possible temperature-dependent secondary effects and embedding them into equations would result in more precise results, it is very challenging to do so considering the difficulties in separating

each factor from overall measured data. To study the effect of possible nonidealities at high V_G, I_{ON} was extracted from various over-drive voltages ($V_{ov} = V_G - V_{Tlin}$) and BE was extracted as seen in Fig. 11. Although it is plausible to expect that I_{ON} extracted from higher V_G would suffer from nonideal effects more severely than those extracted from lower V_G, the overall BE fluctuated negligibly. I_{ON} was reduced to half as V_{OV} was also reduced from 0.8 to 0.4 V but BE changed only by 2.6% point. This reveals that large fluctuation in I_{ON} due to nonideal effects (more prominent in higher V_G) plays minor role in estimation of BE as long as the devices operate with consistently similar nonideal effects throughout the temperature sweep range at given device dimension and voltage conditions since it does not directly use the raw data but takes the temperature-dependent slope values for calculation. Still, there is more room to improve the accuracy of this method by incorporating temperature-dependent nonidealities into the equations.

E. Low-Frequency Noise Analysis

The hint of ballistic transport in nanoscale high-mobility devices can be indirectly studied through several other methods such as thermal imaging [37] or low-frequency noise measurements [38]. Recently, our nGe NWTs with EOT = 2 nm, L_{NW} = 40–80 nm were suggested to exhibit high electron ballisticity through low-frequency noise studies [39]. Through similar measurements of low-frequency noise on devices analyzed in this paper (EOT = 5 nm), it is once again confirmed that low-frequency noise decreases as L_{NW} down scales. Fig. 12 shows the input gate noise normalized by the channel area of the devices defined as width × length of the nanowire devices. Such opposite trend from diffusive long channel devices implies that the electrons are transported with higher BE at shorter L_{NW} and therefore experience lower mobility fluctuation and noise [38], [39].

V. Conclusion

Experimental extraction of ballisticity on high-performance AM Ge NMOS nanowire devices through temperature-dependent analysis was conducted. No *CV* measurements or estimations of mobility from these nanowires were needed throughout the process. The acquired BE was 0.10–0.58 for different nanowire dimensions and temperatures (L_{NW} = 40–100 nm, 170–390 K). The extracted ballisticity at room temperature (292 K) was determined to be 0.47 for devices with L_{NW} = 40 nm. The existence of anomalous BE transition region was observed near L_{NW} = 50–60 nm, similar to the data reported for Si nanowire devices at similar channel lengths. Finally, the low-frequency noise analysis further confirmed that our devices are, in fact, operated in quasi-ballistic regime with high ballisticity as we benchmark most of representative BE works on aggressively scaled Si, Ge, and III–V nanodevices shown in Table I.

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