Mobility Fluctuation-Induced Low-Frequency Noise in Ultrascaled Ge Nanowire nMOSFETs With Near-Ballistic Transport

Wangran Wu, Heng Wu, Weifeng Sun, *Senior Member, IEEE*, Mengwei Si, Nathan Conrad, Yi Zhao, *Senior Member, IEEE*, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— In this paper, we study the low-frequency noise in the Ge nanowire (NW) nMOSFETs with sub-100-nm channel length. The low-frequency noise with 1/*f* characteristics is proved to origin from the carriers' mobility fluctuation. The dependences of low-frequency noise on NW geometry, channel length, equivalent oxide thickness (EOT), and channel doping concentration are examined by evaluating the Hooge parameters. It is shown that the low-frequency noise declines when the channel length of Ge NW nMOSFETs scales down, which is attributed to the electrons' near ballistic transport. The electrons suffer more scatterings in the channels beneath the side walls of NWs or in the highly doped channels. The gate-oxide optimization is strongly demanded with the scaling down of EOT. Ultrascaled Ge NW nMOSFETs promise the enhancement of on-state performance and the suppression of low-frequency noise simultaneously.**

***Index Terms*— Ge nanowire (NW) nMOSFETs, Hooge parameter, low-frequency noise, mobility fluctuation, scattering.**

I. Introduction

AS WE continuously scale down the MOSFETs' gate length following Moore's law, several new technologies are introduced in main stream Si CMOS, such as the high-*k*/metal gate, multigate structure, as well as the high-mobility channel in order to maintain the enhancement in the device performance [1]–[5]. Ge has high and balanced electron and hole mobility [6], [7] with demonstrated n- and p-MOSFETs on Ge substrate [8], [9]. Also, Ge has silicon compatible process, relatively stable performance, and capability for strain engineering [9]–[12]. Thus, Ge may have the best chance among the high mobility materials in the aggressively scaled technology nodes. Advanced gate stacks with scaled equivalent oxide thickness (EOT) and superior MOS interfaces are still needed to develop Ge CMOS manufacturing technology with high reliability, because the formation of sufficiently good high-*k*/Ge interface in Ge MOSFETs is a critical issue [11], [13]. However, when the device's dimensions scale down to sub-100 nm, it is increasingly hard to directly measure the interface and oxide properties. The C–V method cannot be applied in these devices because the intrinsic capacitance is too small and the parallel capacitance is prominent. The substrate is needed during the conventional charge pumping test and it cannot be applied to gate-all-around nanowire (NW) FETs. Therefore, the low-frequency noise can be used as an alternate probe to characterize and optimize these advanced devices because the noise measurement can be done regardless of the small gate capacitance or the float-body channel [14]–[16]. Meanwhile, the low-frequency noise has also serious impacts in scaled nonvolatile memories and logic circuits [17], [18]. Several groups have studied low-frequency noise of long-channel Ge MOSFETs [19], [20]. Recently, we have reported the first observation of random telegraph noise (RTN) in Ge NW nMOSFETs [21]. However, quantitative analysis on the origin of low-frequency noise and associate scattering process is still lack.

On the other hand, understanding the low-frequency noise of Ge MOSFETs is also important for low-noise radio frequency/analog applications. In the real practice, accurate low-frequency noise model is very relevant for CMOS circuit designers and the semiconductor manufacturers in order to reduce the noise figure in Ge CMOS circuits. The comprehensive study on the mechanisms of low-frequency noise in ultrascaled Ge MOSFETs is demanded.

This paper extends the previous conference reports [21] by comprehensively studying the low-frequency noise in the Ge NW nMOSFETs with sub-100-nm-channel length (L_{ch}).

Manuscript received February 21, 2018; revised March 12, 2018; accepted March 23, 2018. Date of publication April 13, 2018; date of current version May 21, 2018. This work was supported in part by SRC and Lam Research, in part by the National Natural Science Foundation of China under Grant 61674030, Grant BK20160691, and Grant BK20150627, and in part by the Fundamental Research Funds for the Central Universities. The review of this paper was arranged by Editor Z. Celik-Butler. *(Corresponding author: Peide D. Ye.)*

W. Wu was with the Birck Nanotechnology Center, School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA. He is now with the National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China (e-mail: wwr620@126.com).

H. Wu, M. Si, N. Conrad, and P. D. Ye are with the Birck Nanotechnology Center, School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

W. Sun is with the National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China (e-mail: swffrog@seu.edu.cn).

Y. Zhao is with the Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2822813

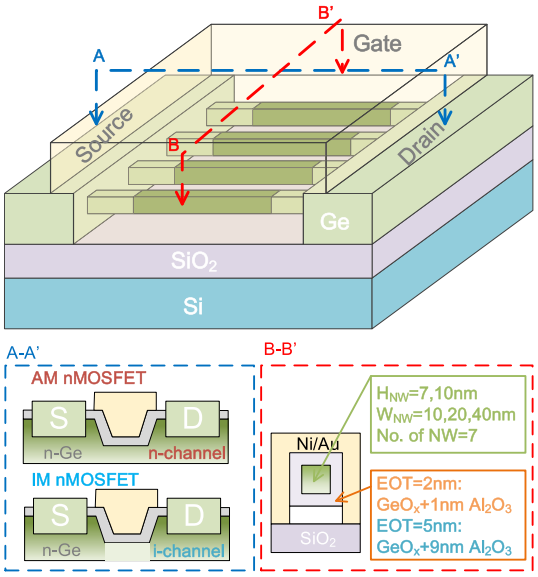

Fig. 1. Schematic of the Ge NW nMOSFETs. The AM and IM nMOSFETs with various key geometry parameters were prepared.

We have made a conclusive inquiry of the origin of the low-frequency noise. The low-frequency noise and associate Hooge parameters are studied in devices with various NW geometries, channel lengths, channel doping concentration, and EOTs. The electrons' scattering process in the channel is also examined.

II. Experiment

The Ge NW nMOSFETs were fabricated on the Ge-on-insulator substrate with 180-nm Ge(100) layer and 400-nm SiO_2 on Si(100) handle wafer from Soitec. The fabrication process is the same as reported in [5]. The recessed source/drain (S/D) method via a SF_6-based inductively coupled-plasma dry etching is adopted to optimize the contact by reducing the Schottky barrier width and realize both heavily doped S/D and lightly doped channel. Fig. 1 illustrates the schematic of the Ge NW nMOSFETs. Both accumulation-mode (AM) nMOSFETs and inversion-mode (IM) nMOSFETs with various key geometry parameters were fabricated (Fig. 1). Devices with NW width (W_{NW}) of 10, 20, and 40 nm, NW height (H_{NW}) of 7 and 10 nm, L_{ch} of 40, 50, 60, and 80 nm, as well as EOT of 2 and 5 nm are prepared and used for the low-frequency noise characteristics. The 1-nm Al_2O_3 was first deposited by atomic layer deposition and then a postdeposition oxidation was performed in pure O_2 ambient to grow GeO_x passivating layer, resulting in the EOT of 2 nm. Then devices with 5-nm EOT were prepared by depositing additional 8-nm Al_2O_3. Each device has seven NWs. The channel width (W_{ch}) is calculated from $W_{ch} = (2 \cdot H_{NW} + W_{NW}) \times$ (number of wires). AM NW nMOSFETs with n-doped channel were measured unless otherwise specified. The IM nMOSFETs with undoped channel was also examined to evaluate the impact of channel doping. All the low-frequency noise measurement of drain current (I_d) was done by the Keysight B1500A with B1530A waveform generator/fast measurement unit under room temperature at a drain voltage (V_{ds}) of 50 mV.

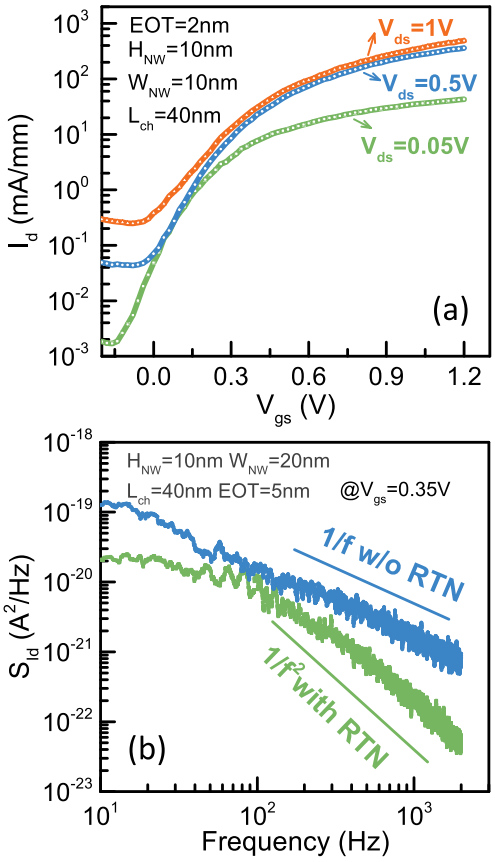

Fig. 2. (a) Transfer characteristics of a 40-nm L_{ch} NW nMOSFET. (b) S_{Id} of two devices, having the same device dimensions, with and without RTNs at V_{gs} of 0.35 V.

III. Results and Discussion

Fig. 2(a) shows the transfer characteristics of an NW nMOSFET with 40-nm L_{ch} and 2-nm EOT. Subthreshold slope of 98 mV/dec is achieved at V_{ds} of 0.05 V, and the amount of drain-induced barrier lowering is 106 mV/V, indicating that the device was well fabricated. Because the electrons in the inversion channel populate very close to the interface, the electrons' transportation is largely affected by the scattering centers (traps, dopants, surface roughness, etc.) near the interface. The low-frequency noise may origin from the carrier number fluctuation or the carrier mobility fluctuation in the conventional theory. According to Hooge's carrier mobility fluctuation model [22], [23], the drain current noise can be given by the empirical formula

$$\frac{S_{Id}}{I_d^2} = \frac{\alpha_H}{f N_{inv}} = \frac{q\alpha_H}{f W_{ch} L_{ch} Q_{inv}} \tag{1}$$

where S_{Id} is the power spectrum density (PSD) of I_d, f is the frequency, q is the elementary charge, α_H is the Hooge parameter, N_{inv} is the number of conducting carriers in the inversion layer, and Q_{inv} is the charge density of inversion layer. Using $I_d = W_{ch}/L_{ch} \cdot \mu_{eff} \cdot V_{ds} \cdot Q_{inv}$ and (1), we have the following relationship:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H \mu_{eff} V_{ds}}{f L_{ch}^2 I_d} \tag{2}$$

where μ_{eff} is the carriers' effective mobility.

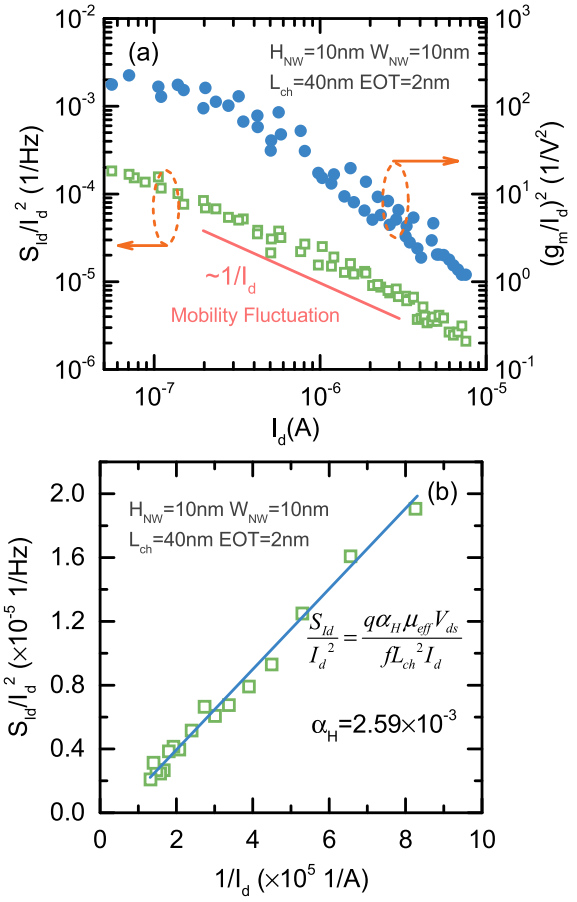

Fig. 3. (a) Normalized S_{Id} and $(g_m/I_d)^2$ versus I_d of devices with $1/f$ low-frequency noise at 10 Hz. (b) S_{Id}/I_d^2 versus $1/I_d$ at 10 Hz and the linear fit. The Hooge parameter is 2.59×10^{-3}.

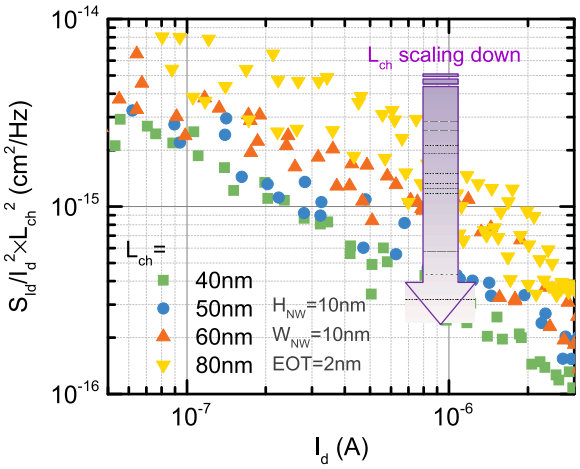

Fig. 4. S_{Id}/I_d^2 normalized by L_{ch}^2 versus I_d of devices with different values of L_{ch} at 10 Hz. Normalized S_{Id}/I_d^2 decreases with the scaling down of L_{ch}.

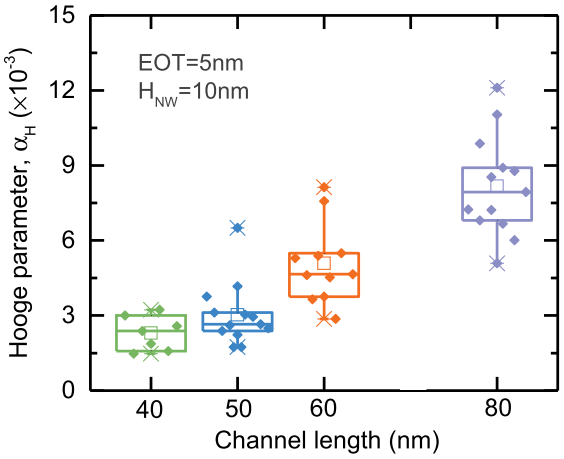

Fig. 5. Box plot of the Hooge parameters of devices with a channel length from 40 to 80 nm. The Hooge parameter decreases with the scaling down of L_{ch}.

Typical $1/f$ characteristics are observed in the devices without RTN signal at a given gate voltage (V_{gs}), while the devices with RTN signal have the Lorentzian spectrum with $1/f^2$ characteristics [Fig. 2(b)]. The low-frequency noise results obtained in devices without RTN are used in the following discussion. The PSD of I_d is noisy when the frequency is high, while the PSD of I_d in low-frequency region is better [Fig. 2(b)]. The PSD of I_d at a frequency of 10 Hz is obtained. Fig. 3(a) shows the normalized S_{Id} (S_{Id}/I_d^2) and $(g_m/I_d)^2$ as a function of I_d at 10 Hz, where g_m is the gate transconductance. The clear $1/I_d$ dependence of S_{Id}/I_d^2 agrees well with the mobility fluctuation model in (2). The S_{Id}/I_d^2 is not linearly correlated with $(g_m/I_d)^2$. In the carrier number fluctuation model with correlated mobility fluctuations (CNF-CMF) [23], [24], S_{Id}/I_d^2 starts from the plateau in the weak inversion region and then decrease as I_d^{-2} in the strong inversion region. When the correlated mobility fluctuations are taken into consideration, a significant deviation from the I_d^{-2} dependence could be observed in the strong inversion region. The results in Fig. 3(a) have covered the region from weak inversion to strong inversion. Neither the plateau at weak inversion nor the deviation at strong inversion is observed as described by the CNF-CMF model. The low-frequency noise in the Ge NW nMOSFETs follows the Hooge mobility fluctuation model. According to (2), α_H can be obtained by linear fit with the knowledge of effective mobility, as shown in Fig. 3(b). We have measured the effective mobility of planar Ge MOSFETs with the same gate-stack but larger gate area [25]. Also, according to the transconductance of devices with various EOTs and devices' dimensions[5], the variation of effective mobility is very small compared with that of the slope of the $S_{Id}/I_d^2 \sim 1/I_d$ curves. The constant electron mobility of 200 $cm^{-2}/V{\cdot}s$ is assumed to extract the Hooge parameters in this paper, since it is extremely hard to precisely extract the carriers' effective mobility in the ultrascaled Ge NW MOSFETs. The Hooge parameter of Ge NW MOSFETs used in this paper is higher compared with the state-of-art Si device and similar to the value of high-k HfO_2/Si devices. The typical value of the Hooge parameter in Si device ranging from 10^{-3} to 10^{-6}, depending on the substrate quality, device structure, and fabrication process. The suppression of the Hooge parameter and low-frequency noise in Ge NW nMOSFETs is highly desired.

In the frame of the conventional carrier mobility fluctuation model, S_{Id}/I_d^2 increases with the scaling down of channel

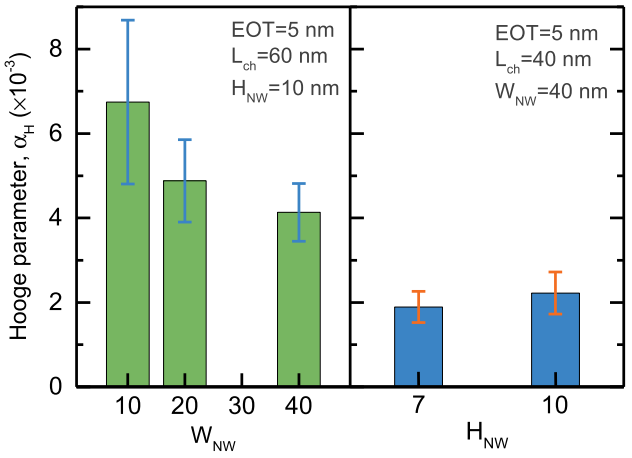

Fig. 6. Hooge parameters in Ge NW nMOSFETs with (a) W_{NW} of 10, 20, 30, and 40 nm and (b) H_{NW} of 7 and 10 nm.

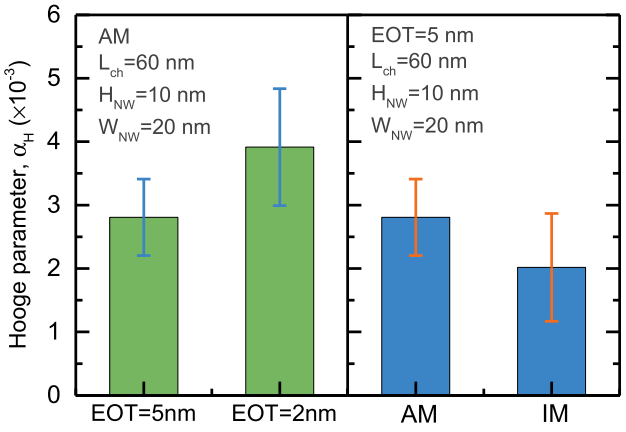

Fig. 7. Hooge parameters in Ge NW nMOSFETs with (a) EOT of 5 and 2 nm and (b) AM Ge NW nMOSFETs and IM Ge NW nMOSFETs.

length and S_{Id}/I_d^2 normalized by L_{ch}^2 shall be independent of channel length as shown in (2). However, the normalized $S_{Id}/I_d^2 \times L_{ch}^2$ in the Ge NW nMOSFETs decreases when L_{ch} scales down from 80 to 40 nm (Fig. 4). The Hooge parameters are extracted by linear fit in order to give a deep insight on anomalous decline of low-frequency noise in ultrascaled Ge NW nMOSFETs. Fig. 5 shows the box plot of Hooge parameters as a function of the channel length. It is clearly shown that the Hooge parameter decreases with the scaling down of channel length. The Hooge parameter reflects the mobility fluctuations induced by the electrons' scattering processes during the transportation in the channel. Assuming the phonon scattering, Coulomb scattering and surface-roughness scattering are independent; the mobility fluctuation noise induced by each scattering process can be represented by (2), separately. The Hooge parameters reflect the strength of each scattering. Thus, we can have [22]

$$\alpha_H = \sum_j \frac{\mu_{\text{eff}}^2}{\mu_j^2} \alpha_{H,j} \tag{3}$$

where j represents specific scattering process, including phonon scattering, Coulomb scattering, and surface-roughness scattering. The reduced Hooge parameter indicates the attenuation in scattering when the electrons traveling through the short channel. The Hooge parameter of devices with 40-nm L_{ch} is only one third of those with 80-nm L_{ch}. This is attributed to the near-ballistic transport of electrons because of the electrons' long mean-free path in Ge. The decreasing low-frequency noise in shorter channel devices was also observed in highly scaled InGaAs MOSFETs [26]. The Hooge parameter results provide a direct evidence for the near ballistic transport in ultrascaled Ge nMOSFETs. It also shows that the low-frequency noise declines when the L_{ch} decreases in the highly scaled Ge nMOSFETs, which is a unique advantage for the application in the scaled low-noise integrated circuit.

Since the Hooge parameter could represent the carriers' scattering process, it is sensitive to the substrate quality, gate-stack properties and substrate doping concentration. The dry etching process used in the formation of Ge NW causes damage in the NW side walls. Thus, electrons beneath the side wall suffer severer scatterings. Fig. 6 illustrates the Hooge parameter dependence on NW width and height. The Hooge parameter decreases when the W_{NW} increases from 10 to 40 nm because of the smaller proportion of NW side wall contributed to the whole channel. The Hooge parameters are smaller in devices with H_{NW} of 7 nm because of the shorter dry etching time and approaching volume inversion condition for Ge. Furthermore, assuming that the electrons are evenly distributed in the inversion layer under the side wall and top wall, the Hooge parameter of electrons beneath the side wall is about two times larger than that of the top wall according to the experimental results in Fig. 6(a). The severe scatterings of electrons caused by the poor side wall quality not only elevate the low-frequency noise, but also suppresse the electrons' mobility. Thus, the dry etching process and side wall quality shall be carefully optimized.

Fig. 7(a) shows that the Hooge parameters in devices with smaller EOT are higher. The severer scatterings in devices with 2-nm EOT may arise from the degradation in GeO_x interfacial layer because the Al_2O_3 capping layer is too thin. Since the Coulomb scattering is also an important source of mobility scattering, the Hooge parameters are smaller in IM NW nMOSFETs because the relative lower channel doping induces less Coulomb scattering [Fig. 7(b)]. The low-frequency noise results provide a direct insight on the electrons' scattering process in ultrascaled Ge NW devices.

IV. Conclusion

We have comprehensively studied low-frequency noise in highly scaled Ge NW nMOSFETs with various NW geometries, channel lengths, EOTs, and channel doping. The low-frequency noise arises from the carrier mobility fluctuation and it declines in devices with shorter channels. This anomalous dependence is ascribed to the electrons' near ballistic transport. The electrons' scattering process is examined by evaluating the Hooge parameters. The NW side wall and gate-oxide optimization is required for the scattering suppression and mobility enhancement. In the perspective of device performance, the ultrascaled Ge NW nMOSFETs promise the enhancement of ON-state performance and the suppression of low-frequency noise simultaneously.

ACKNOWLEDGMENT

This work was carried out at Purdue University, West Lafayette, IN, USA, and Southeast University, Nanjing, China.

REFERENCES

[1] H. Iwai, "Roadmap for 22 nm and beyond (Invited Paper)," *Microelectron. Eng.*, vol. 86, pp. 1520–1528, Jul./Sep. 2009, doi: 10.1016/j.mee.2009.03.129.

[2] S. Takagi *et al.*, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 21–39, Jan. 2008, doi: 10.1109/TED.2007.911034.

[3] J. A. Del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[4] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310–316, Nov. 2011, doi: 10.1038/nature10676.

[5] H. Wu, W. Wu, M. Si, and P. D. Ye, "First demonstration of Ge nanowire CMOS circuits: Lowest SS of 64 mV/dec, highest gmax of 1057 μS/μm in Ge nFETs and highest maximum voltage gain of 54 V/V in Ge CMOS inverters," in *IEDM Tech. Dig.*, Dec. 2015, pp. 2.1.1–2.1.4, doi: 10.1109/IEDM.2015.7409610.

[6] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature*, vol. 479, pp. 324–328, Nov. 2011, doi: 10.1038/nature10678.

[7] A. Toriumi, "Recent progress of germanium MOSFETs," in *Proc. IMFEDK*, May 2012, pp. 1–2, doi: 10.1109/IMFEDK.2012.6218562.

[8] H. Wu, N. Conrad, W. Luo, and P. D. Ye, "First experimental demonstration of Ge CMOS circuits," in *IEDM Tech. Dig.*, Dec. 2014, pp. 9.3.1–9.3.4, doi: 10.1109/IEDM.2014.7047016.

[9] R. Zhang, P.-C. Huang, J.-C. Lin, M. Takenaka, and S. Takagi, "Physical mechanism determining Ge p- and n-MOSFETs mobility in high Ns region and mobility improvement by atomically flat GeOx/Ge interfaces," in *IEDM Tech. Dig.*, Dec. 2012, pp. 16.1.1–16.1.4, doi: 10.1109/IEDM.2012.6479051.

[10] S. Gupta *et al.*, "GeSn technology: Extending the Ge electronics roadmap," in *IEDM Tech. Dig.*, Dec. 2011, pp. 16.6.1–16.6.4, doi: 10.1109/IEDM.2011.6131568.

[11] C. H. Lee, T. Nishimura, T. Tabata, K. Nagashio, K. Kita, and A. Toriumi, "Variation of surface roughness on Ge substrate by cleaning in deionized water and its influence on electrical properties in Ge metal–oxide–semiconductor field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 51, p. 104203, Oct. 2012, doi: 10.1143/JJAP.51.104203.

[12] W. Wu, X. Li, J. Sun, R. Zhang, Y. Shi, and Y. Zhao, "Comparison of different scattering mechanisms in the Ge (111), (110), and (100) inversion layers of nMOSFETs with Si nMOSFETs under high normal electric fields," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1136–1142, Apr. 2015, doi: 10.1109/TED.2015.2398733.

[13] R. Zhang, N. Taoka, P.-C. Huang, M. Takenaka, and S. Takagi, "1-nm-thick EOT high mobility Ge n- and p-MOSFETs with ultrathin GeOx/Ge MOS interfaces fabricated by plasma post oxidation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 28.3.1–28.3.4, doi: 10.1109/IEDM.2011.6131630.

[14] T. Grasser *et al.*, "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424235.

[15] E. R. Hsieh *et al.*, "The experimental demonstration of the BTI-induced breakdown path in 28nm high-k metal gate technology CMOS devices," in *Proc. Symp. VLSI Technol.*, Jun. 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894389.

[16] T. Nagumo, K. Takeuchi, T. Hase, and Y. Hayashi, "Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps," in *IEDM Tech. Dig.*, Dec. 2010, pp. 28.3.1–28.3.4, doi: 10.1109/IEDM.2010.5703437.

[17] M.-L. Fan, V. P.-H. Hu, Y.-N. Chen, P. Su, and C.-T. Chuang, "Analysis of single-trap-induced random telegraph noise on FinFET devices, 6T SRAM cell, and logic circuits," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2227–2234, Aug. 2012, doi: 10.1109/TED.2012.2200686.

[18] J. Zou *et al.*, "Deep understanding of AC RTN in MuGFETs through new characterization method and impacts on logic circuits," in *Proc. Symp. VLSI Technol.*, Jun. 2013, pp. T186–T187.

[19] E. Simoen, B. Kaczer, M. Toledano-Luque, and C. Claeys, "Random telegraph noise: from a device physicist's dream to a designer's nightmare," *Microelectron. Technol. Devices*, vol. 39, no. 1, pp. 3–15, 2011, doi: 10.1149/1.3615171.

[20] E. Simoen *et al.*, "Low-frequency noise characterization of strained germanium pMOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3132–3139, Sep. 2011, doi: 10.1109/TED.2011.2160679.

[21] W. Wu, H. Wu, M. Si, N. Conrad, Y. Zhao, and P. D. Ye, "RTN and low frequency noise on ultra-scaled near-ballistic Ge nanowire nMOSFETs," in *Proc. Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573421.

[22] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994, doi: 10.1109/16.333808.

[23] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, 1991, doi: 10.1002/pssa.2211240225.

[24] G. Ghibaudo, O. Roux-dit-Buisson, and J. Brini, "Impact of scaling down on low frequency noise in silicon MOS transistors," *Phys. Status Solidi A*, vol. 132, no. 2, pp. 501–507, Aug. 1992, doi: 10.1002/pssa.2211320226.

[25] W. Wu, H. Wu, J. Zhang, M. Si, Y. Zhao, and P. D. Ye, "Carrier mobility enhancement by applying back-gate bias in Ge-on-insulator MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 176–179, Feb. 2018, doi: 10.1109/LED.2017.2787023.

[26] M. Si *et al.*, "Low-frequency noise and random telegraph noise on near-ballistic III-V MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3508–3515, Nov. 2015, doi: 10.1109/TED.2015.2433921.

Authors' photographs and biographies not available at the time of publication.