Interfacial Layer Engineering in Sub-5-nm HZO: Enabling Low-Temperature Process, Low-Voltage Operation, and High Robustness

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***Abstract*— For low-voltage reliable operation of ferroelectric devices, the scaling of $Hf_{1-x}Zr_xO_2$ (HZO) thickness (t_{HZO}) is important. Despite the importance of scaling, ferroelectricity degradation and increased process thermal budget hinder progress. In this work, we propose the use of an interfacial layer (IL) to mitigate these scaling issues and validate its effectiveness in thin t_{HZO}. Our findings demonstrate that IL can activate ferroelectricity below the critical temperature of ferroelectric HZO. Moreover, we report 2× polarization improvement, reduced operation voltage from 1.5 to 1.2 V, and substantially improved endurance with >10 years of reliability, all based on experimental results. We believe this systematic work offers a simple yet efficient route toward HZO scaling in ferroelectric devices.**

***Index Terms*— Back-end-of-the-line (BEOL) compatible process, ferroelectricity improvement, $Hf_{1-x}Zr_xO_2$ thickness (t_{HZO}) scaling, HZO reliability, interfacial layer (IL) engineering, operation voltage scaling.**

I. Introduction

THE standard CMOS technology, with transistors as efficient switches, has been the workhorse of today's high-performance systems. However, with the evolving computing workloads and the demand for ubiquitous intelligence, high energy efficiency has come to the forefront. To meet this challenge, the need to rethink the entire computing stack has become apparent. To achieve this goal, there is a need to incorporate more functionalities into a single device, beyond what a CMOS transistor can provide. In light of this, we consider ferroelectric devices, which offer energy-efficient building blocks for boosting performance on challenging workloads [1], [2], [3], [4], [5], [6].

Recent research on ferroelectric devices has focused on scaling the thickness (t_{HZO}) of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) [7], [8], [9], [10], [11], [12]. Achieving lower operation voltage as well as more robustness is the largest gain of scaled t_{HZO}. However, scaling t_{HZO} is hindered by increased process temperature and degraded ferroelectricity because of the increased amorphous structure of HZO [9], [13]. It has been reported that an annealing temperature higher than 450 °C is required to secure sufficient ferroelectricity when t_{HZO} is reduced below 5.6 nm [9] and 4.8 nm [10]. However, that is not favorable for back-end-of-the-line (BEOL) process which has a thermal budget limit of 400 °C [14]. Two different approaches have been tried to improve ferroelectricity in scaled HZO structures. In [11], different top-electrode (TE) and bottom-electrode (BE) combinations were investigated to minimize the depolarization field. Depending on the electrode materials, the formation of nonferroelectric layers (i.e., dead layers) at the ferroelectric/metal interface changes. Although high remnant polarization (P_r) was obtained at $T_{PMA} = 400$ °C, the negative coercive field (E_c) increasing to ~ -1.75 MV/cm at t_{HZO} of 5 nm or less offsets the advantages of scaling t_{HZO}. Additionally, there is a lack of reliability studies in electrode material design. Another approach adopted is the HZO epitaxy high-quality HZO can be obtained. Results show a high P_r even at $t_{HZO} = 4.5$ nm [12]. However, it requires a high temperature of 800 °C for the HZO epitaxy process. Considering ferroelectric devices are mostly to be fabricated in BEOL, such a high process temperature is not a feasible solution. This work proposes an approach to improving P_r and securing low operation voltage even at T_{PMA} below 400 °C.

Previous research has investigated using an interfacial layer (IL) to increase the ferroelectric properties of thicker HZO films (around 10 nm). Table I provides information on the IL materials and annealing processes used in these studies. The IL enhances ferroelectricity by increasing

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TABLE I
SUMMARY OF MATERIALS AND PROCESS INFORMATION OF THE PREVIOUS IL RELATED WORK

IL Material	Ref.	t_{HZO}	t_{IL}	Annealing Conditions	
				Temperature	Time
HfON	[15]	8~25 nm	2~200 nm	500°C	30 sec
HfO_2	[16]	10 nm	1~20 nm	600°C	10 sec
	[17]	10 nm	1 nm	300~400°C	60 sec
	[18]	10 nm	1 nm	350°C	60 sec
	[19]	15 nm	3 nm	450°C	30 sec
TiO_2	[17]	10 nm	1 nm	300~400°C	60 sec
	[20]	10 nm	2~3 nm	500°C	300 sec
	[21]	10 nm	0~5 nm	400°C	-
SiN_x	[22]	4.5 nm	1.5 nm (850°C)	500°C	30 sec
ZrO_2	[17]	10 nm	1 nm	300~400°C	60 sec
	[23]	10 nm	0.5~5.0 nm	600°C	60 sec
	[24]	10 nm	2 nm	400~700°C	60 sec
	[25]	9.5 nm	2 nm	900°C	60 sec
	[26]	10 and 25 nm	1~2 nm	550°C	60 sec
	[27]	12 nm	1.5 nm	550°C	Unknown
	[28]	10 nm	2 nm	500~800°C	30 sec
	[29]	10 nm	2 and 10 nm	300~600°C	60 sec
AlON	[33]	9.5 nm	1.2 nm	800°C	Unknown
Al_2O_3	[23]	10 nm	2 nm	600°C	60 sec
	[25]	9.5 nm	2 nm	900°C	60 sec
	[33]	9.5 nm	1.2 nm	800°C	Unknown
	[34]	10 nm	0.5~3 nm	600~900°C	Unknown
	[35]	10~40 nm	1 nm	500°C	30 sec
	[36]	7 nm	~1 nm	450~600°C	30 sec
Ta_2O_5	[37]	10 nm	1~5 nm	600°C	Unknown

the ferroelectric orthorhombic-phase (*o*-phase) content of the HZO film. One reason for this is claimed as using polycrystalline nature of as-deposited IL, such as ZrO_2 [17], [23], [24], [25], [26], [27], [28], [29], [30]. X-ray diffraction (XRD) data of the ZrO_2 layer before the annealing process was provided to support the claim. Here, the analyzed ZrO_2 layers were 14 nm [23] and 10 nm [29]. However, thicker ZrO_2 (>6 nm) is known to have polycrystallinity during atomic layer deposition (ALD) [31], [32], while the ILs used in the studies listed in Table I were mostly 1–2 nm, and thus too thin to be polycrystalline. Our position on this will be discussed in detail in the last few paragraphs of Section II. The other reason for enhanced ferroelectricity with IL is the large stress introduced onto the HZO layer, which increases *o*-phase fraction [13], [38]. These benefits of using IL naturally motivated us to invoke the idea of adopting it for t_{HZO} scaling.

We propose a simple but effective approach, harnessing an ultrathin IL to alleviate challenges associated with scaling t_{HZO}. Specifically, we investigate the effect of IL materials in sub-5-nm HZO films, covering various perspectives, such as crystallization temperature, ferroelectricity, low-voltage operation capability, and reliability characteristics. Our findings demonstrate that incorporating an IL can induce a higher *o*-phase content in the HZO layer, reduced operation voltage, improved ferroelectricity, and enhanced retention performance.

TABLE II
DEVICE STRUCTURAL AND PROCESS TEMPERATURE CONDITIONS

t_{HZO}	1-nm IL (BE side)	T_{PMA} (Time: 60 sec)
4.5 nm	Without IL HfO_2 ZrO_2 Al_2O_3	300, 350, 400, and 500°C
9.5 nm	Without IL HfO_2 ZrO_2 Al_2O_3	300, 350, 400, and 500°C

Importantly, we observe that the use of an IL can reduce the critical temperature of HZO crystallization. This finding supports the use of IL for scaling t_{HZO}.

II. DEVICE FABRICATION AND ITS FERROELECTRICITY

In this work, ferroelectric capacitors were fabricated to understand the behaviors of the different ferroelectric stacks. A 10-nm-thick TiN BE, an IL, an HZO layer, and a 10-nm-thick TiN TE were deposited subsequently using thermal ALD at 200 °C on the p^+-type Si substrate. Table II contains information about the device structures and annealing conditions that were employed. Note, a 1-nm IL was intentionally deposited between the BE and HZO layer, followed by in situ deposition of 4.5- or 9.5-nm HZO layers, which improves ferroelectricity and endurance [43]. Previous studies have shown that the optimum IL thicknesses to improve P_r with HfO_2 [16], ZrO_2 [23], and Al_2O_3 [34] ILs are 1, 2, and 0.5 nm, respectively. In this work, we aimed to investigate the effects of IL over the HZO layer while keeping the thickness as thin as possible but within a reliable and controllable range. Therefore, we chose a 1 nm of IL thickness to encompass the optimum thicknesses of each IL material. Rapid-thermal annealing (RTA) as a post-metal annealing (PMA) was performed after the TE deposition. Al deposition and lift-off were conducted for capacitor patterning (area: 3600 μm^2). Note, we additionally attempted PMA annealing at $T_{PMA} = 275$ and 300 °C for 60 s and 2 h, but none of the devices showed ferroelectricity.

The electric field (E) is a key metric used to compare the performance of different structures. It is calculated by dividing the applied voltage (V_{apply}) by the total dielectric thickness (averaged E). However, the actual electric field applied to the ferroelectric layer can vary due to factors such as the permittivity of the IL, the quality of the metal-dielectric interface, and the quality of the HZO layer. Even though we do not plot the measurement result with the actual electric field on HZO, we calculated the voltage drop across the HZO (V_{HZO}) by extracting the dielectric constant, charge density, total capacitance, and interfacial capacitance. We then expressed V_{HZO} as a percentage of V_{apply} ($=V_{HZO}/V_{apply} \times 100$). Overall, higher T_{PMA} and the use of an IL increase the percentage of V_{HZO}. However, the differences in the percentage of V_{HZO} between cases with IL and without IL become more significant at thinner t_{HZO}. Among the different ILs, ZrO_2 IL shows the highest percentage of V_{HZO}, due to its high permittivity and improved interface and HZO quality.

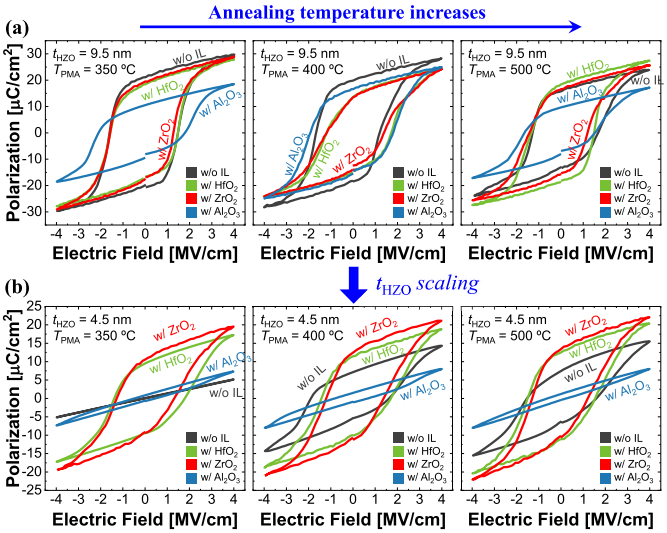

Fig. 1. *P–E* loops of the devices having (a) 9.5- and (b) 4.5-nm t_{HZO}.

Importantly, at 4.5-nm t_{HZO} and low T_{PMA}, ZrO_2 IL indicates 70.5% and 81.4% of V_{apply} dropped on HZO at 350 °C and 400 °C T_{PMA}, respectively (56.0% and 65.7% for HfO_2 IL, and 50.3% and 69.8% for Al_2O_3 IL, respectively).

Fig. 1(a) and (b) depict the measured polarization (P)-electric field (E) loops for 9.5- and 4.5-nm t_{HZO} films annealed at T_{PMA} of 350 °C, 400 °C, and 500 °C, respectively. The period taken in P–E measurement was fixed to 1 kHz. Wake-up pulses of 5000 cycles with ±4 MV/cm amplitude were applied before all measurements. The $2P_r$ ($=P_r^+ - P_r^-$) and the E_c [$=0.5\cdot(E_c^+ - E_c^-)$] extracted from Fig. 1 are plotted in Fig. 2(a) and (b), respectively. For $t_{HZO} = 9.5$ nm, using an IL did not improve $2P_r$ for the 350 °C and 400 °C annealed cases. However, for scaled t_{HZO}, using an IL plays a significant role not only in boosting P_r, but also in reducing E_c (see Fig. 2). Importantly, the IL decreases the critical temperature for HZO crystallization at scaled t_{HZO}. With HfO_2 and ZrO_2 ILs, 350 °C for T_{PMA} is sufficient to activate ferroelectricity, whereas the device without an IL exhibits no ferroelectricity. At $T_{PMA} = 400$ °C, 1.7× and 1.9× of P_r improvements are obtained with HfO_2 and ZrO_2 ILs, respectively, compared to devices without an IL. The usage of HfO_2 and ZrO_2 IL also improves $2P_r$ compared to HZO without an IL at the same voltage condition. At scaled t_{HZO}, the Al_2O_3 IL is not helpful at all in improving ferroelectricity. The devices with E_c values of 9.5-nm t_{HZO} without IL, with HfO_2 IL, and with ZrO_2 IL, exhibit similar behavior. However, the insertion of Al_2O_3 IL results in a high E_c at 9.5-nm t_{HZO} due to its low dielectric constant and a small E_c at 4.5-nm t_{HZO} due to weak ferroelectricity. ZrO_2 IL provides the most consistent E_c values across different t_{HZO} and T_{PMA} conditions. The relationship between E_c and low-voltage operation capability is discussed in Section III.

Transmission electron microscopy (TEM) images of the devices without IL and with ZrO_2 IL ($T_{PMA} = 350$ °C) are shown in Fig. 3(a) and (b), respectively. The HZO layer has an amorphous structure without IL. However, the HZO layer becomes crystallized with 1-nm ZrO_2 IL at the same t_{HZO}. It is

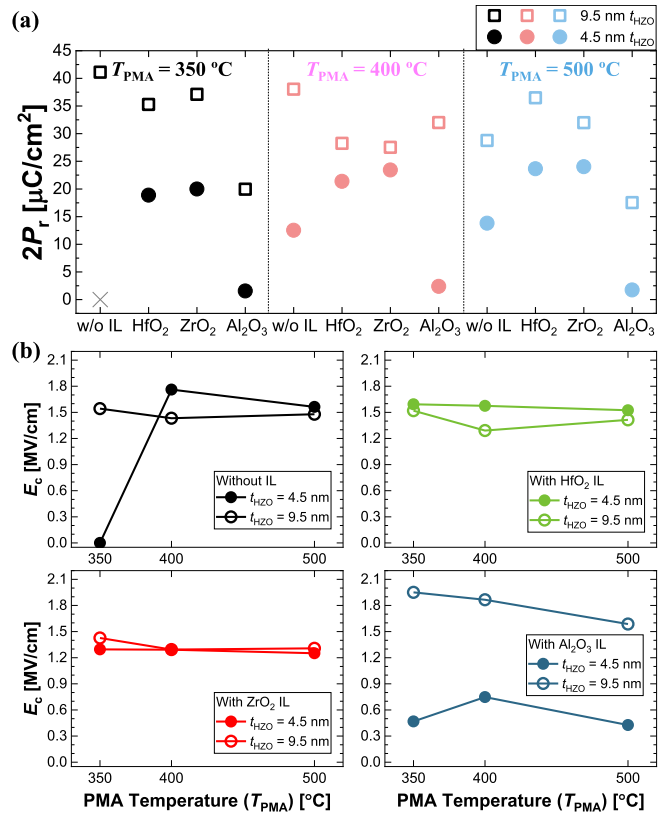

Fig. 2. Extracted figure-of-merits for 9.5- and 4.5-nm t_{HZO} devices. (a) $2P_r$ and (b) E_c plots.

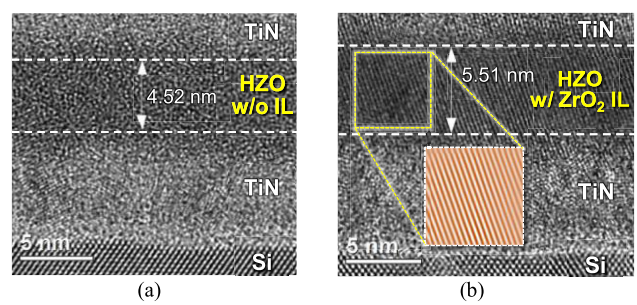

Fig. 3. TEM images for 4.5-nm t_{HZO} devices (a) without IL and (b) with 1-nm ZrO_2 IL. T_{PMA} was 350 °C for both.

worth noting that the ZrO_2 IL might not be intermixed into the HZO layer during or after the PMA process, but rather secured as a bilayer structure. Previous works have demonstrated the maintained bilayer of the 10-nm HZO/2-nm ZrO_2 IL structure even after annealing at 400 °C–700 °C for 60 s [24], [26]. Since our T_{PMA} conditions are between 300 °C and 500 °C, the deposited IL would be preserved after the PMA process. Therefore, our device dielectric stacks cannot be considered as having 5.5-nm $Hf_{1-x}Zr_xO_2$ ($x > 0.5$) without IL.

The use of an IL has resulted in improved crystallinity and higher o-phase content in the HZO layer, which in turn has led to an increase in P_r. To figure out the cause of this improvement, we conducted grazing incidence XRD (GI-XRD) analysis and capacitance measurement. The GI-XRD data for the 400 °C annealed devices is presented in Fig. 4(a). The X-ray intensity contains signals from multiple phases due to XRD

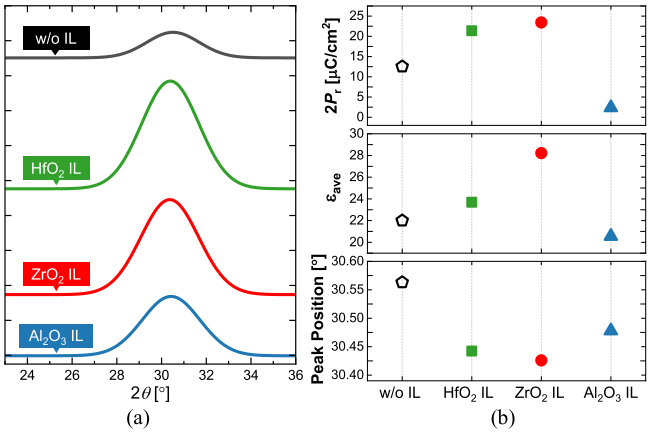

Fig. 4. Devices at T_{PMA} = 400 °C with 4.5-nm t_{HZO}. (a) GI-XRD data and (b) $2P_r$, ε_{ave}, and peak position of 2θ from GI-XRD results.

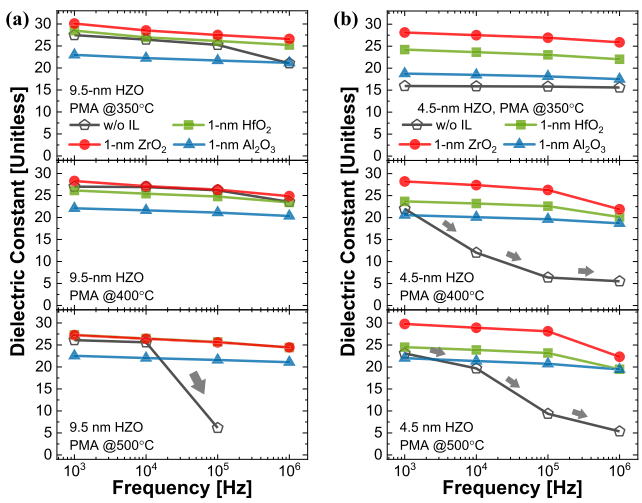

Fig. 5. Average dielectric constant (ε_{ave}) calculated from the C–E measurement ($\varepsilon_{ave} = C/\text{Area} \times (t_{HZO} + t_{IL})$) of (a) t_{HZO} = 9.5 nm and (b) t_{HZO} = 4.5 nm devices.

peak broadening. We estimated the phase concentration based on the position of the intensity peak. The significant degrees of the HZO phases are 28.5° ($m(-111)$), 30.4° ($o(111)$), 30.8° ($t(011)$), and 31.6° ($m(111)$). Fig. 4(b) indicates $2P_r$, the average dielectric constant (ε_{ave}), and XRD peak position for the 400 °C annealed devices with 4.5-nm t_{HZO}. The HZO without IL exhibits the smallest X-ray signal and the peak is located far from 30.4° ($o(111)$), indicating low phase concentration. In contrast, the devices with HfO_2 and ZrO_2 IL show strong intensities with peaks located close to 30.4°, representing a high ferroelectric o-phase concentration. Additionally, >10 μC/cm^2 of $2P_r$ is obtained with HfO_2 and ZrO_2 IL, indicating the introduction and stabilization of high o-phase concentration in thin HZO. The HZO with Al_2O_3 IL also exhibits a comparable X-ray intensity with HfO_2 and ZrO_2 IL, but has almost zero $2P_r$, indicating large nonferroelectric phases on HZO.

Capacitance (C)–E measurement was performed for all devices at different frequencies (f) of 1 kHz, 10 kHz, 100 kHz, and 1 MHz. Fig. 5(a) and (b) show calculated ε_{ave} from C–E measurement, which were extracted at the cross point of the butterfly curves in forward- and reverse-direction sweeps. Here, RC delay was observed, which suggests that the evaluated ε_{ave} may be lower than the actual value. However, the observed trends between devices and our conclusions would not be affected. The dielectric constants of the o- and tetragonal (t)-phase are known to be ~30 and 32–40, respectively [40]. The ε_{ave} of amorphous HZO is 16 (the value is from the 4.5-nm t_{HZO} without IL at 350 °C T_{PMA}). When both ε_{ave} and $2P_r$ are considered, it can be assumed that the devices with the ε_{ave} of ~16 and weak ferroelectricity contain a significant portion of amorphous or nonferroelectric phases in HZO. This finding is consistent with the cases of Al_2O_3 IL. Thereby, the introduction of Al_2O_3 is believed to create phases in HZO, as indicated by the intensity in GI-XRD data, but most cannot stabilize to o-phase.

In the following paragraphs, we will discuss the factors contributing to improved ferroelectricity and reduced crystallization temperature of ferroelectric HZO. Achieving a high o-phase concentration is significant for improving P_r. Additionally, surface energy plays a crucial role in stabilizing the crystalline phases in the thin HZO structure [41]. To transform nonferroelectric t-phase to ferroelectric o-phase, sufficient stress is required after amorphous HZO is converted to crystalline HZO in the t-phase [42]. The different coefficients of thermal expansion (CTEs) between HZO and abutting layers, as well as the lattice mismatch-induced strain, are the primary factors affecting the transformation of the dominant HZO crystalline phase from t- to o-phase.

During the annealing process, HfO_2, ZrO_2, and Al_2O_3 can trigger the formation of t-phase in HZO due to their inherent material properties. HfO_2 and ZrO_2 have low surface energies owing to their thin thickness and small grain sizes [7], [43]. The thermodynamic model with Gibbs free energy can explain these properties [41]. A previous study reported that deposited Al_2O_3 underneath HZO can effectively reduce grain size and hinder grain growth of HZO [35]. Therefore, all HfO_2, ZrO_2, and Al_2O_3 IL can induce t-phase during the PMA process, as verified by our GI-XRD data in Fig. 4. The t-phase can later transform to o-phase via in-plane tensile stress that originates from the different CTEs of stacked materials [13], [38], and lattice mismatch strain induced by crystallized phases [20].

It is important to note that there are properties distinguishing HfO_2 and ZrO_2 IL from Al_2O_3 IL. Both HfO_2 and ZrO_2 have similar crystallization temperatures [32], [44], crystal structures, and phase formation energies with HZO [45]. This suggests that HfO_2 and ZrO_2 IL can mutually affect HZO during the crystallization process, leading to their crystallization during annealing. This can be observed in the TEM image in Fig. 3(b), which shows a vertically grown HZO layer with no interface with the crystallized ZrO_2 IL. The resulting decrease in surface-to-volume-ratio (due to the increased volume of the crystallized layer) can lower the kinetic barrier for the transition from amorphous to crystalline and t- to o-phase transition [44], [46]. As a result, high o-phase concentrations are observed for both HfO_2 and ZrO_2 IL cases in our measurement data. However, Al_2O_3 IL has a higher crystallization temperature (900 °C) than HfO_2 and ZrO_2 IL, making it less effective in inducing o-phase in HZO under the given T_{PMA} conditions [47].

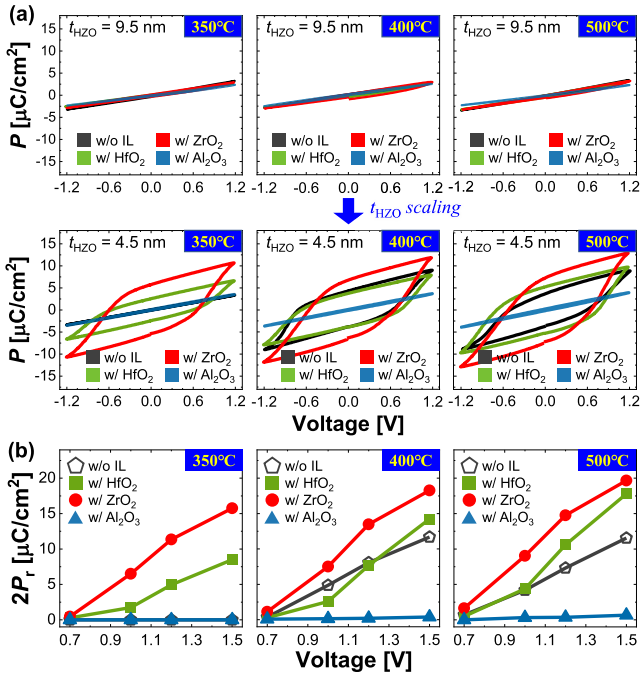

Fig. 6. Low-voltage operation characteristics. (a) P–V loops when the voltage sweep range is fixed to ±1.2 V at t_{HZO} = 9.5 nm (upper) and 4.5 nm (lower). (b) $2P_r$ versus operation voltage of 4.5-nm HZO devices.

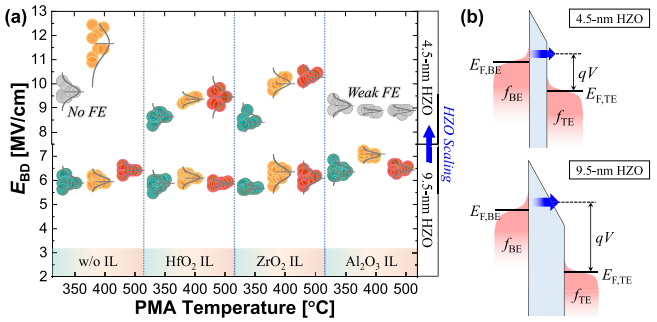

Fig. 7. Dielectric breakdown characteristics. (a) E_{BD} distribution plots. (b) Energy-band diagram when t_{HZO} is thin (upper) and thick (lower).

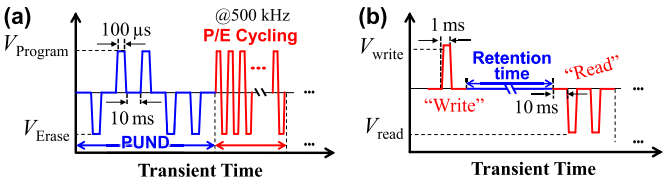

Fig. 8. Pulsing schemes for reliability test of (a) endurance and (b) retention.

To lower the crystallization temperature of ferroelectric HZO, it is important to choose IL which has a low crystallization temperature and structural similarity to HZO. Furthermore, an IL with a low CTE can also help lower the crystallization temperature of HZO [48], [49], [50]. As previously reported, using a low CTE electrode generates stress in HZO during the crystallization [48], [49], [50]. The CTE values of TiN, HZO, HfO_2, ZrO_2, and Al_2O_3 are 7–9.4 × 10^{-6} K^{-1} [20], [51], 5 × 10^{-5} K^{-1} [52], 3.8 × 10^{-6}, 7–10.3 × 10^{-6}, and 8.1–8.4 × 10^{-6} K^{-1} [20], [53], respectively. Compared to ZrO_2 and Al_2O_3, HfO_2 has a large difference in CTE with HZO, which can induce greater stress in HZO. This enables HfO_2 IL to have superior ferroelectric performance, despite its slightly higher crystallization temperature compared to ZrO_2 or HZO [44].

III. Low-Voltage Operation Capability

Along with dimension scaling, reducing operation voltage is important to decrease power consumption. Fig. 6(a) shows the P–V loops of devices with 9.5- and 4.5-nm t_{HZO} at ±1.2 V voltage sweep, and Fig. 6(b) shows the $2P_r$ observed for the 4.5-nm t_{HZO} devices at different operating voltages. At ±1.2 V, the 9.5-nm HZO samples do not exhibit $2P_r$ above 10 $\mu C/cm^2$. However, the 4.5-nm HZO devices achieve high $2P_r$ due to the relatively unchanged E_c (= coercive voltage (V_c) divided by the t_{HZO}) between 9.5 and 4.5 nm of t_{HZO} [see Fig. 2(b)]. With the usage of ZrO_2 IL, HZO shows superior low-voltage operation performance, inducing a small E_c and the largest $2P_r$ at scaled t_{HZO}. The required operation voltage for the ZrO_2 IL case to obtain $2P_r$ > 10 $\mu C/cm^2$ is 1.2 V, which is 0.3 V lower than without IL. At 1.2-V operation, P_r increases 1.67 times with ZrO_2 IL (T_{PMA} = 400 °C) compared to one without IL. For 500 °C annealed devices, 1.5 and 2.0 times of $2P_r$ improvement are observed by using HfO_2 and ZrO_2 IL, respectively. The improved low-voltage operation capability is confirmed based on our claim that the IL (HfO_2 and ZrO_2) promotes the large o-phase content onto the scaled HZO and enhances the quality of HZO and interfaces.

IV. Reliability Characteristics

In previous sections, we have confirmed that the use of IL leads to increased P_r, lower operational voltage, and reduced process temperature. In this section, we will examine the impact of T_{PMA} and IL on various reliability performances of the device, including hard breakdown electric field (E_{BD}), endurance, and retention. To investigate dielectric strength, a time-zero dielectric breakdown test was conducted. Fig. 7(a) displays the distribution of the E_{BD} and Fig. 7(b) shows the energy band diagram across TE-HZO-BE. In endurance and retention measurement, the positive-up-negative-down (PUND) method was used. The pulsing schemes used in endurance and retention measurement are shown in Fig. 8(a) and (b). For the endurance measurement, the program/erase (P/E) bipolar cycling was employed at high-stress condition of ±4 MV/cm.

Fig. 9(a) and (b) show the polarization switching amounts (P^*) for the 9.5- and 4.5-nm of t_{HZO} samples, respectively. The endurance performance of the device is closely related to its E_{BD}, which is proportional to the observed endurance performance (see Fig. 9). The E_{BD} and endurance performance are improved by reducing t_{HZO}. Note that RC delay and the high endurance cycling frequency can cause the electric field across HZO to be less than the applied field. This is due to device capacitances and measurement equipment limitations. While the absolute number of breakdown cycles may differ, the performance trend across the devices remains consistent.

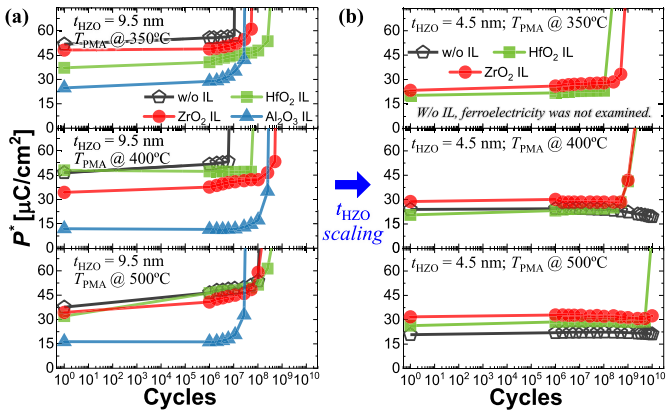

Fig. 9. Endurance performances with 4 MV/cm of bipolar cycling for the devices with (a) 9.5- and (b) 4.5-nm t_{HZO}.

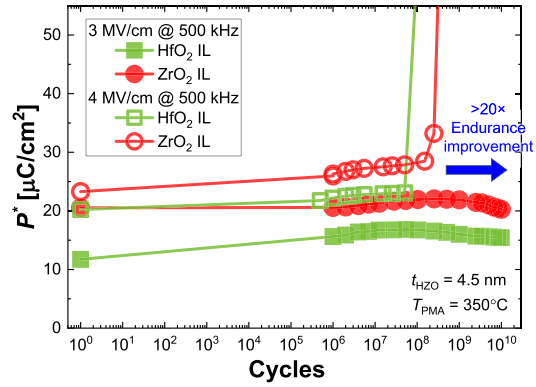

Fig. 10. Endurance improvement when the electric field of P/E bipolar cycle is reduced from ±4 to ±3 MV/cm. Measured devices have 4.5-nm t_{HZO} with HfO_2 and ZrO_2 IL.

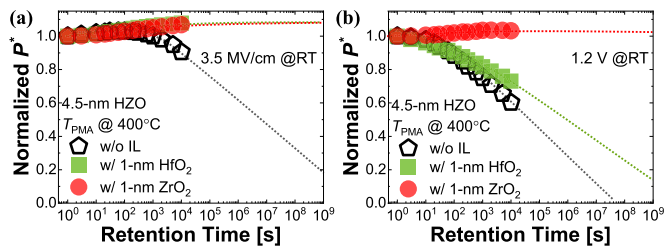

Fig. 11. Retention characteristics with 4.5-nm t_{HZO} without IL, with a ZrO_2 IL, and with a HfO_2 IL. (a) Fixed write/read pulses to 3.5 MV/cm and (b) 1.2 V.

Several reasons for improved dielectric robustness have been reported, including reduced electron injection energy (see Fig. 7(b)) [9], suppressed bulk charge trapping [54], and the formation of a relatively thick t-phase IL at the metal/HZO interface with decreased t_{HZO} [55].

The study yielded three significant findings with regard to endurance improvement: 1) scaling t_{HZO} and increasing T_{PMA} can improve endurance; 2) scaled t_{HZO} without IL shows similar or better endurance compared to devices with IL; and 3) ZrO_2 IL provides better endurance over HfO_2 IL. Generally, the endurance performance of HZO degrades as T_{PMA} increases due to increased defects and monoclinic-phase concentration [7], [40], [56]. However, the degradation of endurance is only observed from 600 °C of T_{PMA} [40], [57], [58]. In this work, no degradation in endurance was observed since T_{PMA} was intentionally limited to 500 °C to ensure BEOL process applicability.

In thin t_{HZO} devices, endurance can be improved by increasing T_{PMA} from 350 °C to 500 °C. However, decreasing T_{PMA} is a preferred method in the BEOL process. The only downside of using HfO_2 and ZrO_2 IL is relatively inferior endurance compared to devices without IL. To improve endurance, reducing input electric field and decreasing operation voltage are considered a reasonable direction for low-power-operation-aimed technology nodes. Importantly, the devices have sufficient $2P_r$, enabling further electric field reduction. Fig. 10 shows endurance measurement results measured at ±3 MV/cm of P/E cycles on devices with 4.5-nm t_{HZO} and with HfO_2 and ZrO_2 IL (T_{PMA} = 350 °C), which had the poorest endurance in Fig. 9(b). The devices show over 20 times improvement in endurance compared to the input with 4 MV/cm. The devices also do not experience breakdown until 10^{10} cycles. This implies that degraded device endurance, the only obstacle of using IL, can be overcome by scaling the operation electric field or voltage.

To compare the effect of IL on retention, we performed retention measurements on 4.5-nm t_{HZO} devices annealed at 400 °C that are available to compare cases without and with IL, and within the reasonable range for the BEOL process [14]. The write/read pulses had an amplitude of ±3.5 MV/cm (see Fig. 11(a)) and 1.2 V (see Fig. 11(b)). Each cycle included a positive-up (write) and two negative-down pulses (read and preset the ferroelectric layer for the next write operation) (see Fig. 8(b)).

Note, the usage of HfO_2 and ZrO_2 IL remarkably improves the retention behavior by suppressing depolarization field. Moreover, with ZrO_2 IL, the programmed state can be retained for a projected 10 years at 1.2-V operation (see Fig. 11(b)).

The retention performance of the device without IL is the worst due to a high depolarization field. To understand this, interface capacitance (C_i) was calculated using the formula $1/C_{total} = 1/C_{HZO} + 1/C_i$. C_{total} is from the capacitance measurement, C_{HZO} is the ferroelectric capacitance of the HZO layer, and C_i is the lumped capacitor including dead layer capacitance and IL capacitance. To avoid confusion, it should be clarified that the "dead layer" refers to the nonferroelectric IL generated by electrode metal oxidation, while the intentionally deposited layer of 1-nm thickness is referred to as the "IL." The assumption is that only C_{HZO} depends on t_{HZO}. The C_i extraction process is shown in Fig. 12(a), and the calculated C_i for different T_{PMA} is indicated in Fig. 12(b). Small C_i, which is considered a major device reliability decelerating factor, induces a high field inside the IL and/or dead layer. This can be attributed to charges accumulating at the IL/dead layer boundaries, which can shield the ferroelectric polarization [59]. In particular, HZO without IL has the smallest C_i in all T_{PMA} cases, resulting in poorer retention characteristics compared to HZO with an IL. This is also consistent with the small percentage of V_{apply} on HZO without IL that we calculated in Section II. To improve device

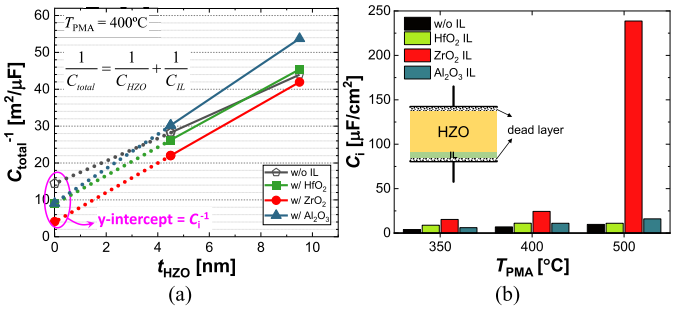

Fig. 12. Interfacial capacitance (C_i) evaluation. (a) C_{total}^{-1} versus t_{HZO} for 400 °C annealed devices. (b) Extracted C_i of all devices.

retention performance, it is suggested to use sub-5-nm t_{HZO}, reduce the operation voltage, and adopt a 1-nm-thin IL to increase C_i.

V. Conclusion

Our study proposes the use of a 1-nm IL can effectively alleviate the challenges associated with scaling t_{HZO} for use in ferroelectric devices. This is a simple but effective method that can be feasible in the BEOL process. By increasing the concentration of *o*-phase, the IL has enabled low-voltage operation with high $2P_r$, and improved retention by increasing C_i. At 4.5-nm t_{HZO}, ZrO_2 IL offers superior characteristics compared to devices without IL, including 2× larger P_r, 0.3-V lower operation voltage (reduced from 1.5 to 1.2 V), and >10 years of long retention. Importantly, the use of an IL can effectively address the increased critical temperature for ferroelectric HZO crystallization associated with t_{HZO} scaling. While devices with IL show degraded endurance at high electric field operation, their performance has improved substantially under moderate operation condition of 3 MV/cm. Overall, these findings provide a promising approach for improving the performance of ferroelectric devices in advanced technology nodes.

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