Atomically Thin Indium-Tin-Oxide Transistors Enabled by Atomic Layer Deposition

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***Abstract*— In this work, indium-tin-oxide (ITO) transistors with atomically thin channel thickness (T_{ch}) of 2.1 nm realized by atomic layer deposition (ALD) are demonstrated. A maximum ON-state current of 970 mA/mm at V_{DS} of 0.8 V and an ON/OFF ratio up to 10^7 are achieved in ITO transistor with In:Sn ratio of 9:1, channel length (L_{ch}) of 60 nm, and dielectric equivalent oxide thickness (EOT) of 2.1 nm. Comparison between devices with different In:Sn ratios indicates a significant reduction of electron transport resulting from more Sn concentrations in ITO. The impact of back-end-of-line (BEOL) compatible low-temperature annealing is also investigated. An enhancement-mode operation with minimum subthreshold slope (SS) of 80 mV/dec and maximum field-effect mobility (μ_{FE}) of 28 $cm^2/V{\cdot}s$ is achieved after O_2 annealing. Besides, bias instability measurement shows the negative threshold voltage (V_T) shift under both positive and negative gate bias stress due to donor-like interface states below the trap neutral level (TNL). The realization of large-area synthesis of atomically thin ITO films by ALD and decent electrical performance provide opportunities in future monolithic 3-D device integration with BEOL compatibility.**

***Index Terms*— Atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, bias instability, indium tin oxide, low-temperature annealing, thin-film transistor.**

I. Introduction

THIN-FILM transistors (TFTs) based on amorphous oxide semiconductors have gained continuous attention over the past decades [1]–[7]. Due to several remarkable features, such as high carrier mobility, fast response, flexible ultrathin body, high transparency, amorphous oxide semiconductors are considered as competitive channel material candidates for next-generation BEOL-compatible CMOS transistor channels for monolithic 3-D integration [8]–[13]. However, the main challenges for the application of such materials so far are controllable large-scale ultrathin film synthesis as well as reliable device performance. ITO, as a wide bandgap oxide semiconductor (3.5–4.3 eV), is known to be widely used as transparent electrodes in optoelectronics, while its semiconductor behavior has been rarely explored due to its degeneracy in the conduction band. A high electron density for typical ITO is usually around 10^{20}–$10^{21}/cm^3$, leading to unsatisfactory switching characteristics [14]–[16]. By reducing the film thickness to modulate the bandgap and adjust the carrier density in oxide semiconductor materials as reported previously [14], [16]–[18], a functional ITO channel can be expected to meet the requirement for monolithic 3-D integration. ALD provides the unprecedented advantage to control the thickness and In:Sn ratio at the atomic accuracy compared to other physical vapor deposition (PVD) techniques.

In this article, the synthesis of ITO films with a thickness of 2.1 nm is realized by the ALD technique. High-performance ITO transistors with different In:Sn ratios, channel length (L_{ch}) down to 60 nm, and channel thickness (T_{ch}) of 2.1 nm are achieved with a maximum drain current of 970 mA/mm at a drain-to-source voltage (V_{DS}) of 0.8 V and an ON/OFF ratio up to 10^7. Comparison between ITO transistors with different Sn concentrations demonstrates that the electron transport in ALD ITO films is impeded by SnO_2, supported by density-functional-theory (DFT) simulation and modeling. The impact of BEOL-compatible low-temperature annealing in O_2 and forming gas (FG, 96% N_2/4% H_2) is also systematically studied. O_2 annealing is found to shift the threshold voltage (V_T) positively and an enhancement-mode operation with V_T of 0.33 V is observed in the ITO transistor with In:Sn of 9:1 and L_{ch} of 60 nm, which can be understood by the passivation of oxygen vacancies in the as-grown channel. In addition, bias instability measurement points out the possible existence of donor-like interface states below the trap neutral level (TNL), contributing to a negative V_T shift under stress.

II. Experimental and Computational Procedure

Fig. 1(a) illustrates the schematic of an ITO transistor. The gate-stack includes 40 nm Ni as the bottom gate, 5 nm HfO_2 as the gate dielectric, 2.1 nm ITO as the semiconducting channel, and 60 nm Ni as source/drain contacts. Fig. 1(b) presents the fabrication process flow. Fig. 1(c) shows the scanning electron

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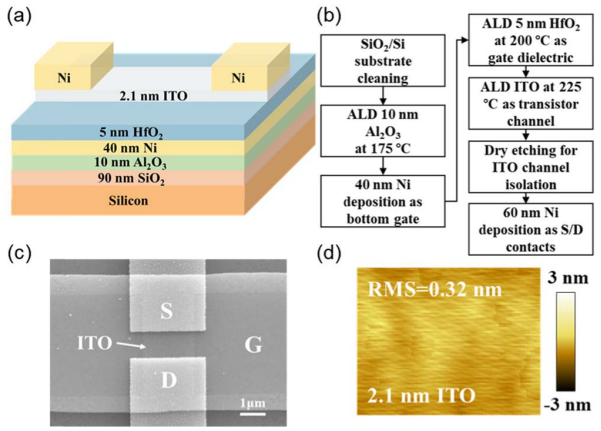


Fig. 1. (a) Schematic of the atomically thin ITO transistor with 40 nm Ni as the bottom gate. (b) Fabrication process flow of an ITO transistor. (c) SEM image of an ITO transistor with L_{ch} of 1 μm. (d) AFM measurement of the surface roughness on a 2.1 nm as-grown ITO film with In:Sn ratio of 9:1.

microscopy (SEM) image of a typical fabricated ITO transistor with L_{ch} of 1 μm.

The device fabrication process started with a standard cleaning process of p^+ Si substrate with 90 nm thermally grown SiO_2. A standard cleaning process refers to that the substrate was rinsed with toluene, acetone, and IPA in an ultrasonic cleaner and dried by nitrogen to remove possible organic particles and dirty materials. A 10 nm Al_2O_3 was deposited by ALD at 175 °C to obtain a smooth surface, using $(CH_3)_3Al$ (TMA) and H_2O as Al and O precursors. A bilayer photoresist lithography process similar to [13] was then applied for the sharp lift-off 40 nm Ni bottom gate by e-beam evaporation. A 5 nm HfO_2 was deposited by ALD at 200 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as Hf and O precursors. A 2.1 nm ITO was deposited by ALD at 225 °C with $(CH_3)_3In$ (TMIn), $[(CH_3)_2N]_4Sn$ (TDMASn), and H_2O as In, Sn and O precursors. TMIn and TDMASn precursors were heated to 60 °C to provide sufficient vapor pressure and N_2 with a flow rate of 40 sccm was used as the carrier gas. The HfO_2 and ITO were grown in two different ALD chambers but the two ALD systems are located in the same glovebox under environment control like a cluster system. This ALD process started with one cycle of SnO_2 with TDMASn and H_2O pulsed for 2 and 1 s, respectively, followed by N cycles of In_2O_3 with TMIn and H_2O pulsed for 0.625 and 0.75 s at each cycle, then repeated. N was set to 3, 6, and 9 to obtain ITO films with different In:Sn ratios. The thickness of the ALD ITO film was measured by ellipsometer (Gaertner L116A) and calibrated by transmission electron microscopy (TEM) and atomic force microscope (AFM). Fig. 1(d) shows a low surface roughness of 0.32 nm for the ITO film with In:Sn of 9:1 measured by AFM. No obvious difference of surface roughness is observed between ALD-deposited ITO films with different In:Sn ratios and before/after O_2 annealing. ITO channel isolation was done by plasma dry etching (BCl_3: 15 sccm; Ar: 60 sccm; pressure: 0.6 Pa; RF source power: 100 W; RF bias power: 50 W; time: 20 s). 60 nm Ni was deposited by e-beam evaporation as source/drain contacts, patterned by electron beam lithography with L_{ch} ranging from 60 nm to 1 μm. The fabricated devices were also annealed in O_2 and FG at 250 °C and 300 °C for 60 s to investigate the intrinsic properties of ALD ITO films.

The charge neutrality levels (CNLs) and band alignment of In_2O_3 and SnO_2 were calculated by DFT as implemented in the Vienna *ab initio* simulation package (VASP) [19], [20]. Perdew–Burke–Ernzerhof-generalized gradient approximation (GGA-PBE) functional is used for electron exchange-correlation interaction [21], [22]. The CNLs were calculated by performing Brillouin zone average using Kohn–Sham eigenenergies computed at Γ-centered Monkhorst–Pack k-points [23]

$$E_{\mathrm{CNL}} = \frac{1}{2N_k}\sum_{k\in BZ}\left[\frac{1}{N_{CB}}\sum_{i}^{N_{CB}} E_{CB_i}(k) + \frac{1}{N_{VB}}\sum_{j}^{N_{VB}} E_{VB_j}(k)\right]$$

where N_k is the number of k-points. For SnO_2 unit cell containing two formula units, two conduction bands ($N_{CB} = 2$) and four valence bands ($N_{VB} = 4$) were used; for In_2O_3 primitive cell containing eight formula units, $N_{CB} = 16$ and $N_{VB} = 32$. The band alignment of In_2O_3 and SnO_2 was then determined by aligning their CNLs with valence band edges rigidly shifted to reproduce the experimental band gaps.

III. Results and Discussion

Fig. 2(a) and (b) show the transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 1 μm and T_{ch} of 2.1 nm. Decent drain current saturation is observed at high V_{DS} up to 2 V. A low contact resistance (R_C) of 0.6 Ω·mm is extracted through the TLM method. Significant improvement of drain current can be achieved by channel length scaling. A maximum ON-state current of 970 mA/mm and an on/off ratio up to 10^7 are achieved at $V_{DS} = 0.8$ V for a scaled device with L_{ch} of 60 nm as shown in Fig. 2(c) and (d). Fig. 2(e)–(j) present similar transfer and output characteristics of scaled ITO transistors with In:Sn ratio of 6:1 and 3:1, as well as pure In_2O_3 transistors as the comparison group. Note that the hysteresis of the transfer curve is increasing from 0.14 V for In:Sn 9:1 device to 0.31 V for In:Sn 3:1 device, while a negligible hysteresis of 0.01 V is observed in pure In_2O_3 transistor, suggesting such hysteresis may origin from the traps at the In_2O_3/SnO_2 interface in ITO alloy formed during ALD growth.

Fig. 3 summarizes the scaling metrics of ITO transistors with different In:Sn ratios and L_{ch} from 60 nm to 1 μm. All parameters are extracted at V_{DS} of 0.1 V to avoid the impact of the self-heating effect. Each data point represents the average of at least three devices. The small error bar indicates the ultrathin ITO films grown by ALD are highly uniform at least in the area of 1 cm^2 sample size. Fig. 3(a) shows In:Sn ratio-dependent V_T relation. A trend of positive V_T shift is demonstrated as Sn concentration increases. Fig. 3(b) and (d) present the In:Sn ratio-dependent subthreshold slope (SS) and field-effect mobility (μ_{FE}) versus L_{ch} characteristics. A minimum SS of 163 mV/dec and a maximum μ_{FE} of 19 $cm^2/V{\cdot}s$ are achieved in the ITO transistor with In:Sn ratio of 9:1 and T_{ch} of 2.1 nm. The threshold voltage (V_T) was extracted by the linear-extrapolation method at $V_{DS} = 0.1$ V. SS was the average value over several decades in the subthreshold region.

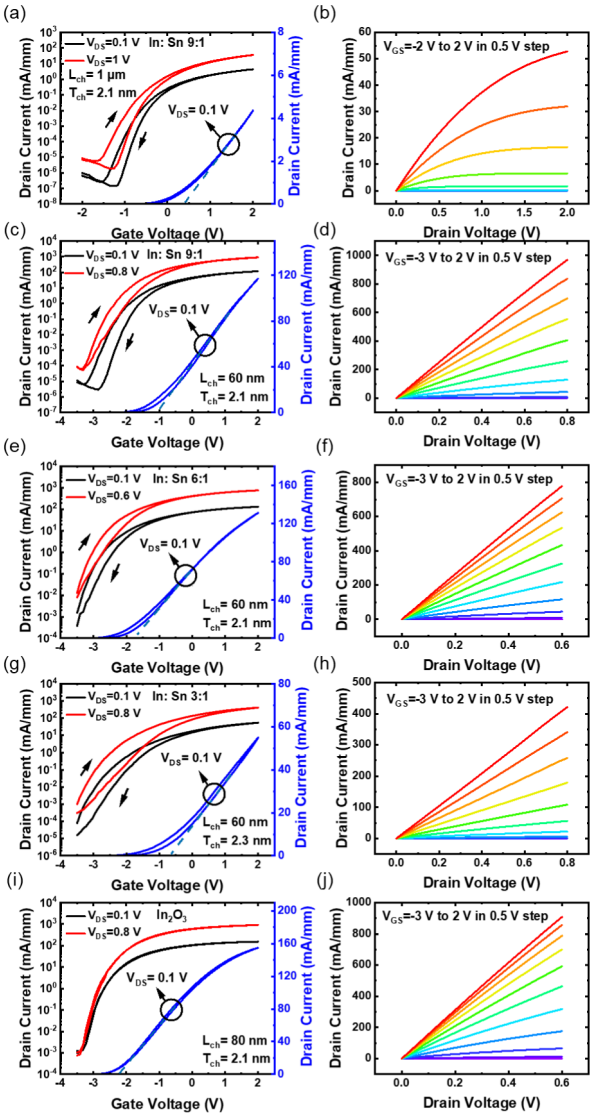


Fig. 2. (a) Transfer and (b) output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 1 μm, and T_{ch} of 2.1 nm. (c) Transfer and (d) output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 60 nm, and T_{ch} of 2.1 nm. (e) Transfer and (f) output characteristics of an ITO transistor with In:Sn ratio of 6:1, L_{ch} of 60 nm, and T_{ch} of 2.1 nm. (g) Transfer and (h) output characteristics of an ITO transistor with In:Sn ratio of 3:1, L_{ch} of 60 nm, and T_{ch} of 2.3 nm. (i) Transfer and (j) output characteristics of an In_2O_3 transistor with L_{ch} of 80 nm and T_{ch} of 2.1 nm.

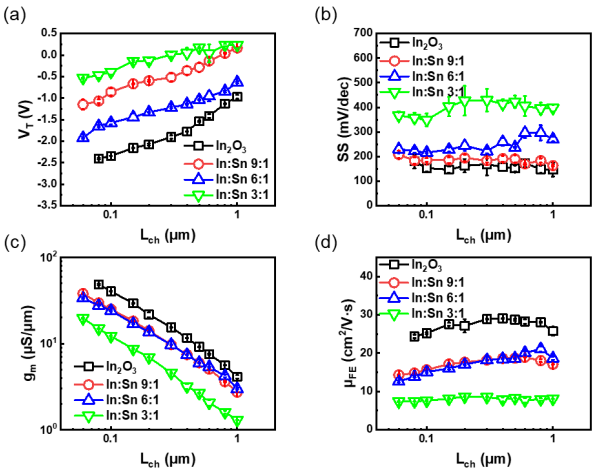


Fig. 3. (a) V_T, (b) SS, (c) g_m, (d) μ_{FE} scaling metrics of ITO transistors with In:Sn ratio of 9:1, 6:1, 3:1, L_{ch} from 60 nm to 1 μm and pure In_2O_3 transistors as a comparison group. T_{ch} of ITO transistors with In:Sn ratio of 9:1, 6:1, and In_2O_3 transistors is 2.1 nm. T_{ch} of ITO transistors with In:Sn ratio of 3:1 is 2.3 nm. Each data point represents the average of at least three devices.

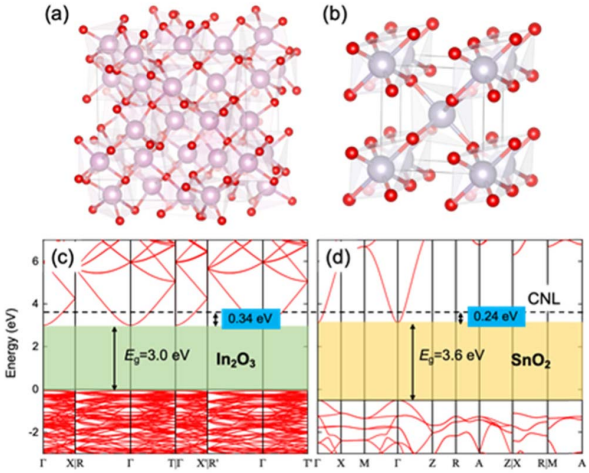


Fig. 4. Atomic structures of (a) In_2O_3 and (b) SnO_2 used for CNL and band alignment calculation. Band structures of (c) In_2O_3 and (d) SnO_2. The calculated CNL of In_2O_3 lies ~0.34 eV above CBE, while CNL of SnO_2 lies ~0.24 eV above CBE. CNLs are used for band alignment between In_2O_3 and SnO_2. The band edges are rigidly shifted to reproduce the experimental band gaps.

The g_m was measured at $V_{DS} = 0.1$ V and also the average value. All μ_{FE} were calculated at $V_{DS} = 0.1$ V. Besides, it can be seen that SS increases and μ_{FE} decreases with more Sn doping concentration in ALD ITO films.

To understand such In:Sn ratio-dependent device performance, DFT calculation was performed to determine the band alignment between In_2O_3 and SnO_2 as shown in Fig. 4. The presence of the interfaces and amorphous disorders in ALD films pins the Fermi level at the CNL. The band edges of In_2O_3 and SnO_2 are therefore positioned by aligning their CNLs to ensure the Fermi level stays continuously throughout the heterointerface [23]. For both In_2O_3 and SnO_2, their CNLs lie above the conduction band edges (CBE). Note that the calculated CNL of In_2O_3 (0.34 eV above E_C) is quantitatively agreeing with the experimental result of ~0.4 eV above E_C [24]. In this band alignment, the conduction band of SnO_2 is ~0.1 eV above that of In_2O_3, so electrons will accumulate in the In_2O_3 region in the In_2O_3-SnO_2 composite films. As a result, In_2O_3 would act as the main electron-conducting channel while SnO_2 behaves as the weak potential barrier in the ITO film against electron transport. Therefore, higher Sn concentration will reduce the electron transport through the In_2O_3 conduction pathway and lead to poorer device performance including larger SS and lower μ_{FE}.

Fig. 5(a) and (b) present the typical transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 60 nm, and T_{ch} of 2.1 nm after 300 °C annealing in O_2 for 60 s. An on/off ratio of 3.3×10^7 and a positive V_T of 0.33 V are achieved at V_{DS} of 0.1 V, indicating an enhancement-mode operation by definition. Such positive V_T shift can be understood by the filling of the existing oxygen vacancies in ALD ITO films. It is known that oxygen vacancies

act as shallow donors in doped In_2O_3, which accounts for the Fermi level pinned deeply in the conduction band [15], [25]. A previous study has reported the carrier density in pulsed laser deposited ITO film can be adjusted by O_2 pressure during growth [26]. Similarly, oxygen atoms induced during O_2 annealing can also fill oxygen vacancies, lower the electron density, and bring down the Fermi level. Fig. 5(c) and (d) show the transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 1 μm and T_{ch} of 2.1 nm after 300 °C annealing in O_2 for 60 s. The hysteresis is significantly reduced to 0.02 V compared to devices without annealing, suggesting O_2 annealing helps eliminate the traps at the In_2O_3/SnO_2 interfaces in the alloy ITO film. There is no obvious improvement in device performance by increasing O_2 annealing time. Fig. 5(e)–(h) presents the transfer and output characteristics of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm and 1 μm, respectively, T_{ch} of 2.1 nm after 300 °C annealing in FG for 60 s. Compared to as-fabricated devices, FG annealing at 300 °C slightly shifts the V_T negatively and has a limited effect to improve the In_2O_3/SnO_2 interface quality. FG annealing effect here is similar to other reported work on ternary or quaternary oxide semiconductors and in great contract to ALD In_2O_3 film [13].

Fig. 6 summarizes the scaling metrics of ITO transistors with In:Sn ratio of 9:1, 6:1, 3:1, and L_{ch} from 60 nm to 1 μm after O_2 and FG annealing at 250 °C and 300 °C for 60 s compared to devices without annealing. Fig. 6(a) compares V_T of ITO transistors with In:Sn ratio of 9:1 under different annealing conditions. A large positive V_T shift is observed in all O_2 annealed ITO transistors due to the filling of oxygen vacancies and likely also the reduction of defects induced in fabrication [13], [27]. Besides, O_2 annealing also weakens the L_{ch} dependent V_T. Fig. 6(b) and (d) show SS and μ_{FE} versus L_{ch} characteristics of ITO transistors with In:Sn ratio of 9:1 under different annealing conditions. A minimum SS of 80 mV/dec and a maximum μ_{FE} of 28 $cm^2/V{\cdot}s$ are achieved after O_2 annealing, which is comparable to other amorphous oxide semiconductor TFTs. Similar phenomena are also observed in ITO transistors with In:Sn ratio of 6:1 and 3:1 as shown in Fig. 6(e)–(l). Therefore, O_2 can be considered as a better choice to passivate the interface traps and improve device electrical performance in low-temperature annealing process [13], [27].

In addition, bias instability of ALD ITO transistors is also studied. Fig. 7(a) and (b) demonstrate the evolution of transfer characteristics of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm, and T_{ch} of 2.1 nm under gate bias of −3 and 3 V, respectively, for a stress time up to 2000 s. Fig. 7(c) and (d) show $-\Delta V_T$ versus time of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm and 1 μm. A negative V_T shift is observed in both cases under gate bias of −3 and 3 V, which is different from indium-gallium-tin-oxide (IGZO) TFTs where positive V_T shift is observed resulting from the charge trapping of accumulated electrons [28], [29]. Such a phenomenon can be explained by introducing the TNL model [30]. According to the previous calculation, TNL is located ~0.32 eV above the conduction band in ultrathin In_2O_3 [31]. Because of the similarity of ALD In_2O_3 and ALD ITO, it can be assumed

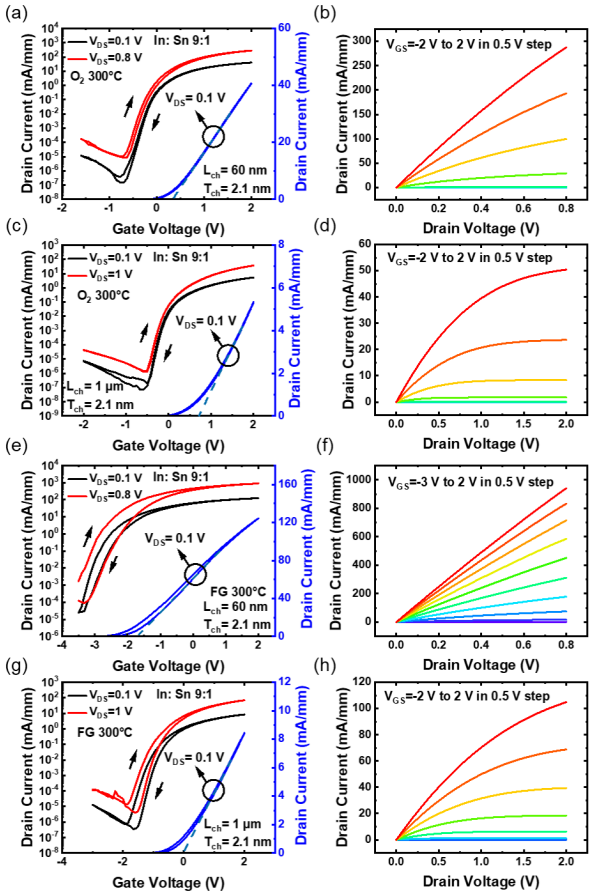


Fig. 5. (a) Transfer and (b) output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 60 nm and T_{ch} of 2.1 nm after 60 s O_2 annealing at 300 °C. (c) Transfer and (d) output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 1 μm and T_{ch} of 2.1 nm after 60 s O_2 annealing at 300 °C. (e) Transfer and (f) output characteristics an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 60 nm after 60 s FG annealing at 300 °C. (g) Transfer and (h) output characteristics of an ITO transistor with In:Sn ratio of 9:1, L_{ch} of 1 μm and T_{ch} of 2.1 nm after 60 s FG annealing at 300 °C.

that TNL in ITO is also likely to be deeply aligned in the conduction band due to its large density of valence band states [24], [32], [33]. Since the Fermi level is located below TNL, the donor-like interface states in between will always lead to a negative V_T shift regardless of the polarity of gate bias, similar to the observation in ALD In_2O_3 [33]. Fig. 7(e) and (f) show $-\Delta V_T$ as a function of stress time of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm and 1 μm after O_2 annealing at 250 °C for 60 s. The L_{ch} dependent $-\Delta V_T$ relation is nearly eliminated by the removal of defects after O_2 annealing. Fig. 7(g) and (h) present $-\Delta V_T$ as a function of stress time of ITO transistors with In:Sn ratio of 9:1 after FG annealing at 250 °C for 60 s. No big difference is observed between the results after FG annealing and as-fabricated ITO transistors, indicating ALD ITO films are more stable in FG compared to the serious hydrogen doping issue in IGZO [9], [34]. Reliability is one of the most important factors that need serious consideration in the development of a manufacturing technology. Despite the encouraging transistor characteristics of atomically thin ITO films demonstrated above, further experiments are still highly

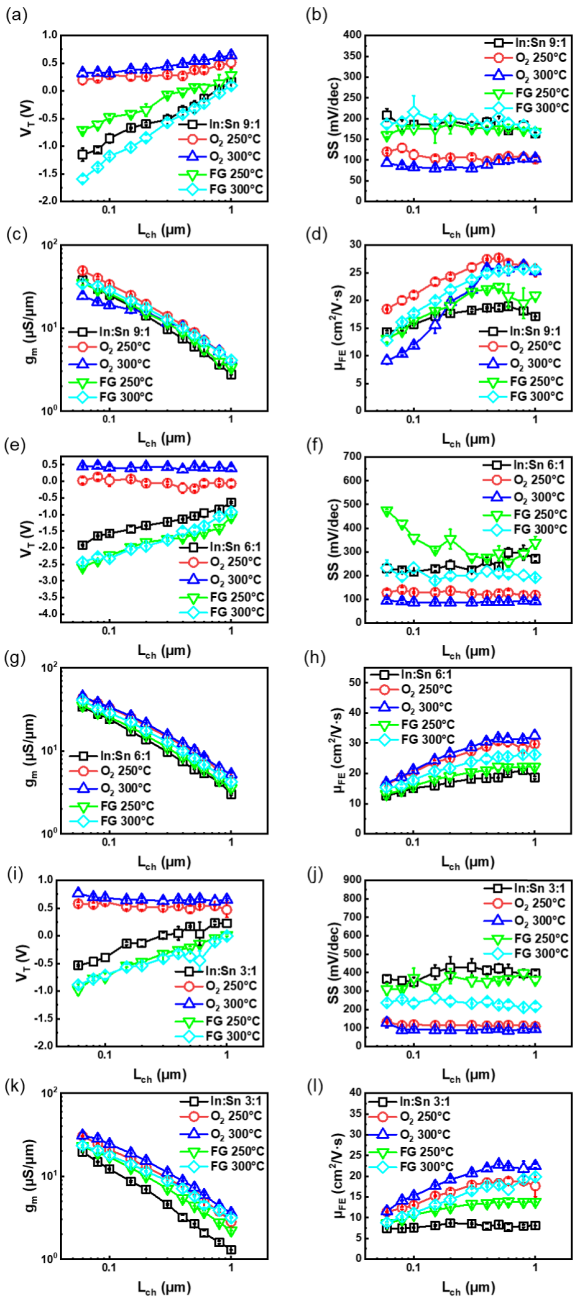


Fig. 6. (a) V_T, (b) SS, (c) g_m, (d) μ_{FE} scaling metrics of ITO transistors with In:Sn ratio of 9:1, L_{ch} from 60 nm to 1 μm and T_{ch} of 2.1 nm compared to the results after 60 s O_2 and FG annealing at 250 °C and 300 °C. (e) V_T, (f) SS, (g) g_m, (h) μ_{FE} scaling metrics of ITO transistors with In:Sn ratio of 6:1, L_{ch} from 1 μm to 60 nm and T_{ch} of 2.1 nm under same annealing conditions. (i) V_T, (j) SS, (k) g_m, (l) μ_{FE} scaling metrics of ITO transistors with In:Sn ratio of 3:1, L_{ch} from 60 nm to 1 μm and T_{ch} of 2.3 nm under same annealing conditions.

demanded to improve the interface quality and reduce bias instability to meet the requirement for the application of ALD ITO as a BEOL-compatible transistor channel.

Fig. 8 presents a benchmark of ON-state current versus film thickness of recent ITO transistors deposited by ALD and sputtering. It can be seen that ALD deposited ITO films exhibit comparably high ON-state current as sputtered ITO films. Meanwhile, ALD has a more accurate control of the film thickness with high reproducibility and conformability

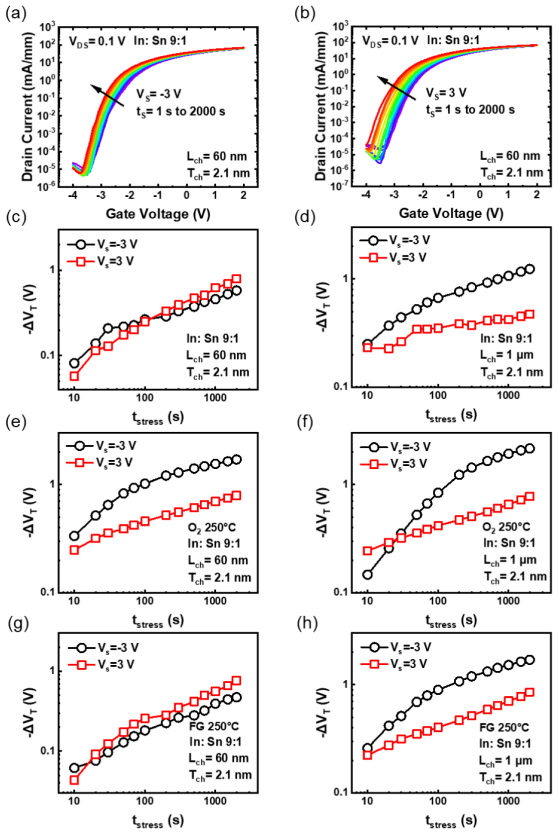
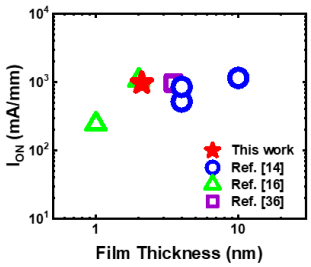


Fig. 7. Evolution of transfer characteristics of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm, and T_{ch} of 2.1 nm under gate bias of (a) −3 and (b) 3 V for a stress time of 2000 s. (c) and (d) V_{th} shift as a function of stress time of as-fabricated ITO transistors with In:Sn ratio of 9:1, T_{ch} of 2.1 nm, L_{ch} of 60 nm, and 1 μm separately. (e) and (f) V_{th} shift as a function of stress time of ITO transistors with In:Sn ratio of 9:1, L_{ch} of 60 nm and 1 μm after 60 s O_2 annealing at 250 °C. (g) and (h) V_{th} shift as a function of stress time of ITO transistors with In:Sn ratio of 9:1, T_{ch} of 2.1 nm, L_{ch} of 60 nm and 1 μm after 60 s FG annealing at 250 °C.



ITO	t_{ch} (nm)	L_{ch} (μm)	V_{DS} (V)
This work	2.1	0.06	0.8
Ref. [14]	4	0.04	2
	4	0.1	2
	10	0.2	1
Ref. [16]	1	0.8	4
	2	0.6	4
Ref. [36]	3.5	0.015	0.5

Fig. 8. Benchmark of ON-state current versus film thickness of recent ITO transistors. Solid symbol represents ITO films deposited by ALD and hollow symbols represent ITO films deposited by sputtering.

than sputtering, which paves way for further device scaling with high precision.

IV. Conclusion

In summary, atomically thin ITO transistors are demonstrated for the first time by the ALD process at 225 °C. A maximum ON-state current of 970 mA/mm at V_{DS} of 0.8 V and an on/off ratio up to 10^7 are achieved in ITO transistor with In:Sn ratio of 9:1, L_{ch} of 60 nm and T_{ch} of 2.1 nm. Comparison between ITO transistors with different In:Sn ratios reveals the effect of Sn concentration to impede the electron transport which is understood by DFT calculation of band

alignment of In_2O_3 versus SnO_2. BEOL-compatible low-temperature annealing is also systematically studied. An SS as low as 80 mV and a μ_{FE} of 28 $cm^2/V{\cdot}s$ are achieved after O_2 annealing due to the filling of oxygen vacancies and elimination of exhibiting defects. Finally, bias instability measurement shows a negative V_T shift for both positive and negative stress voltage, which is ascribed to the existence of donor-like interface states below TNL. This work provides prospects for the future application of ALD ITO films in monolithic 3-D integration.

REFERENCES

[1] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 5B, pp. 4303–4308, May 2006, doi: 10.1143/JJAP.45.4303.

[2] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, Feb. 2010, Art. no. 044305, doi: 10.1088/1468-6996/11/4/044305.

[3] H. Yabuta *et al.*, "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering," *Appl. Phys. Lett.*, vol. 89, no. 11, Sep. 2006, Art. no. 112123, doi: 10.1063/1.2353811.

[4] H. Y. Kim *et al.*, "Low-temperature growth of indium oxide thin film by plasma-enhanced atomic layer deposition using liquid dimethyl(*N*-ethoxy-2,2-dimethylpropanamido)indium for high-mobility thin film transistor application," *ACS Appl. Mater. Interfaces*, vol. 8, no. 40, pp. 26924–26931, Oct. 2016, doi: 10.1021/acsami.6b07332.

[5] I. H. Baek *et al.*, "High-performance thin-film transistors of quaternary indium-zinc-tin oxide films grown by atomic layer deposition," *ACS Appl. Mater. Interface*, vol. 11, no. 16, pp. 14892–14901, Apr. 2019, doi: 10.1021/acsami.9b03331.

[6] H. Salami, A. Uy, A. Vadapalli, C. Grob, V. Dwivedi, and R. A. Adomaitis, "Atomic layer deposition of ultrathin indium oxide and indium tin oxide films using a trimethylindium, tetrakis(dimethylamino)tin, and ozone precursor system," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 37, no. 1, Jan. 2019, Art. no. 010905, doi: 10.1116/1.5058171.

[7] C. R. Allemang *et al.*, "High-performance zinc tin oxide TFTs with active layers deposited by atomic layer deposition," *Adv. Electron. Mater.*, vol. 6, no. 7, Jul. 2020, Art. no. 2000195, doi: 10.1002/aelm.202000195.

[8] H. Kim *et al.*, "Indium tin oxide thin films for organic light-emitting devices," *Appl. Phys. Lett.*, vol. 74, no. 23, pp. 3444–3446, Jun. 1999, doi: 10.1063/1.124122.

[9] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 12, pp. 468–483, Dec. 2009, doi: 10.1109/JDT.2009.2034559.

[10] A. Nathan, S. Lee, S. Jeon, and J. Robertson, "Amorphous oxide semiconductor TFTs for displays and imaging," *IEEE/OSA J. Display Technol.*, vol. 10, no. 11, pp. 917–927, Nov. 2014, doi: 10.1109/JDT.2013.2292580.

[11] H.-I. Yeom, J. B. Ko, G. Mun, and S.-H.-K. Park, "High mobility polycrystalline indium oxide thin-film transistors by means of plasma-enhanced atomic layer deposition," *J. Mater. Chem. C*, vol. 4, no. 28, pp. 6873–6880, 2016, doi: 10.1039/c6tc00580b.

[12] J. Lee *et al.*, "High mobility ultra-thin crystalline indium oxide thin film transistor using atomic layer deposition," *Appl. Phys. Lett.*, vol. 113, no. 11, Sep. 2018, Art. no. 112102, doi: 10.1063/1.5041029.

[13] M. Si, A. Charnas, Z. Lin, and P. D. Ye, "Enhancement-mode atomic-layer-deposited In_2O_3 transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1075–1080, Mar. 2021, doi: 10.1109/TED.2021.3053229.

[14] S. Li *et al.*, "Nanometre-thin indium tin oxide for advanced high-performance electronics," *Nature Mater.*, vol. 18, no. 10, pp. 1091–1097, Oct. 2019, doi: 10.1038/s41563-019-0455-8.

[15] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[16] M. Si *et al.*, "Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating," *ACS Nano*, vol. 14, no. 9, pp. 11542–11547, Sep. 2020, doi: 10.1021/acsnano.0c03978.

[17] H. Kim *et al.*, "Effect of film thickness on the properties of indium tin oxide thin films," *J. Appl. Phys.*, vol. 88, no. 10, pp. 6021–6025, Nov. 2000, doi: 10.1063/1.1318368.

[18] M. Si, Z. Lin, A. Charnas, and P. D. Ye, "Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V," *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 184–187, Feb. 2021, doi: 10.1109/LED.2020.3043430.

[19] G. Kresse and J. Hafner, "*Ab initio* molecular-dynamics simulation of the liquid-metal–amorphous-semiconductor transition in germanium," *Phys. Rev. B, Condens. Matter*, vol. 49, no. 20, pp. 14251–14269, May 1994, doi: 10.1103/PhysRevB.49.14251.

[20] G. Kresse and J. Furthmüller, "Efficient iterative schemes for *ab initio* total-energy calculations using a plane-wave basis set," *Phys. Rev. B, Condens. Matter*, vol. 54, no. 16, pp. 11169–11186, Oct. 1996, doi: 10.1103/PhysRevB.54.11169.

[21] J. P. Perdew *et al.*, "Atoms, molecules, solids, and surfaces: Applications of the generalized gradient approximation for exchange and correlation," *Phys. Rev. B, Condens. Matter*, vol. 46, no. 11, pp. 6671–6687, Sep. 1992, doi: 10.1103/PhysRevB.46.6671.

[22] J. P. Perdew, K. Burke, and M. Ernzerhof, "Generalized gradient approximation made simple," *Phys. Rev. Lett.*, vol. 77, pp. 3865–3868, Oct. 1996, doi: 10.1103/PhysRevLett.77.3865.

[23] A. Schleife, F. Fuchs, C. Rödl, J. Furthmüller, and F. Bechstedt, "Branch-point energies and band discontinuities of III-nitrides and III-/II-oxides from quasiparticle band-structure calculations," *Appl. Phys. Lett.*, vol. 94, no. 1, Jan. 2009, Art. no. 012104, doi: 10.1063/1.3059569.

[24] P. D. C. King, T. D. Veal, D. J. Payne, A. Bourlange, R. G. Egdell, and C. F. McConville, "Surface electron accumulation and the charge neutrality level in In_2O_3," *Phys. Rev. Lett.*, vol. 101, no. 11, Sep. 2008, Art. no. 116808, doi: 10.1103/PhysRevLett.101.116808.

[25] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structure of the amorphous oxide semiconductor a-$InGaZnO_{4-x}$: Tauc–Lorentz optical model and origins of subgap states," *Phys. Status Solidi A*, vol. 206, no. 5, pp. 860–867, May 2009, doi: 10.1002/pssa.200881303.

[26] H. Kim, J. S. Horwitz, G. P. Kushto, Z. H. Kafafi, and D. B. Chrisey, "Indium tin oxide thin films grown on flexible plastic substrates by pulsed-laser deposition for organic light-emitting diodes," *Appl. Phys. Lett.*, vol. 79, no. 3, pp. 284–286, Jul. 2001, doi: 10.1063/1.1383568.

[27] A. Charnas, M. Si, Z. Lin, and P. D. Ye, "Enhancement-mode atomic-layer thin In_2O_3 transistors with maximum current exceeding 2 A/mm at drain voltage of 0.7 V enabled by oxygen plasma treatment," *Appl. Phys. Lett.*, vol. 118, no. 5, Feb. 2021, Art. no. 052107, doi: 10.1063/5.0039783.

[28] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, "Constant-voltage-bias stress testing of a-IGZO thin-film transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1365–1370, Jul. 2009, doi: 10.1109/TED.2009.2021339.

[29] K. H. Ji *et al.*, "Comparative study on light-induced bias stress instability of IGZO transistors with SiN_x and SiO_2 gate dielectrics," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1404–1406, Oct. 2010, doi: 10.1109/LED.2010.2073439.

[30] P. D. Ye, "Main determinants for III–V metal-oxide-semiconductor field-effect transistors (invited)," *J. Vac. Sci. Technol. A, Vac., Surf., Films*, vol. 26, no. 4, pp. 697–704, Jul. 2008, doi: 10.1116/1.2905246.

[31] M. Si *et al.*, "Why In_2O_3 can make 0.7 nm atomic layer thin transistors," *Nano Lett.*, vol. 21, no. 1, pp. 500–506, Jan. 2021, doi: 10.1021/acs.nanolett.0c03967.

[32] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. Process., Meas.*, vol. 18, no. 3, pp. 1785–1791, 2000, doi: 10.1116/1.591472.

[33] A. Charnas, M. Si, Z. Lin, and P. D. Ye, "Improved stability with atomic-layer-deposited encapsulation on atomic-layer In_2O_3 transistors by reliability characterization," *IEEE Trans. Electron Devices*, to be published.

[34] T. Kamiya and H. Hosono, "(Invited) roles of hydrogen in amorphous oxide semiconductor," *ECS Trans.*, vol. 54, no. 1, pp. 103–113, Jun. 2013, doi: 10.1149/05401.0103ecst.

[35] S. Li *et al.*, "BEOL compatible 15-nm channel length ultrathin indium-tin-oxide transistors with I_{on}= 970 $\mu A/\mu m$ and on/off ratio near 10^{11} at V_{ds}=0.5 V," in *IEDM Tech. Dig.*, 2019, pp. 3.5.1–3.5.4, doi: 10.1109/IEDM19573.2019.8993488.