

# Realization of Maximum 2 A/mm Drain Current on Top-Gate Atomic-Layer-Thin Indium Oxide Transistors by Thermal Engineering

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**Abstract**—In this work, we demonstrate the record high maximum drain current ( $I_D$ ) of 2 A/mm of top-gate (TG) indium oxide ( $\text{In}_2\text{O}_3$ ) transistors. The scaled and atomic-layer-deposited (ALD)  $\text{In}_2\text{O}_3$  transistors have channel length ( $L_{\text{ch}}$ ) down to 40 nm and channel thickness ( $T_{\text{ch}}$ ) down to 1.3 nm. Besides, the thermal budget of the whole material formation and device fabrication process is as low as 225 °C, making it compatible with back-end-of-line (BEOL) technologies by a huge margin. On the other hand, highly resistive silicon is utilized to serve as a desired high thermal conducting substrate to dissipate the generated heat efficiently as a larger current is conducted under a larger voltage bias. It greatly alleviates the self-heating effect (SHE) and allows an approximately 100% higher drain current. Quantitative studies of the SHE and channel temperature at ON-state with  $\text{SiO}_2/\text{Si}$  and highly resistive silicon substrates are also presented.

**Index Terms**—Atomic layer deposition, back-end-of-line (BEOL), oxide semiconductor.

## I. INTRODUCTION

BEING widely applied as channel materials for thin-film transistors (TFTs) and potentially for back-end-of-line (BEOL) compatible monolithic 3-D integration, oxide semiconductors have received extensive attention and been broadly explored in the past years [1]–[9]. Among them, indium oxide ( $\text{In}_2\text{O}_3$ ) [1]–[3] and doped indium oxides [4]–[8] are even of great interest because of their exceptional properties including high growth scalability and reproducibility to enable mass production, atomically smooth roughness to guarantee the surface quality, ambient stability to achieve little material degradation in air, and low thermal budget to be well suited with BEOL technologies.

Given its roughly 2.7-eV bandgap [9],  $\text{In}_2\text{O}_3$  as an oxide semiconductor has attracted revived attention as a

promising channel material. Especially, the conformal growth of the atomic-layer-deposited (ALD)  $\text{In}_2\text{O}_3$  enables it to form on uneven surfaces including sidewalls and deep trenches, which dramatically benefits the monolithic 3-D integration [1], [2], [10]–[13]. Moreover, another superiority of ALD is the ultrathin film growth and the precise thickness control down to the angstrom scale. It is known that as the physical size of transistors in integrated circuits becomes smaller according to Moore's law, electrostatic control of the devices begins to lose. To maintain the controllability, natural length (proportional to the square root of  $T_{\text{ch}}$ ) shorter than one-third of the  $L_{\text{ch}}$ , indicating an ultrathin channel, is favored [14]. Nonetheless, for ultrathin-body silicon devices, the mobility descends drastically with a power of six to the thickness [15], resulting in the low current density with the atomically thin channel such as 1–2 nm. Therefore, it requires a higher current density around this thickness range for a single device to conduct enough current. It has been reported that scaled back-gate (BG)  $\text{In}_2\text{O}_3$  transistors accomplish channel thickness ( $T_{\text{ch}}$ ) down to 0.7 nm [1] and drain current ( $I_D$ ) up to 2.2 A/mm in enhancement mode as 1.5-nm-thick  $\text{In}_2\text{O}_3$  acts as the channel [3], [16], qualifying  $\text{In}_2\text{O}_3$  as a candidate material which has advantages in the ultrathin-body transistors.

However, the investigations of the  $\text{In}_2\text{O}_3$  devices mostly focus on BG structure [1]–[3], and top-gate (TG)  $\text{In}_2\text{O}_3$  transistors are rarely explored. On the other hand, TG devices are particularly demanded in many practical integration applications. The challenges for TG devices are due to 1) the performance degradation of the  $\text{In}_2\text{O}_3$  channel after the growth of the high- $\kappa$  oxide gate dielectric and 2) the drastic self-heating effect (SHE) as the current density becomes higher under high voltage biases. For the former, it is proposed that the oxygen atoms in the  $\text{In}_2\text{O}_3$  layer are lost and taken away as the ALD hafnium oxide ( $\text{HfO}_2$ ) is formed, which intensely generates more oxygen vacancies in the  $\text{In}_2\text{O}_3$  channel and increases the OFF-state current value [17]. Fortunately, this is resolvable by lowering the growth temperature of  $\text{HfO}_2$  from 200 °C to 120 °C followed by a low-temperature rapid-thermal-annealing (RTA) treatment in an  $\text{O}_2$  environment. This method makes the TG  $\text{In}_2\text{O}_3$  devices gate-tunable; however, the maximum  $I_D$  reaches only 570 mA/mm [17] because of the thermal issue. In addition, the high channel temperature might even result in the damage of the gate dielectric and the diminishing of the long-term reliability [18], [19]. To address this, thermal engineering which has been applied to other materials [20]–[22] might be a solid solution.

Therefore, we herein realize ALD-based TG  $\text{In}_2\text{O}_3$  transistors achieving  $I_D$  as high as 2 A/mm by employing highly resistive silicon substrate to minimize SHE. In the previous

Manuscript received October 4, 2021; revised October 30, 2021; accepted November 3, 2021. Date of publication November 17, 2021; date of current version December 29, 2021. This work was supported in part by the Semiconductor Research Corporation (SRC), Nanoelectronic Computing REsearch (nCORE), the Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Center, in part by the SRC/Defense Advanced Research Projects Agency (DARPA), the Joint University Microelectronics Program (JUMP), the Applications and Systems Driven Center for Energy-Efficient Integrated Nanotechnologies (ASCENT) Center. The review of this article was arranged by Editor J. F. Conley. (Corresponding author: Peide D. Ye.)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TED.2021.3125923>.

Digital Object Identifier 10.1109/TED.2021.3125923

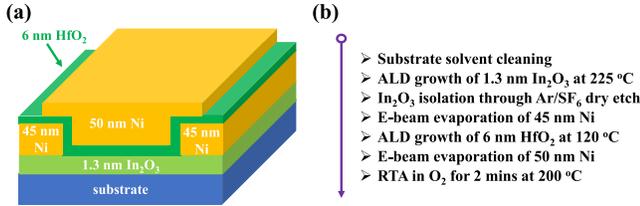


Fig. 1. (a) Schematic and (b) workflow of the fabrication process of a TG  $\text{In}_2\text{O}_3$  transistor. The substrate is either 90-nm thermally grown  $\text{SiO}_2$  on silicon or highly resistive silicon (resistivity  $\sim 10^5 \Omega \cdot \text{cm}$ ).

exploration [1]–[3], silicon dioxide on silicon ( $\text{SiO}_2/\text{Si}$ ) is usually chosen as the substrate due to its insulating property and vast commercial availability. Nevertheless, the thermal conductivity of silicon ( $\kappa = 142 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ ) [23] is approximately 100 times higher than  $\text{SiO}_2$  ( $\kappa = 1.1 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ ) [24], implying that the generated heat can be dissipated much more efficiently from the bottom as silicon serves as the substrate. In this case, we utilize highly resistive silicon (resistivity  $\sim 10^5 \Omega \cdot \text{cm}$ ) to block the leakage current through the substrate. Additionally, to estimate and compare the rough temperature of the channel with different substrates as a certain amount of current flows through, we measure the regression of the transconductance ( $g_m$ ) of  $\text{In}_2\text{O}_3$  TG transistors from room temperature to  $160^\circ\text{C}$  as an approximate channel thermometer [25]–[28]. It is revealed that the  $\text{In}_2\text{O}_3$  on  $\text{SiO}_2$  is already heated up to  $140^\circ\text{C}$  locally while the silicon devices are still under  $40^\circ\text{C}$  in the same condition. The enormous thermal conductivity difference benefits the realization of scaled TG  $\text{In}_2\text{O}_3$  transistors with high current carrying capacity up to a maximum  $I_D$  of 2 A/mm.

## II. EXPERIMENTS

Fig. 1 illustrates the schematic view of a TG  $\text{In}_2\text{O}_3$  transistor and the workflow of the fabrication. From bottom to top, the stacks are substrate (either 90-nm thermally grown  $\text{SiO}_2$  on silicon or highly resistive silicon), isolated  $\text{In}_2\text{O}_3$  channel with a thickness of 1.3 nm, 45-nm Ni serving as source and drain metal contacts, 6-nm  $\text{HfO}_2$  of the gate dielectric, and 50-nm Ni acting as TG metal electrode.

Standard solvent cleaning steps are followed before the substrates are used in the device fabrication process. 1.3-nm of  $\text{In}_2\text{O}_3$  thin film is deposited by ALD at  $225^\circ\text{C}$  with trimethylindium (TMIn) and  $\text{H}_2\text{O}$  as the In and O precursors, respectively, on the pre-cleaned substrates. The as-deposited  $\text{In}_2\text{O}_3$  thin film is isolated through a dry-etch process with  $\text{Ar}/\text{SF}_6$  plasma at room temperature. Then, 45-nm Ni as source and drain contacts are defined with variant  $L_{\text{ch}}$  by e-beam lithography, e-beam evaporation, and a lift-off process. On top of them, 6-nm  $\text{HfO}_2$  is conformally formed by ALD at  $120^\circ\text{C}$  with  $[(\text{CH}_3)_2\text{N}]_4\text{Hf}$  (TDMAHf) and  $\text{H}_2\text{O}$  as the Hf and O precursors, respectively. The relatively low temperature is chosen to minimize the interaction between  $\text{In}_2\text{O}_3$  and the growth of  $\text{HfO}_2$  to preserve the intrinsic properties of the channel semiconducting material [17] and dedicated ALD chambers are employed in order to prevent cross-contamination of  $\text{In}_2\text{O}_3$  and  $\text{HfO}_2$  deposition. 50-nm Ni serving as TG electrode is formed in the same way as the source and drain contacts. Last, the devices are treated with RTA in an  $\text{O}_2$  environment at  $200^\circ\text{C}$  for 2 min to reduce the oxygen vacancies in the  $\text{In}_2\text{O}_3$  channel induced by the ALD growth process of  $\text{HfO}_2$  [17]. The whole fabrication process requires a thermal budget as

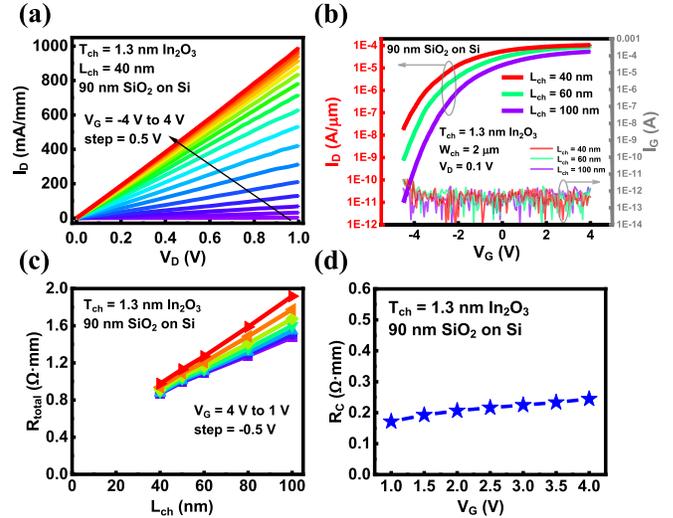
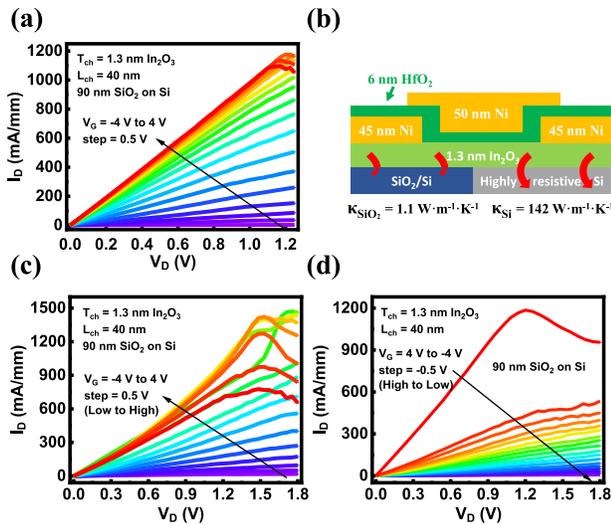


Fig. 2. (a) Output and (b) transfer characteristics of TG  $\text{In}_2\text{O}_3$  transistors with  $\text{SiO}_2/\text{Si}$  substrate and  $L_{\text{ch}}$  of (a) 40 nm and (b) 40, 60, and 100 nm. (c) Total resistance of the devices with variant  $L_{\text{ch}}$  on ON-state for TLM extraction. (d) Extracted  $R_C$  values from (c) showing great contact between the  $\text{In}_2\text{O}_3$  channel and source/drain contacts.

low as  $225^\circ\text{C}$  which is for the formation of the atomic-layer-thin  $\text{In}_2\text{O}_3$  channel.

## III. RESULTS AND DISCUSSION

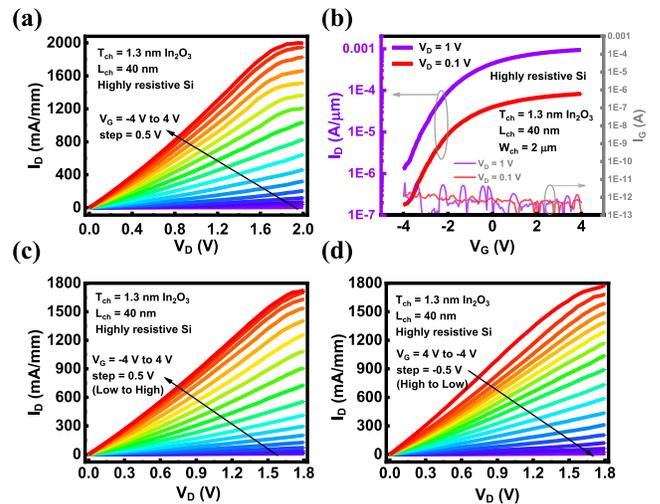
Fig. 2(a) exhibits the output characteristics of a representative TG  $\text{In}_2\text{O}_3$  transistor with  $L_{\text{ch}}$  of 40 nm,  $T_{\text{ch}}$  of 1.3 nm,  $W_{\text{ch}}$  of  $2 \mu\text{m}$ , 6-nm  $\text{HfO}_2$  as the TG dielectric,  $\text{SiO}_2/\text{Si}$  as the substrate, and annealing at  $200^\circ\text{C}$  in an  $\text{O}_2$  environment. The TG voltage ( $V_G$ ) sweeps from  $-4$  to  $4$  V with a 0.5-V step, and the maximum  $I_D$  achieves 991 mA/mm at  $V_G$  of 4 V and a drain voltage ( $V_D$ ) of 1 V, which surpasses the highest reported value of 570 mA/mm for TG  $\text{In}_2\text{O}_3$  transistors [17] to the best of our knowledge. Fig. 2(b) presents the transfer characteristics, showing an ON-OFF ratio of almost 4 to more than 6 orders with variant  $L_{\text{ch}}$  from 40 to 100 nm. The gate leakage currents are illustrated and much smaller than the drain currents. Some key parameters are extracted as follows, threshold voltage ( $V_T$ ) being  $-1.1$ ,  $-1.8$ , and  $-2.5$  V, subthreshold swing being 344, 433, and 577 mV/dec for  $L_{\text{ch}}$  of 100, 60, and 40 nm, respectively, and field-effect mobility ( $\mu_{\text{FE}}$ ) being  $4.1 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ . For the devices with  $L_{\text{ch}}$  of 100, 60, and 40 nm, the maximum  $I_D$  of them are 405, 660, and 991 mA/mm, respectively, at  $V_G$  of 4 V and  $V_D$  of 1 V. It is noticeable that the  $I_D$  of the transistors at  $V_G$  of 4 V and  $V_D$  of 1 V is roughly proportional to the inverse of the  $L_{\text{ch}}$ , indicating that 1) the semiconducting  $\text{In}_2\text{O}_3$  channel can be nicely scaled and 2) most of the resistance is contributed by the channel, that is, contact resistance ( $R_C$ ) is reasonably low. To further explore the  $R_C$  of TG  $\text{In}_2\text{O}_3$  devices at ON-state, the total resistances ( $R_{\text{total}}$ ) with different  $L_{\text{ch}}$  and  $V_G$  from 4 to 1 V are extracted and arranged into Fig. 2(c) where  $R_{\text{total}}$  consists of 1)  $2R_C$  designated to the contacts between the semiconducting channel and source/drain metal and 2) sheet resistance ( $R_{\text{sh}}$ ) contributed by the channel material and proportional to the  $L_{\text{ch}}$ . In each case of  $V_G$ , the extracted data points are in a superb linear fashion, and therefore, the  $R_C$  is accordingly obtained by extrapolation with a traditional transfer length measurement (TLM) method [29]. The y-axis intersection with the extrapolated regression line is regarded



**Fig. 3.** (a) Degraded  $I_D$  curves of a TG  $\text{In}_2\text{O}_3$  transistor with  $\text{SiO}_2/\text{Si}$  substrate and a large  $V_D$  up to 1.25 V, revealing the SHE. (b) Cross-sectional exhibition of the heat dissipation of  $\text{In}_2\text{O}_3$  devices with different substrates. Silicon with around 100 times higher thermal conductivity is able to passivate the generated thermal energy much more efficiently. Drastically degenerated and extremely chaotic  $I_D$ - $V_D$  curves with  $V_G$  sweeping (c) from low to high and (d) from high to low. The totally different behaviors imply that SHE is dominating over the transport performance.

as  $2R_C$ . Fig. 2(d) illustrates the acquired  $R_C$  under different  $V_G$  with the largest value of  $0.24 \Omega \cdot \text{mm}$  at  $V_G$  of 4 V, which is still lower than the reported value of  $0.36 \Omega \cdot \text{mm}$  [1] with a BG structure. The low  $R_C$  value implies that the  $\text{In}_2\text{O}_3$  channel and the Ni source/drain are of satisfactory contact in the TG structure.

Even though TG  $\text{In}_2\text{O}_3$  devices with  $\text{SiO}_2/\text{Si}$  substrates manifest  $I_D$  of roughly 1 A/mm, it is unable to achieve even higher as the BG transistors show up to 2.2 A/mm [3]. Fig. 3(a) reveals the difficulties as a larger  $V_D$  is applied. Noticeably, the curves of  $I_D$  start to saturate and then degrade while  $V_D$  of 1.25 V is kept applied with variant  $V_G$  sweeping, which is mostly ascribed to the SHE. As illustrated in Fig. 3(b), a large amount of heat could be generated when large current passes through the ultrathin  $\text{In}_2\text{O}_3$  channel. Nevertheless, the device is not capable of dissipating the created thermal energy efficiently when  $\text{SiO}_2/\text{Si}$  serves as the substrate, causing dramatic elevation of the local temperature and the damage of the  $\text{In}_2\text{O}_3$  channel. Under certain conditions, the transistors no longer behave well and are even unrecoverable. To further investigate the SHE, a larger  $V_D$  of 1.8 V is applied to two devices with one sweeping the  $V_G$  from low to high and the other one from high to low as exhibited in Fig. 3(c) and (d), respectively. The two situations reveal completely different results. Observably, in Fig. 3(c), the current degradation becomes more and more critical over the sweeps of larger  $V_G$ . The curves are entirely in an unexpected situation and the behavior becomes extremely unstable due to the severe SHE. The red color is chosen and utilized to imply the high-temperature condition. On the other hand, in Fig. 3(d), even the first curve already reveals poor performance with  $V_G$  of 4 V applied first. After the first measurement and thermal stress, the device is degraded significantly or partly damaged. All the following measurements show underscored performance. The limited capability of heat dissipation of the devices restricts themselves from broader applications. Note that similar SHE also exhibits on BG transistors [1]–[3].



**Fig. 4.** (a) Output and (b) transfer characteristics of TG  $\text{In}_2\text{O}_3$  transistors with highly resistive silicon substrate and  $L_{\text{ch}}$  of 40 nm. Cured  $I_D$ - $V_D$  curves with  $V_G$  sweeping (c) from low to high and (d) from high to low.

To address this issue, a thermal management method is adopted. Highly resistive silicon (resistivity  $\sim 10^5 \Omega \cdot \text{cm}$ ) is used to replace the  $\text{SiO}_2/\text{Si}$  substrate to assist in dissipating the generated thermal energy as large current is conducted. Silicon is chosen because of its much higher thermal conductivity of  $142 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$  [23] compared with that of  $\text{SiO}_2$   $1.1 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$  [24], the widely commercial availability, and the great affordability. Fig. 4(a) illustrates the output characteristics of a TG  $\text{In}_2\text{O}_3$  device with highly resistive silicon as the substrate, the same  $L_{\text{ch}}$  of 40 nm,  $T_{\text{ch}}$  of 1.3 nm, 6-nm of  $\text{HfO}_2$  as the TG dielectric, and  $200^\circ\text{C}$  RTA in an  $\text{O}_2$  environment. The only difference is the substrate in operation. Even with  $V_D$  of 2 V applied, the created heat can be majorly dissipated ascribed to the high thermal conductivity of silicon. Consequently, the critical SHE is considerably mitigated, and the device achieves a much higher  $I_D$  of 2 A/mm at  $V_D$  of 2 V and  $V_G$  of 4 V. The 2 A/mm value is around 100% higher than that of 0.99 A/mm with  $\text{SiO}_2/\text{Si}$  substrate. Fig. 4(b) exhibits the transfer characteristics of the device. It performs roughly three orders of ON-OFF ratio, which is close to that of  $\text{SiO}_2/\text{Si}$  in Fig. 2(b). To compare the SHE in the two cases, alike Fig. 3(c) and (d),  $V_D$  of 1.8 V is applied to two  $\text{In}_2\text{O}_3$  transistors with one sweeping the  $V_G$  from low to high and the other one from high to low. In Fig. 4(c), decent output curves are obtained. Unlike Fig. 3(c) exhibiting the dramatic current descent, Fig. 4(c) shows much healed SHE only with the utmost two curves being close. Similarly, in Fig. 4(d), even though the difference between the topmost two curves is a little larger, the severe SHE is greatly eliminated compared with Fig. 3(d) whose  $I_D$  degrades drastically within and after the first curve. With the huge discrepancies between Figs. 3(c) and (d) and 4(c) and (d), it is direct and unambiguous evidence that substituting the  $\text{SiO}_2/\text{Si}$  substrate with highly resistive silicon in TG  $\text{In}_2\text{O}_3$  transistors largely reduces the SHE and observably benefits its transport performance.

In order to further quantitatively explore the SHE on the TG  $\text{In}_2\text{O}_3$  device behavior, the current conducted through the transistors at ON-state with the two different substrates is measured ten times in a row. Because of the SHE, the local temperature at the  $\text{In}_2\text{O}_3$  channel will increase after each measurement and degrade the channel mobility and contacts, which leads to performance degradation in the following

measurements. The same dimensional parameters of 40-nm  $L_{ch}$ , 1.3-nm  $T_{ch}$ , and 6-nm  $HfO_2$  are utilized, and  $V_G$  of 4 V is chosen to ensure the entire experimental setup to be the same. Fig. 5(a)–(d) illustrates the ten collections of  $I_D$  curves with  $SiO_2/Si$  substrate and variant  $V_D$  applied where individual transistors with the same structure are employed in each subfigure. The  $V_D$  in Fig. 5(a) is only 0.5 V, and all the ten curves overlap with each other, meaning that no SHE takes place. The  $V_D$  in Fig. 5(b) is elevated to 0.8 V, and the curves start to decrease one time after another with around a 9% reduction in the tenth test compared to the first. The  $V_D$  applied in Fig. 5(c) is further enlarged to 1.0 V, and the distinctions between the curves become more obvious, indicating that SHE is deteriorating the electric behavior. The  $V_D$  in Fig. 5(d) is up to 1.8 V, and the performance in the first collection is already damaged, specifying the acute SHE. Moreover, the current degrades radically in the following measurements, and the  $I_D$  is decreased by approximately 77% compared to the first collection with the tenth. It is observable that the few topmost curves in this figure are principally similar to the ones in Fig. 3(d), implying that the SHE partly damages the device permanently as large  $V_G$  is applied first. Besides, it also verifies the reproducibility of the experiments and the consistency of the setup and devices. In great contrast to Fig. 5(d), Fig. 5(e) illustrates  $V_D$  of 1.8 V with silicon as the substrate. Observably, the SHE is mostly cured, and only a little degradation remains. The current deterioration between the first and the tenth measurement is only 7.5% which is even better than the case of  $V_D$  of 0.8 V with  $SiO_2/Si$ . The comparison of the degeneration over the ten collections between the two different substrates is arranged in Fig. 5(f), and the descending rate of highly resistive silicon substrate devices is less than 10% of the  $SiO_2/Si$  ones. The satisfactory capacity of heat dissipation of silicon considerably alleviates the serious SHE suffering  $SiO_2$  and profits the exceptional  $I_D$  of 2 A/mm for TG  $In_2O_3$  devices.

Besides, to roughly estimate the local temperature of the  $In_2O_3$  channel as operating at ON-state in a quantitative way, the changes of the transconductance ( $g_m$ ) under variant chuck temperature up to 160 °C are statistically investigated with  $SiO_2/Si$  serving as the substrate [25]–[27]. The  $g_m$  values here are extracted from  $I_D$ – $V_G$  measurements at  $V_G$  around 4 V. A long  $L_{ch}$  of 1  $\mu m$  and a low  $V_D$  of 50 mV are chosen to minimize the produced heat by the devices during the measurements. It is shown previously in Fig. 5(a) and discussed above that the SHE at  $V_D$  of 500 mV is already negligible and causes no degradation in the experiments. Therefore,  $V_D$  of 50 mV is more than safe to be utilized in the  $g_m$  measurements. In Fig. 6, each data point is calculated from at least five devices by dividing the average  $g_m$  with the certain chuck temperature by the  $g_m$  at that of 20 °C, and a minimum of 5 min is allowed after the environmental temperature becomes stable to ensure the preciseness. The error bars indicate 95% confidence intervals. Noticeably, the  $g_m$  of the TG  $In_2O_3$  transistors degrades relatively slowly before 80 °C, and 90% or more of the  $g_m$  is preserved within this range. On the other hand, it decreases substantially after 100 °C, and only 35% is left at 160 °C. Applying this effect as a rough channel thermometer, the local temperature at the channel is less than 40 °C after the 1.8-V measurements at  $V_G$  of 4 V on a silicon substrate as exhibited in Fig. 5(e) and based on the estimation of Fig. 6; while it reduces to roughly 1 A/mm [ $I_D$  at  $V_D = 1.8$  V of the first measurement

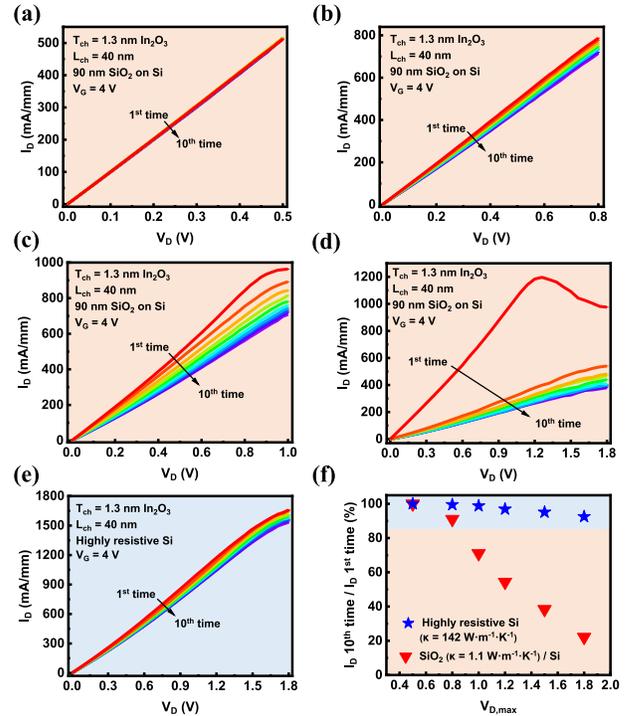


Fig. 5.  $I_D$ – $V_D$  measurement of TG  $In_2O_3$  transistors with (a)  $V_D$  up to 0.5 V and  $SiO_2/Si$  substrate, (b)  $V_D$  up to 0.8 V and  $SiO_2/Si$  substrate, (c)  $V_D$  up to 1 V and  $SiO_2/Si$  substrate, (d)  $V_D$  up to 1.8 V and  $SiO_2/Si$  substrate, and (e)  $V_D$  up to 1.8 V and highly resistive silicon substrate ten times in a row. (f)  $I_D$  preservation percentage between the first and tenth measurement with different  $V_D$  and substrates.

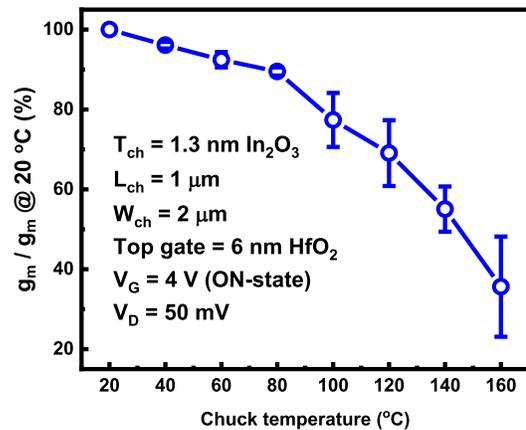


Fig. 6.  $g_m$  regression of TG  $In_2O_3$  devices with long channels of 1  $\mu m$ , low  $V_D$  of 50 mV, and ascending temperature up to 160 °C as an approximate channel thermometer.

in Fig. 5(d)] from 1.8 A/mm [ $I_D$  at  $V_D = 1.8$  V on silicon in Fig. 4(d)]. 45% reduction in  $g_m$  and  $I_D$  refers to 140 °C device temperature from Fig. 6, which is significant. The evidential contrast specifies that the thermal engineering methodology does benefit the improved performance of the  $In_2O_3$  TG transistors.

For high power density devices in general, substrates with even higher thermal conductivity might be desired. For instance, it is revealed that diamond ( $\kappa = 1000$ – $2200$  W·m<sup>-1</sup>·K<sup>-1</sup> [22], [28]) as a substrate is capable of further profiting the performance of  $\beta$ - $Ga_2O_3$ -based power devices [22]. Nevertheless, the transparent body of diamond upraises the fabrication difficulties to a great extent, and its narrower commercial availability and much poorer affordability compared with a

wide variety of silicon restrict it from mass production. With moderate power density, TG  $\text{In}_2\text{O}_3$  transistors with highly resistive silicon substrate are sufficient enough for dissipating the produced heat efficiently to avoid self-heating as previously presented and discussed, which makes it much more competitive in the realistic implementation and qualifies it in practical applications. For BEOL-compatible monolithic 3-D integration, high thermal conductive interlayer material is obviously desired for addressing thermal management issues.

#### IV. CONCLUSION

In summary, TG atomic-layer-thin  $\text{In}_2\text{O}_3$  transistors on  $\text{SiO}_2/\text{Si}$  substrate or highly resistive silicon substrate are investigated. In the former case, a maximum  $I_D$  of 1 A/mm is achieved by scaling the  $L_{ch}$  down to 40 nm, and a low  $R_C$  of 0.24  $\Omega\cdot\text{mm}$  is obtained. By replacing the substrate with highly resistive silicon, the maximum  $I_D$  is elevated by approximately 100% to 2 A/mm. The significant improvement is due to the much higher thermal conductivity of silicon to dissipate the generated heat through the bottom substrate efficiently and mitigate the SHE. A quantitative study of the SHE on TG  $\text{In}_2\text{O}_3$  devices is performed, and a rough thermometer based on the changes of the  $g_m$  under variant temperature is utilized to estimate the local temperature of  $\text{In}_2\text{O}_3$  channels at ON-state. The current degradation rate with ascending temperature of silicon is less than 10% of  $\text{SiO}_2$ , and the channel temperature is safely under 40 °C as highly resistive silicon serves as the substrate while up to 140 °C with  $\text{SiO}_2/\text{Si}$  substrate. Thermal engineering using high thermal conducting substrate or interlayer becomes critical for further exploration of  $\text{In}_2\text{O}_3$  transistors with high current carrying capacity in practical monolithic 3-D integration applications.

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