Low-Frequency Noise and Random Telegraph Noise on Near-Ballistic III–V MOSFETs

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***Abstract*— In this paper, we report the observation of random telegraph noise (RTN) in highly scaled InGaAs gate-all-around (GAA) MOSFETs fabricated by a top-down approach. RTN and low-frequency noise were systematically studied for devices with various gate dielectrics, channel lengths, and nanowire diameters. Mobility fluctuation is identified to be the source of 1/f noise. The 1/f noise was found to decrease as the channel length scaled down from 80 to 20 nm comparing with classical theory, indicating the near-ballistic transport in highly scaled InGaAs GAA MOSFET. Low-frequency noise in ballistic transistors is discussed theoretically.**

***Index Terms*— Ballistic transport, gate-all-around (GAA), InGaAs, low-frequency noise, MOSFET, random telegraph noise (RTN).**

I. Introduction

InGaAs has been considered as one of the promising channel materials for future CMOS logic circuit because of its large electron injection velocity [1]. In the last decade, tremendous efforts have been spent on the development of high-performance InGaAs transistors with both competitive ON-state and OFF-state performance to replace silicon in low-power and high-speed applications [2]–[10]. In particular, InGaAs gate-all-around (GAA) MOSFETs have been demonstrated to offer large drive current and excellent immunity to short channel effects down to deep sub-100-nm channel length (L_{ch}) [2]. However, one of the bottlenecks that prevents InGaAs MOSFETs to be applied in mainstream industry is the defective interface and gate-stack [11]–[13]. Thus, accurate and reliable measurement of interface and oxide property on a single device is required for device characterization and process optimization. However, the conventional oxide characterization methods, such as, C–V method and charge pumping method, cannot be used for ultrasmall devices without a body contact. Meanwhile, noise measurement is not limited by the small gate capacitance. Therefore, low-frequency noise and random telegraph noise (RTN) characterizations can be used as alternate probes to quantitatively analyze performance, variability, and reliability of highly scaled devices [14]–[22]. Furthermore, low noise is required in advanced digital or analog circuit applications, so that it is important to systematically study the noise performance and identify noise sources for transistors made of new material systems such as InGaAs MOSFETs [23].

It has been generally admitted that the low-frequency noise in MOSFETs can be well described by carrier number fluctuation model or mobility fluctuation model [23]. RTN is attributed to the trapping and detrapping event in a single defect. 1/f noise is the superposition of a number of individual RTNs in the carrier number fluctuation theory. On the other hand, classical theories suggest that 1/f noise increases inversely with decreasing channel length [24]–[31]. If true, this may negate some of the performance gain of short channel transistors [14]–[16]. Several groups have recently reported RTN of bottom-up synthesized long-channel InAs nanowire MOSFETs [32]–[34], and InGaAs FinFETs [35]. However, there have not been any work systematically studies low-frequency noise and RTN on highly scaled InGaAs MOSFETs.

In this paper, we: 1) report the observation of RTN on top-down fabricated InGaAs GAA MOSFETs; 2) examine the origin of low-frequency noise on highly scaled InGaAs GAA MOSFETs; 3) systematically study the property of low-frequency noise and RTN characteristics on near-ballistic InGaAs GAA nanowire MOSFETs with nanowire width (W_{NW}) varying from 20 to 35 nm, channel length varying from 20 to 80 nm, and with various gate dielectrics; and 4) theoretically study and predict the low-frequency noise behavior in transistors working in ballistic limit.

II. Experiment

Fig. 1(a) shows the schematic and cross-sectional view of an InGaAs GAA MOSFET. The top-down fabrication process can be found in [2]. The samples used for noise characterizations and device dimensions are summarized in Table I. Samples A and B have a 0.5-nm Al_2O_3/4 nm $LaAlO_3$ stack (EOT = 1.2 nm), where Al_2O_3 was grown before $LaAlO_3$ for Sample A and vice versa for Sample B, EOT is equivalent oxide thickness. Sample C has 3.5-nm Al_2O_3 as gate dielectric (EOT = 1.7 nm). The InGaAs channel layer consists of one 10-nm $In_{0.53}Ga_{0.47}As$ layer sandwiched by two 10-nm

Manuscript received March 9, 2015; revised May 11, 2015; accepted May 13, 2015. Date of publication June 1, 2015; date of current version October 20, 2015. This work was supported in part by the Defense Threat Reduction Agency through the Basic Research under Award HDTRA1-14-1-0039 and in part by the Air Force Office of Scientific Research. The review of this paper was arranged by Editor J. S. Suehle.

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Digital Object Identifier 10.1109/TED.2015.2433921

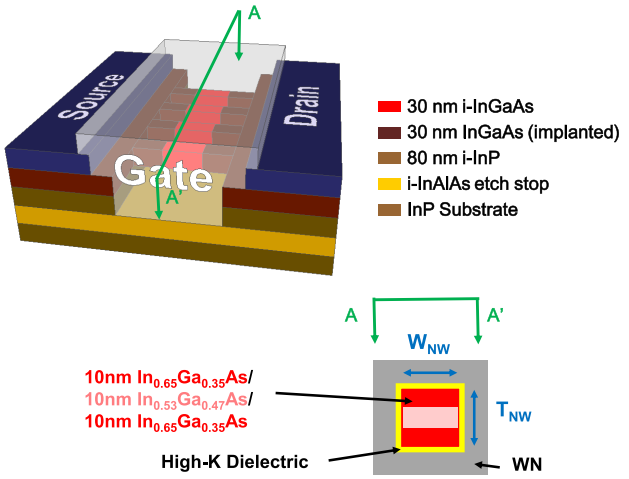

Fig. 1. Schematic and cross section of the present InGaAs GAA MOSFETs.

TABLE I
DESCRIPTION OF SAMPLES AND DEVICE DIMENSIONS

	Sample A (Al_2O_3 first)	Sample B ($LaAlO_3$ first)	Sample C (Al_2O_3 only)
Channel Material	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$	10 nm $In_{0.65}Ga_{0.35}As$/ 10 nm $In_{0.53}Ga_{0.47}As$/ 10 nm $In_{0.65}Ga_{0.35}As$
L_{ch} (nm)	20	20, 30, 50, 80	20
L_{NW} (nm)	200	200	200
W_{NW} (nm)	20	20, 25, 30, 35	20
T_{NW} (nm)	30	30	30
Gate Dielectric	0.5nm Al_2O_3/ 4nm $LaAlO_3$	4nm $LaAlO_3$/ 0.5nm Al_2O_3	3.5nm Al_2O_3
EOT (nm)	1.2	1.2	1.7

$In_{0.65}Ga_{0.35}As$ layers. Devices with L_{ch} varying from 20 to 80 nm, W_{NW} varying from 20 to 35 nm, nanowire thickness (T_{NW}) of 30 nm and nanowire length (L_{NW}) of 200 nm are measured. L_{NW} is the physical length of the nanowire, while L_{ch} is the channel length defined by implantation.

Source current power spectral density (S_{Is}) was measured in the linear region of operation (V_{ds} = 50 mV). The gate voltage (V_{gs}) is supplied by a digital controllable voltage source. A Stanford SR570 battery-powered current amplifier is used as source voltage supply and monitor and amplifier for the source current (I_s). I_s is used due to the relatively large junction leakage current in drain current (I_d). I_s shows more clearly the fundamental transport properties inside the nanowire. The SR570 current amplifier output is directly connected to a Tektronix TDS5032B oscilloscope to record RTN signal and an Agilent 35670A dynamic signal analyzer to obtain the power spectrum density (PSD) of the noise of I_s at the same time. All noise measurements were performed at V_{ds} = 50 mV and at V_{gs} from −0.2 to 0.4 V and at room temperature unless otherwise specified. Positive bias temperature instability measurement confirms that V_T shift <10 mV during noise measurement (maximum V_{gs} = 0.4 V) is ensured [36], so that I_s shift is negligible during noise measurement.

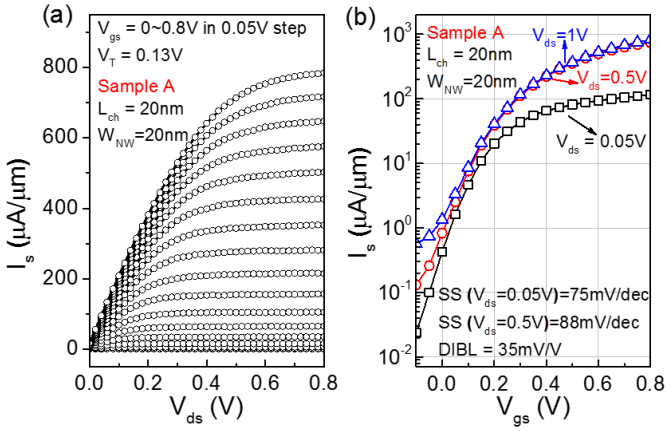

Fig. 2. (a) Output and (b) transfer characteristics of an L_{ch} = 20 nm InGaAs GAA MOSFET with $Al_2/O_3/LaAlO_3$ gate dielectric (Sample A, EOT = 1.2 nm) and W_{NW} = 20 nm. I_s is used due to a relatively large junction leakage current in I_d.

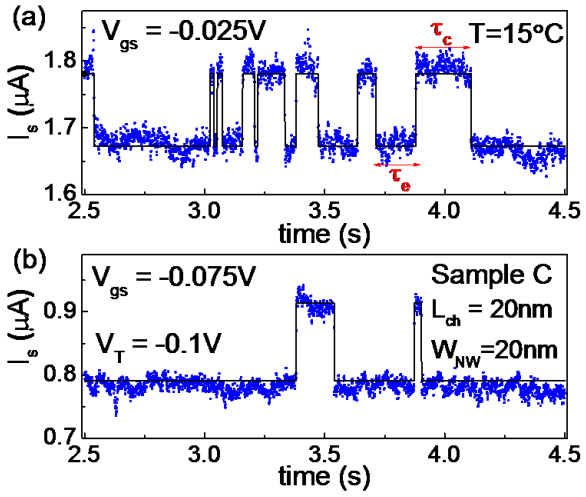

Fig. 3. I_s fluctuation due to RTN in (a) V_{gs} = −0.025 V and (b) V_{gs} = −0.075 V on InGaAs GAA MOSFETs measured at 15 °C. Capture/emission time constants (τ_c/τ_e) are defined in (a).

III. RESULTS AND DISCUSSION

Fig. 2(a) and (b) shows a typical output and transfer characteristics of a GAA MOSFET measured in this paper with $L_{ch} = W_{NW} = 20$ nm. Fig. 3(a) and (b) shows RTN signals in time domain of an InGaAs GAA MOSFET, with L_{ch} = 20 nm, W_{NW} = 20 nm, and 3.5 nm Al_2O_3 as gate dielectric, at $V_{gs} = -0.025$ V and $V_{gs} = -0.075$ V at 15 °C. Two distinct current switching levels are observed, which clearly indicates the existence of a single active trap. Fig. 4 shows S_{Is} normalized by I_s^2 (i.e., S_{Is}/I_s^2) of the RTN signal shown in Fig. 3(a). A typical Lorentzian spectrum is shown in the noise spectrum with $1/f^2$ characteristics. Clear RTN signals were observed on ~1/3 of devices measured on Samples A, B, and C, but only when V_{gs} is near threshold voltage (V_T). The PSD of devices without RTN signals shows 1/f characteristics.

Fig. 5 shows (a) I_s histogram and (b) RTN signal in time domain on an L_{ch} = 20 nm, W_{NW} = 25 nm device of Sample B, (c) a time segment inside (b), showing the superposition of two switching level signal and a Gaussian-like noise.

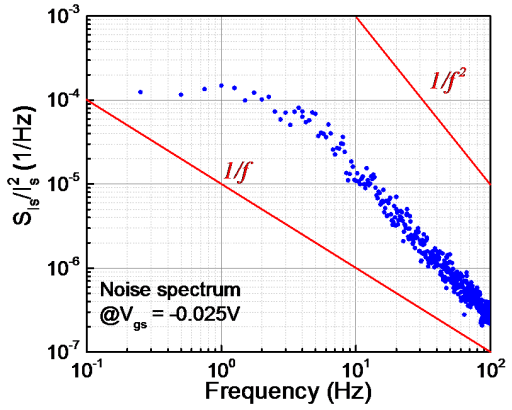

Fig. 4. Normalized I_s noise of RTN signal shown in Fig. 3(a), showing $1/f^2$ characteristics.

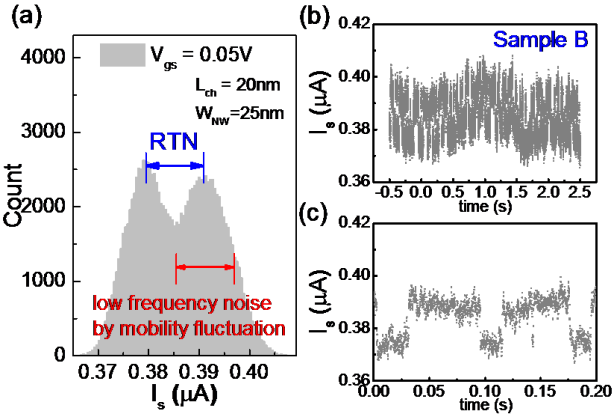

Fig. 5. (a) Histogram of an RTN signal of Sample B with $L_{ch} = 20$ nm and $W_{NW} = 25$ nm. (b) and (c) RTN signals in time domain of the same signal as (a). (c) is a time segment inside (b).

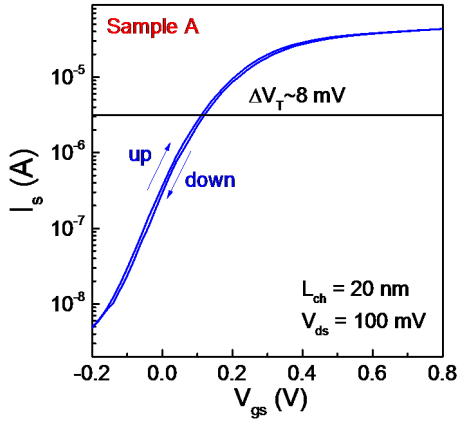

Fig. 6. Measurement of hysteresis of a typical device of Sample A with $L_{ch} = 20$ nm and $W_{NW} = 20$ nm. The device shows negligible hysteresis. The estimated trap number by hysteresis is on the order of several traps.

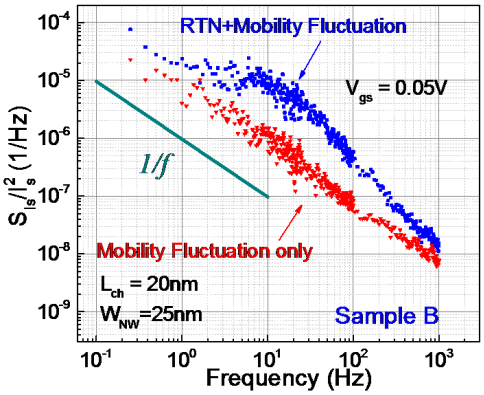

Fig. 7. Normalized I_s noise of Sample B devices with RTN signal and without RTN signal. Noise spectrum of device without RTN is attributed to mobility fluctuation.

In the device without an RTN signal, the I_s histogram shows only Gaussian-like distribution and with a 1/f noise spectrum. This phenomenon suggests the fact that mobility fluctuation (rather than number fluctuation) is the origin of the 1/f noise on devices without RTN signal. In classical noise theory, 1/f noise in MOSFETs can be well described by carrier number fluctuation model or mobility fluctuation model [23]. For carrier number fluctuation theory, current fluctuation in a MOSFET is attributed to the trapping and detrapping events within a number of traps which induces V_T shift. Each individual trapping and detrapping event has a Lorentzian spectrum, as shown in Fig. 4, so-called RTN. The 1/f spectrum is the superposition of these Lorentzian spectra, as suggested by McWhorter model [37]. In this paper, the number of traps is not likely to be enough to support a 1/f spectrum and that explains why RTN is observed. Fig. 6 shows the measurement of hysteresis of a typical device of Sample A with $L_{ch} = 20$ nm and $W_{NW} = 20$ nm. By estimating the electron trapping events that are responsible for the hysteresis, we can estimate the number of defects in the oxide. The estimated number of active defects is calculated as $AC_{ox}\Delta V_T/q$, where A is the gate area for the devices, C_{ox} is the gate capacitance calculated from EOT, ΔV_T is the hysteresis V_T shift, and q is the elementary charge. ΔV_T of Sample A is on the order of several millivolt measured with maximum $V_{gs} = 0.8$ V, corresponding to several active traps. Furthermore, not all traps will be effective to the current fluctuation because of distribution of trap energy levels, in other words, not all oxide traps are active at a certain gate voltage. Moreover, the inversion charges in this paper are farther from the interface than planar MOSFETs due to the volume inversion nature of GAA MOFSETs, as suggested by simulation results [38]. It could potentially reduce the interaction between oxide traps and inversion charges, as suggested in low-frequency noise study in silicon nanowire MOSFETs [30].

Therefore, for those devices with 1/f spectrum in which RTN signal cannot be observed, mobility fluctuation is the source of low-frequency noise. Fig. 7 shows the comparison of noise spectrum between a device with RTN signal and a device without RTN. The two devices share the same device dimension with $L_{ch} = 20$ nm, $W_{NW} = 25$ nm, and 3.5 nm Al_2O_3 as gate dielectric. It is clear that noise spectrum of the device without RTN shows 1/f characteristic, while the noise spectrum of the device with RTN is the superposition of 1/f noise spectrum and a Lorentzian spectrum. This is not the only evidence for the identification of noise source as mobility

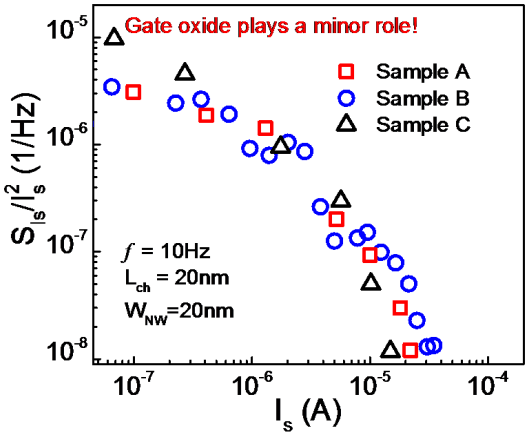

Fig. 8. PSD of I_s normalized by I_s^2 versus I_s at $f = 10$ Hz for Samples A, B, and C devices with $L_{\rm ch} = 20$ nm and $W_{\rm NW} = 20$ nm. Devices with different gate oxides exhibit similar noise level, showing weakly dependent on interfaces and types of oxides.

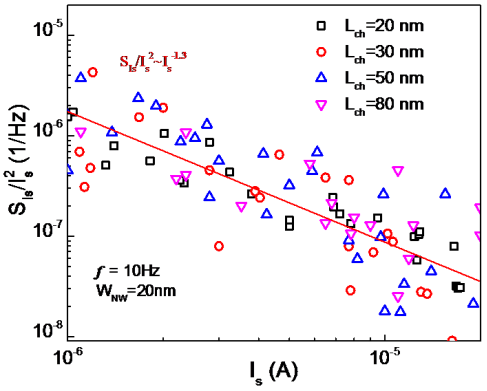

Fig. 9. PSD of I_s normalized by I_s^2 at $f = 10$ Hz for various $L_{\rm ch}$ and $W_{\rm NW} = 20$ nm at $V_{\rm ds} = 0.05$ V on Sample B. Normalized I_s noise versus I_s of devices with different values of $L_{\rm ch}$ weakly depend on interfaces and types of oxides. At least five devices are measured for each $L_{\rm ch}$, showing a statistical trend.

fluctuation in this paper. This fact will be further discussed in the following part. Fig. 8 shows $S_{\rm Is}/I_s^2$ as a function of I_s on Samples A, B, and C with $L_{\rm ch} = 20$ nm and $W_{\rm NW} = 20$ nm at $f = 10$ Hz, which is weakly dependent on interface and oxide quality. All the three selected devices show 1/f spectrum and no RTN was observed. $S_{\rm Is}/I_s^2$ can be modulated by I_s indicates the noise source is from channel other than series resistance. Meanwhile, $S_{\rm Is}/I_s^2$ depends only weakly on types of gate oxide and interface, suggesting that oxide trapping and detrapping induced carrier number fluctuation might not be the source of low-frequency noise in this paper.

Fig. 9 shows source current PSD normalized by I_s^2 ($S_{\rm Is}/I_s^2$) versus I_s at $f = 10$ Hz, $W_{\rm NW} = 20$ nm, and various channel lengths for Sample B. $S_{\rm Is}/I_s^2$ versus I_s shows weakly dependence on $L_{\rm ch}$, which is opposite to the classical noise $L_{\rm ch}$ scaling characteristics ($S_{\rm Is}/I_s^2 \sim 1/L_{\rm ch}$ at a given current). Fig. 10 shows the input gate noise (S_{Vg}) normalized by channel area ($\rm WLS_{Vg}$) versus I_s. It can be seen clearly that the normalized input noise is reduced by channel length scaling down, while in classical theory $\rm WLS_{Vg}$ should be

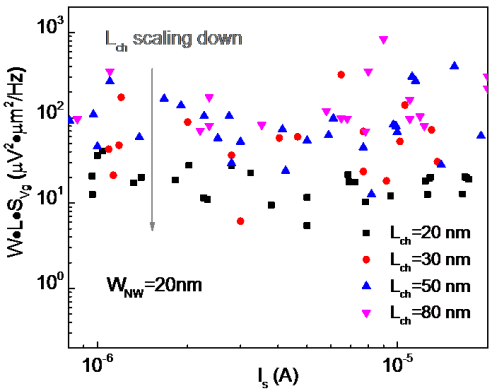

Fig. 10. Input gate voltage noise normalized by channel width times channel length of the same data set as Fig. 9. W is the channel width and L is the channel length in this figure.

independent of channel area. In both classical carrier number fluctuation model and mobility fluctuation model, S_{Vg} and $S_{\rm Is}/I_s^2$ is inversely proportional to $L_{\rm ch}$. The experimental data show that the I_s noise measured in the InGaAs GAA MOSFETs is reduced at short channel devices comparing with classical theory. This phenomenon cannot be explained by carrier number fluctuation theory because the V_T shift caused by a single trapping and detrapping event can be estimate simply by $\Delta V_T = q/(AC_{\rm ox})$, where A is proportional to $L_{\rm ch}$. We will have larger ΔV_T at smaller channel length, so that amplitude of the single trapping and detrapping event is increased. As current fluctuation is the combination of a number of single trapping and detrapping events, noise will be increased while channel length scaling down if carrier number fluctuation noise dominates the $S_{\rm Is}/I_s^2$. Thus, the anomalous scaling trend in Figs. 9 and 10 also indicate that the carrier number fluctuation is not the source of 1/f noise in the highly scaled InGaAs GAA MOSFETs. In classical theory of noise sources diagnosis, $S_{\rm Is}/I_s^2$ is proportional to $(g_m/I_s)^2$ for carrier number fluctuation, while $S_{\rm Is}/I_s^2$ is proportional to $1/I_s$ in mobility fluctuation theory [39]. However, there have not been any theoretical study on whether this diagnosis will still work on ballistic or near-ballistic transistors. In this paper, the slope of $S_{\rm Is}/I_s^2$ versus I_s is extracted in Fig. 9 to be -1.3, which is close to -1, by linear fitting of all the measured data in log–log plot from weak inversion to ON-state. But it is still open to question that whether classical theory on this slope still to be correct in near-ballistic regime. The Hooge's parameter is estimated as $3\times10^{-4}-1.2\times10^{-3}$ depending on the channel length [40].

This weak dependence of $S_{\rm Is}/I_s^2$ versus I_s on $L_{\rm ch}$ leads to the conclusion of this paper that the near-ballistic transport of electrons in the channel is achieved through noise study. Although mobility fluctuation model also suggests $1/L_{\rm ch}$ scaling metrics for $S_{\rm Is}/I_s^2$, this conclusion might not be the truth in devices with short channel length and long mean free path in high mobility channel materials. As electrons from source cannot equilibrate to lattice temperature immediately at drain contact, the classical mobility fluctuation model, which assumes uniform carrier distribution and diffusive transport,

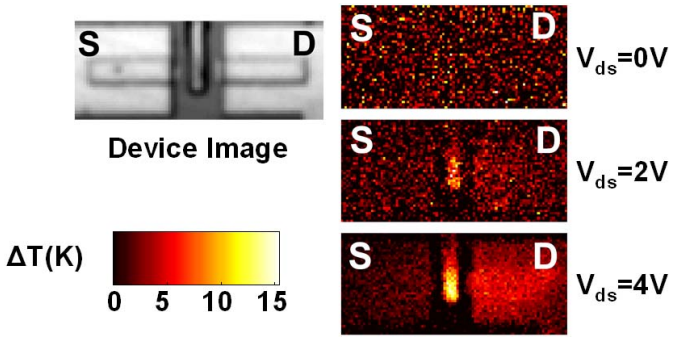

Fig. 11. Thermoreflectance image on an InGaAs GAA MOSFET with $L_{ch} = 80$ nm, $W_{NW} = 30$ nm at $V_{gs} = 1$ V and at V_{ds} from 1 to 4 V. Color scale: temperature difference (ΔT) in kelvin. The drain side is heated at high V_{ds} by ballistic electrons, indicating that electrons travel substantial distance into the contact before reaching equilibrium which indicates near-ballistic transport.

is no longer valid. In our near-ballistic InGaAs GAA MOSFETs, electrons encounter less scattering at smaller L_{ch} during transport from source to drain. Therefore, scattering-induced mobility fluctuation decreases at small L_{ch}, so that the normalized I_s noise is reduced at small L_{ch} comparing with the prediction of classical theory. This property also confirms that mobility fluctuation is the origin of low-frequency for highly scaled InGaAs MOSFETs. To confirm the transport property of the devices, an ultrafast high resolution thermoreflectance imaging technique is applied to image the local surface temperature of the InGaAs GAA devices [41]. Fig. 11 shows the top-view thermoreflectance image on an InGaAs GAA MOSFET with $L_{ch} = 80$ nm, $W_{NW} = 30$ nm at $V_{gs} = 1$ V, and V_{ds} varying from 0 to 4 V. The drain side is heated at high V_{ds} by ballistic electrons, indicating that electrons travel substantial distance into the drain contact before reaching equilibrium with the lattice. It supports the conclusion of Figs. 9 and 10 that InGaAs GAA MOSFETs in this paper are near-ballistic. Hot carrier injection (HCI) measurement on Sample C shows HCI degradation is weakly dependent on L_{ch} because less electrons would interact with interface and oxide at the end of channel. It further confirms the near-ballistic transport in the devices as we reported in [12].

To further understand the low-frequency noise behavior in near-ballistic MOSFETs, low-frequency noise is theoretically studied in ballistic transistors. In principle, in a ballistic MOSFET, electrons transport from source to drain without any scattering processes, and then equilibrate to lattice temperature at drain contact. Therefore, mobility fluctuation will not happen inside the channel of ballistic transistors. There have been theoretical and experimental study on long-channel carbon nanotube ballistic transistor [42], [43]. Carrier number fluctuation is proposed to dominate the 1/f noise in the long-channel (600 nm) carbon nanotube transistors because the large number of defects inside the gate oxide. However, this theory will not be applied in the short channel III–V MOSFETs because the highly scaled channel length make it impossible to have enough number of defects in gate oxide to have a 1/f noise spectrum. In this paper, low-frequency noise in ballistic transistors with no trapping and detrapping events in gate oxide is studied. In ideal case, if there are no active defects meanwhile no scattering process inside channel, there will be no current fluctuation with fixed V_{gs} and V_{ds} in an ideal ballistic transistor. However, as series resistance (R_{SD}) exists in every transistor and resistor noise also has a 1/f noise spectrum, current fluctuation from series resistor is one of the noise sources in ballistic transistors. The noise originating from source and drain (S/D) resistances can be modeled as the combination of mobility fluctuation noise and thermal noise. Thermal noise can be negligible in low-frequency noise analysis because it is independent of frequency in noise spectrum. As R_{SD} is fluctuated, the V_{gs} and V_{ds} of the ballistic transistor will also be fluctuating. Thus, it is important to understand the effect of R_{SD} on the low-frequency noise of ballistic transistors. If we consider S/D resistance and ballistic transistor together, the total source current PSD can be expressed as [23]

$$S_{I_s} = \frac{S_{I_{ch}} + g_{ch}^2 R_D^2 S_{I_{R_D}} + R_S^2 (g_m + g_{ch})^2 S_{I_{R_S}}}{[1 + g_m R_S + g_{ch}(R_S + R_D)]^2} \tag{1}$$

where S_{Ich} is the source current PSD inside channel, S_{IRD} is the source current PSD in drain series resistance (R_D), S_{IRS} is the source current PSD in source series resistance (R_S), g_{ch} is the channel conductance, and g_m is the transconductance. If we consider ballistic transistor and symmetric S/D so that $S_{Ich} = 0$, $R_S = R_D = R_{SD}/2$, and $S_{IRS} = S_{IRD} = 2S_{IRSD}$, (1) becomes

$$S_{I_s} = \frac{R_{SD}^2\left[g_{ch}^2 + (g_m + g_{ch})^2\right] S_{I_{R_{SD}}}}{2\left[1 + (g_m + 2g_{ch})R_{SD}/2\right]^2} = A S_{I_{R_{SD}}} = \frac{A\alpha_H I_s^2}{fN} \tag{2a}$$

$$A = \frac{R_{SD}^2\left[g_{ch}^2 + (g_m + g_{ch})^2\right]}{2\left[1 + (g_m + 2g_{ch})R_{SD}/2\right]^2} \tag{2b}$$

$$\frac{S_{I_s}}{I_s^2} = \frac{A\alpha_H}{fN} \tag{2c}$$

where we consider $S_{IRSD} = \alpha_H I_s^2/fN$, α_H is the Hooge parameter, and N is the number of carriers in S/D region [40]. Thus, in ballistic transistors, S_{Is}/I_s^2 will be independent of L_{ch}. If $(g_m + 2g_{ch})R_{SD}/2 \gg 1$, S_{Is}/I_s^2 is independent of I_s to the zeroth-order approximation. If $(g_m + 2g_{ch})R_{SD}/2 \ll 1$, S_{Is}/I_s^2 has a positive correlation with I_s. Fig. 12 shows the relation between S_{Is}/I_s^2 and I_s/V_{ds} in an InGaAs GAA MOSFETs with $L_{ch} = 20$ nm, $W_{NW} = 25$ nm, and at V_{ds} from 0.1 to 0.5 V. S_{Is}/I_s^2 is plotted versus I_s/V_{ds} because S_{Is}/I_s^2 is inversely proportional to I_s/V_{ds} in mobility fluctuation model of MOSFETs [23]. S_{Is}/I_s^2 shows weaker negative correlation with I_s/V_{ds} as V_{ds} increases. This phenomenon suggests noise from series resistance has a higher contribution to the source current noise as V_{ds} increases. In near-ballistic transistors, ballistic efficiency at high V_{ds} increases which reduces the noise from the channel, so that low-frequency noise depends more on the series resistance.

Classical number fluctuation and mobility fluctuation theories were set up based on diffusive transport assumption. In diffusive assumption, electrons are in thermal-equilibrium while in ballistic transistors, electron transport is a nonequilibrium process. In particular, electron equilibrate to the lattice

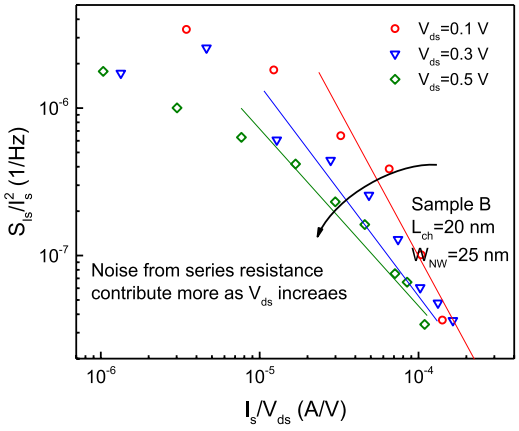

Fig. 12. S_{Is}/I_s^2 versus I_s/V_{ds} at different V_{ds}. S_{Is}/I_s^2 shows weaker negative correlation with I_s/V_{ds} as V_{ds} increases. This phenomenon suggests noise from series resistance has a higher contribution to the source current noise as V_{ds} increases.

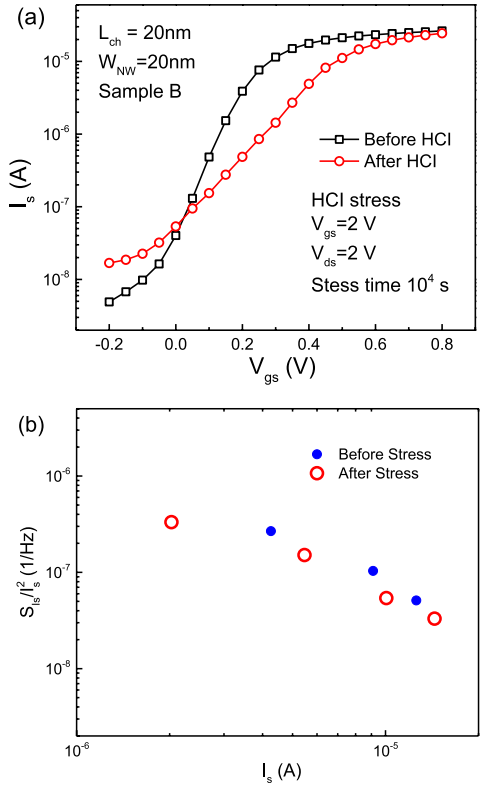

Fig. 13. (a) Transfer characteristics of an $L_{ch} = 20$ nm, $W_{NW} = 20$ nm device of Sample B, fresh device (square) and after $V_{gs} = 24$ V, and $V_{ds} = 2$ V stress for 10^4 s (circle). (b) S_{Is}/I_s^2 versus I_s/V_{ds} of the device in (a) before stress and after stress measured at $V_{ds} = 0.05$ V. Although defects are generated at drain side, the PSD of I_s shows similar level on fresh device and stressed device.

temperature at drain side. We should identify that if this nonequilibrium process is the source of 1/f noise in the near-ballistic transistors. To achieve this goal, noise measurement is performed before and after HCI stress. The HCI degradation study on InGaAs GAA MOSFETs suggests that the maximum damage condition is at $V_{gs} \sim V_{ds}$ [12]. In this paper, $V_{gs} = 2$ V and $V_{ds} = 2$ V are applied as HCI stress for 10^4 s to generate defects by the injection of hot electrons into drain side.

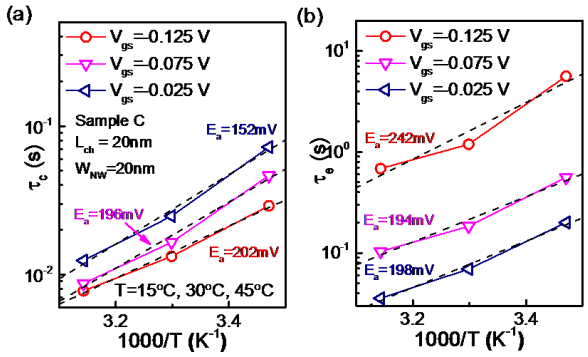

Fig. 14. Temperature dependent (a) capture and (b) emission time constant of RTN in device shown in Fig. 3.

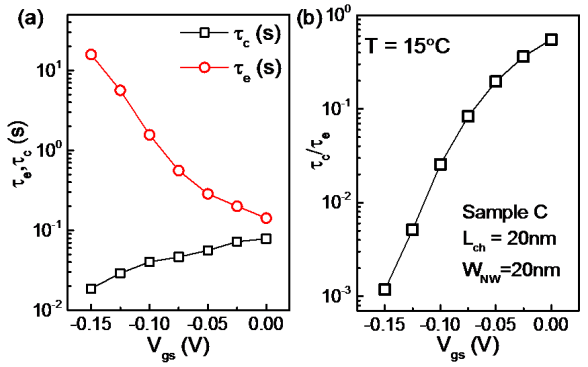

Fig. 15. (a) Mean capture and emission time constant corresponding to different gate voltages. (b) τ_c/τ_e dependence on V_{gs}. The positive correlation indicates electron trapping happens between channel and gate oxide.

The generated defects will interact with electrons in the relaxation process at drain side. Fig. 13 shows transfer characteristics and S_{Is}/I_s^2 versus I_s of an InGaAs GAA MOSFET before and after HCI stress. The PSD of I_s shows similar level on fresh device and stressed device, indicating the relaxation of electrons at drain side is not the source of 1/f noise.

In Figs. 14 and 15, the time domain characteristics of RTN in the same condition as in Fig. 3 from $V_{gs} = -0.15$ to 0 V are studied. Capture time constant (τ_c) is defined as time duration in the lower state, while emission time constant (τ_e) is defined as time duration in the higher state, as shown in Fig. 3(a). Fig. 14 shows the relation between time constants and the reciprocal of temperature (1000/T). τ_c and τ_e are extracted at 15 °C, 30 °C, and 45 °C and the activation energy (E_a) is extracted by linear extrapolation of $\ln(\tau_c$ or $\tau_e)$ versus $1/k_BT$, where k_B is the Boltzmann constant. Both τ_c and τ_e are reduced by increasing the temperature, suggesting thermal emission contributes to the trapping and detrapping event in $LaAlO_3$/InGaAs or Al_2O_3/InGaAs systems. Fig. 15(a) shows the relation between τ_c, τ_e, and V_{gs}. Fig. 15(b) studies the relation between τ_c/τ_e and V_{gs}. The positive correlation between τ_c/τ_e and V_{gs} indicates electrons trapping and detrapping happen between channel and gate oxide rather than between gate metal and gate oxide, as suggested in [21].

IV. Conclusion

Low-frequency noise and RTN in highly scaled InGaAs GAA MOSFETs are systematically studied. For highly scaled InGaAs GAA MOSFETs, both number fluctuation and mobility fluctuation exist in the low frequency current fluctuation. Noise from number fluctuation typically is RTN because the lack of defects to support a 1/f spectrum. Mobility fluctuation is confirmed to be the source of 1/f noise of devices without RTN or at high V_{gs}. It is experimentally observed that low-frequency noise is suppressed at shorter channel length due to the near-ballistic transport at this length scale. The short channel length, long mean free path (high mobility), and volume inversion nature of InGaAs GAA structure are believed to be the origin of the noise reduction in the devices of this paper. The reduced low-frequency noise in highly scaled InGaAs MOSFETs suggests their potential for low noise MOSFET applications. Low-frequency noise is also studied in ballistic transistors and series resistance plays an important role in the low-frequency noise of ballistic transistors with negligible oxide defects. RTN is observed on top-down InGaAs GAA MOSFETs and only around threshold voltage because RTN is negligible comparing with mobility fluctuation induced noise at high V_{gs}.

Acknowledgment

The authors would like to thank X. Wang, X. B. Lou, and R. G. Gordon for the technical support on device fabrications.

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