

# High-Performance Atomic-Layer-Deposited Indium Oxide 3-D Transistors and Integrated Circuits for Monolithic 3-D Integration

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**Abstract**—In this work, we report the experimental demonstration of  $\text{In}_2\text{O}_3$  3-D transistors coated on fin structures and integrated circuits by a back-end-of-line (BEOL) compatible atomic layer deposition (ALD) process. High-performance planar back-gate  $\text{In}_2\text{O}_3$  transistors with high mobility of  $113 \text{ cm}^2/\text{V}\cdot\text{s}$  and high maximum drain current ( $I_D$ ) of  $2.5 \text{ mA}/\mu\text{m}$  are achieved by channel thickness engineering and postdeposition annealing. The high-performance ALD  $\text{In}_2\text{O}_3$ -based zero- $V_{GS}$ -load inverter is demonstrated with a maximum voltage gain of 38 V/V and a minimum supply voltage ( $V_{DD}$ ) down to 0.5 V. Top-gate indium oxide ( $\text{In}_2\text{O}_3$ ) transistors by low-temperature ALD of both gate insulator and channel semiconductor are also demonstrated with  $I_D$  of  $570 \mu\text{A}/\mu\text{m}$  and low subthreshold slope (SS) down to 84.6 mV/decade. ALD  $\text{In}_2\text{O}_3$  3-D Fin transistors with the top-gate structure are then demonstrated, benefiting from the conformal deposition capability of ALD. These results suggest that ALD oxide semiconductors and devices have unique advantages and are promising toward BEOL-compatible monolithic 3-D integration for 3-D integrated circuits.

**Index Terms**—3-D structure, atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, indium oxide, oxide semiconductor, thin-film transistor.

## I. INTRODUCTION

OXIDE semiconductors are the leading semiconducting channel materials for flat-panel display applications [1], [2]. Recently, indium oxide ( $\text{In}_2\text{O}_3$ ) or doped- $\text{In}_2\text{O}_3$ , such

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as (indium gallium zinc oxide, IGZO), are being investigated as promising channel materials for back-end-of-line (BEOL) compatible transistors for monolithic 3-D integration [3], by both sputtering [4]–[13] and atomic layer deposition (ALD) [14]–[18], due to their high mobility, wide bandgap, low variability, and high stability. ALD-based oxide semiconductors [19]–[23] are of special interest due to the atomically smooth surface, ultrathin thickness, and the capability of conformal deposition on 3-D structures. Recently, high-performance back-gate ALD  $\text{In}_2\text{O}_3$  transistors have been demonstrated with a high drain current over  $2 \text{ mA}/\mu\text{m}$  in both depletion-mode (D-mode) and enhancement-mode (E-mode) operations [15], [16]. The devices have ultrascaled channel thickness ( $T_{ch}$ ) down to 0.7 nm, channel length down ( $L_{ch}$ ) to 40 nm, low thermal budget below 400 °C, and stability in the  $\text{H}_2$  environment, which are highly compatible with the BEOL process. Meanwhile, for many practical applications, a top-gate device structure is required for integrated circuits and other applications. However, how to form high-quality gate dielectric on top of ALD  $\text{In}_2\text{O}_3$  and how to realize high-performance top-gate ALD  $\text{In}_2\text{O}_3$  transistors remain unclear.

In this work, the performance of back-gate ALD  $\text{In}_2\text{O}_3$  transistors is further enhanced by  $T_{ch}$  engineering and post-deposition annealing. An optimized  $T_{ch}$  is determined to be 2.2–2.5 nm, achieving record high mobility of  $113 \text{ cm}^2/\text{V}\cdot\text{s}$  and record-high maximum drain current of  $2.5 \text{ mA}/\mu\text{m}$  at  $L_{ch}$  of 40 nm and  $V_{DS} = 0.7 \text{ V}$ . The high-performance back-gate ALD  $\text{In}_2\text{O}_3$  transistors-based zero- $V_{GS}$ -load inverter is demonstrated with a maximum voltage gain of 38 V/V and a minimum supply voltage ( $V_{DD}$ ) down to 0.5 V. Top-gate  $\text{In}_2\text{O}_3$  transistors are also demonstrated by low-temperature ALD of both gate insulator and channel semiconductor. High-performance top-gate  $\text{In}_2\text{O}_3$  transistors are realized with a maximum drain current ( $I_D$ ) of  $570 \mu\text{A}/\mu\text{m}$  and a low subthreshold slope (SS) down to 84.6 mV/decade. It is found that the deposition of hafnium oxide ( $\text{HfO}_2$ ) as gate insulator at low temperature and postdeposition annealing in  $\text{O}_2$  at low temperature are critical to annihilate defects that are generated during the formation of top dielectrics and top-gate electrodes. ALD  $\text{In}_2\text{O}_3$  3-D Fin transistors with top-gate structures coated on  $\text{SiO}_2$  fin structures are also demonstrated for the first time, taking advantage of conformal deposition of ALD on 3-D structures.

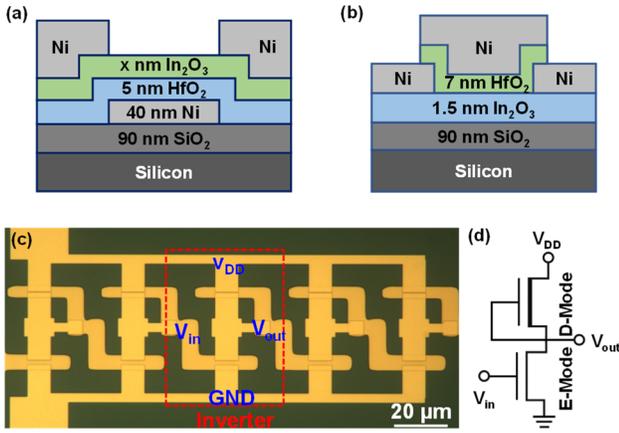


Fig. 1. Schematic of a planar  $\text{In}_2\text{O}_3$  transistor with (a) back-gate and (b) top-gate structures. (c) Photograph image of an  $\text{In}_2\text{O}_3$  zero- $V_{\text{GS}}$ -load inverter in a five-stage ring oscillator. (d) Circuit diagram of a zero- $V_{\text{GS}}$ -load inverter.

## II. EXPERIMENTS

Fig. 1 presents the schematic of planar (a) back-gate and (b) top-gate  $\text{In}_2\text{O}_3$  transistors. The back-gate device structure is similar to previously reported in [15] and [16], which is used for circuit demonstration. The gate-stack consists of 40-nm Ni as gate metal, 5-nm  $\text{HfO}_2$  as gate dielectric, 0.5–3.5-nm  $\text{In}_2\text{O}_3$  as semiconducting channels, and 80-nm Ni as source/drain electrodes. The device fabrication process is similar to [15] and [16]. The fabricated devices were annealed in  $\text{O}_2$ ,  $\text{N}_2$ , or forming gas (FG, 96%  $\text{N}_2/4\%$   $\text{H}_2$ ) for 30 s at different temperatures from 250 °C to 350 °C according to the optimized annealing conditions achieved in [15]. Fig. 1(c) shows the photograph of a fabricated  $\text{In}_2\text{O}_3$  zero- $V_{\text{GS}}$ -load inverter in a five-stage ring oscillator. The circuit diagram of the  $\text{In}_2\text{O}_3$  zero- $V_{\text{GS}}$ -load inverter is shown in Fig. 1(d). D-mode and E-mode transistors could be achieved by threshold voltage ( $V_{\text{T}}$ ) engineering, such as plasma treatment described in [17]. The E-mode device has a channel length ( $L_{\text{ch}}$ ) of 2  $\mu\text{m}$ , while  $L_{\text{ch}}$  of D-mode devices ( $L_{\text{D}}$ ) varies from 0.1 to 0.3  $\mu\text{m}$  to engineer the load resistance.

The gate-stack of planar top-gate  $\text{In}_2\text{O}_3$  transistors, as shown in Fig. 1(b), includes 40-nm Ni as gate metal, 7-nm  $\text{HfO}_2$  as gate dielectric, 1.5-nm  $\text{In}_2\text{O}_3$  as the semiconducting channel, and 40-nm Ni as source/drain electrodes. The device fabrication starts with a standard cleaning of 90-nm  $\text{SiO}_2/\text{p}^+\text{Si}$  substrates. The 1.5-nm-thick  $\text{In}_2\text{O}_3$  films were then deposited by ALD at 225 °C, using  $(\text{CH}_3)_3\text{In}$  (TMIn) and  $\text{H}_2\text{O}$  as In and O precursors. Channel isolation was done by wet etching use concentrated HCl. The 40-nm Ni was then deposited by e-beam evaporation as S/D contacts. Then,  $\text{HfO}_2$  was deposited by ALD at various temperatures of 120 °C/150 °C/200 °C, using  $[(\text{CH}_3)_2\text{N}]_4\text{Hf}$  (TDMAHf) and  $\text{H}_2\text{O}$  as Hf and O precursors. The impact of ALD deposition temperature is discussed in great detail in the following section. The fabricated devices were annealed by rapid thermal annealing (RTA) in  $\text{O}_2$  at different temperatures. 3-D Fin transistors with top-gate structures were fabricated on a  $\text{SiO}_2/\text{Si}$  substrate with  $\text{SiO}_2$  fin structures. The top-gate dielectric of

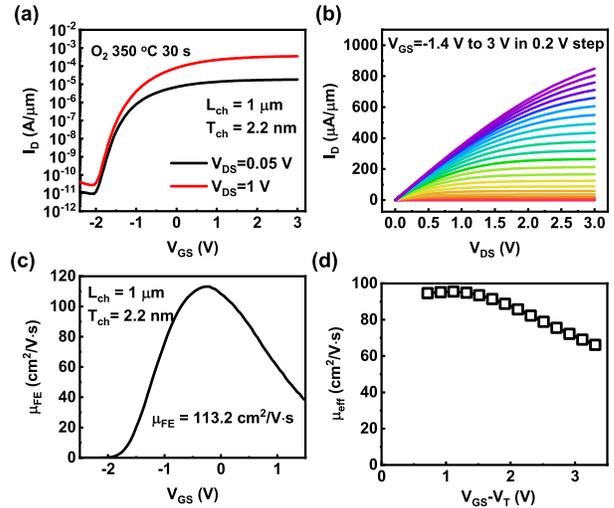


Fig. 2. (a)  $I_{\text{D}}-V_{\text{GS}}$  and (b)  $I_{\text{D}}-V_{\text{DS}}$  characteristics of a planar back-gate  $\text{In}_2\text{O}_3$  transistor with  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and  $T_{\text{ch}}$  of 2.2 nm with  $\text{O}_2$  annealing at 350 °C for 30 s. (c)  $\mu_{\text{FE}}$  versus  $V_{\text{GS}}$  extracted from the maximum  $g_{\text{m}}$  at  $V_{\text{DS}}$  of 0.05 V from the transfer curve. (d)  $\mu_{\text{eff}}$  versus  $V_{\text{GS}}$  extracted from the  $g_{\text{d}}$  from the output curve.

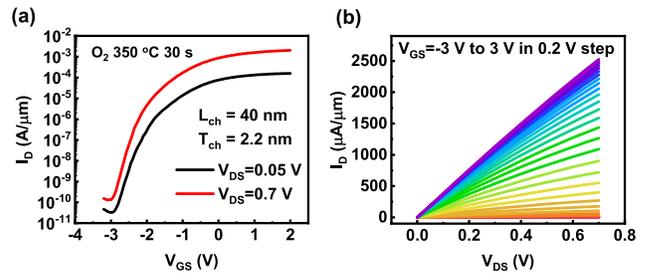


Fig. 3. (a)  $I_{\text{D}}-V_{\text{GS}}$  and (b)  $I_{\text{D}}-V_{\text{DS}}$  characteristics of a planar back-gate  $\text{In}_2\text{O}_3$  transistor with  $L_{\text{ch}}$  of 40 nm and  $T_{\text{ch}}$  of 2.2 nm with  $\text{O}_2$  annealing at 350 °C.

7-nm  $\text{HfO}_2$  was formed by low-temperature ALD at 120 °C, which is critical to form top-gate devices.

## III. RESULTS AND DISCUSSION

Fig. 2(a) shows the  $I_{\text{D}}-V_{\text{GS}}$  characteristics of a planar  $\text{In}_2\text{O}_3$  transistor with  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and  $T_{\text{ch}}$  of 2.2 nm with  $\text{O}_2$  annealing at 350 °C for 30 s. Fig. 2(b) shows the corresponding  $I_{\text{D}}-V_{\text{DS}}$  characteristics of the same device, exhibiting high maximum  $I_{\text{D}}$  of 850  $\mu\text{A}/\mu\text{m}$  even with  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and well-behaved drain current saturation at high  $V_{\text{DS}}$ . Such high  $I_{\text{D}}$  is the result of high field-effect mobility ( $\mu_{\text{FE}}$ ) of 113  $\text{cm}^2/\text{V}\cdot\text{s}$ , as shown in Fig. 2(c), extracted from the maximum transconductance ( $g_{\text{m}}$ ) at  $V_{\text{DS}}$  of 0.05 V. Effective mobility ( $\mu_{\text{eff}}$ ) versus  $V_{\text{GS}}$  extracted from drain conductance ( $g_{\text{d}}$ ) are presented in Fig. 2(d), which is consistent with  $\mu_{\text{FE}}$ . Fig. 3(a) and (b) presents the  $I_{\text{D}}-V_{\text{GS}}$  and  $I_{\text{D}}-V_{\text{DS}}$  characteristics of an  $\text{In}_2\text{O}_3$  transistor with  $L_{\text{ch}}$  of 40 nm and  $T_{\text{ch}}$  of 2.2 nm, exhibiting a high maximum  $I_{\text{D}}$  of 2.5  $\text{mA}/\mu\text{m}$  under  $V_{\text{DS}} = 0.7$  V and  $V_{\text{GS}} - V_{\text{T}} = 4$  V with optimized  $T_{\text{ch}}$  and annealing conditions. Further dielectric scaling is needed to realize  $V_{\text{GS}} - V_{\text{T}}$  approaching  $V_{\text{DS}}$ .

The mobility of  $\text{In}_2\text{O}_3$  in this work is significantly improved compared to other ALD-based oxide

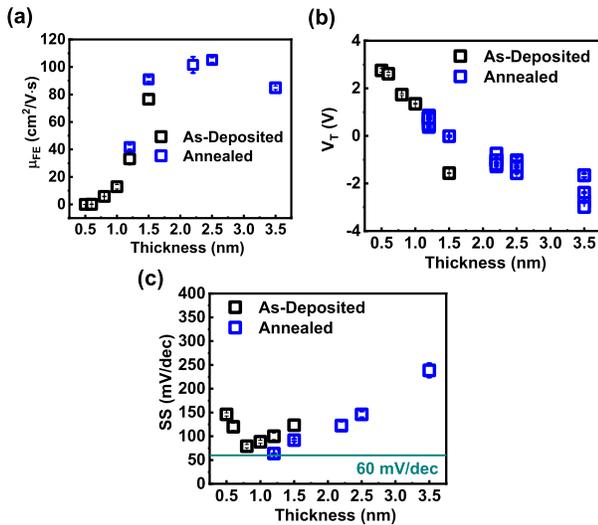


Fig. 4. (a)  $\mu_{FE}$ , (b)  $V_T$ , and (c) SS versus  $T_{ch}$  extracted from as-deposited devices and devices with optimized annealing conditions.

semiconductors [19]–[23]. Such high mobility is achieved by  $T_{ch}$  engineering and postdeposition annealing, as shown in Fig. 4(a). Average  $\mu_{FE} > 100$  cm<sup>2</sup>/V·s is achieved with  $T_{ch}$  of 2.2–2.5 nm at optimized annealing conditions.  $\mu_{FE}$  decreases rapidly with  $T_{ch}$  below 1 nm, most likely due to the enhanced surface scattering and quantum confinement effect on the band structure [14].  $\mu_{FE}$  decreases at  $T_{ch}$  above 3 nm due to the higher carrier concentration and weaker gate electrostatic control, as also shown in  $V_T$  versus  $T_{ch}$  in Fig. 4(b). Postdeposition annealing for the reduction of oxygen vacancies in as-deposited films is needed to tune  $V_T$  of devices with  $T_{ch}$  above 2 nm to obtain a sufficiently high on/off ratio.  $V_T$  of devices with certain  $T_{ch}$  can be controlled by annealing conditions, as shown in Fig. 4(b). Fig. 4(c) shows  $T_{ch}$ -dependent SS extracted from as-deposited devices and devices with optimized annealing conditions, exhibiting SS close to the thermal limit of 60 mV/decade at room temperature at  $T_{ch} \sim 1$  nm. The thickness-dependent SS indicates that the interface trap density  $D_{it}$  in the subthreshold region may be related to  $T_{ch}$ . However, the atomic configuration at the oxide/semiconductor interface does not have a  $T_{ch}$  dependence. Thus, the defect energy levels should not change with respect to the vacuum level. Therefore, the only possible reason is that the band structure of In<sub>2</sub>O<sub>3</sub> is changing with  $T_{ch}$  (such as  $T_{ch}$ -dependent conduction band minimum,  $E_C$ ) so that the Fermi level ( $E_F$ ) alignment at the subthreshold region is changing. This result is consistent with previous theoretical analysis and density function theory (DFT) simulations [14].

Fig. 5(a) presents  $V_{out}$  versus  $V_{in}$  curve of an In<sub>2</sub>O<sub>3</sub> zero- $V_{GS}$ -load inverter with  $L_D$  of 0.3  $\mu$ m at different  $V_{DD}$ 's from 2 down to 0.5 V, showing well-behaved voltage transfer characteristics. The voltage gains are given in Fig. 5(b), achieving a maximum voltage gain of 38 V/V at  $V_{DD}$  of 2 V. The midpoint voltage of the In<sub>2</sub>O<sub>3</sub> zero- $V_{GS}$ -load inverter can be engineered by tuning the load resistance and varying the channel length of the D-mode transistor, as illustrated in Fig. 5(c), providing the essential approach for  $V_{DD}$  and midpoint voltage

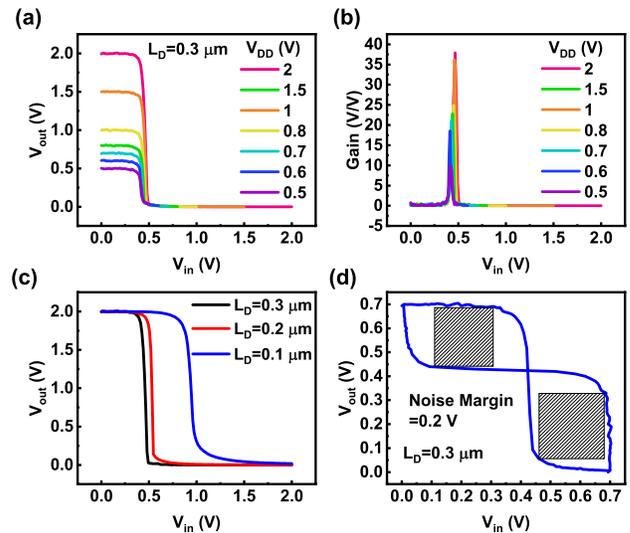


Fig. 5. (a)  $V_{out}$  versus  $V_{in}$  and (b) voltage gain of an In<sub>2</sub>O<sub>3</sub> zero- $V_{GS}$ -load inverter with  $L_D$  of 0.3  $\mu$ m at different  $V_{DD}$ 's. (c)  $V_{out}$  versus  $V_{in}$  of In<sub>2</sub>O<sub>3</sub> zero- $V_{GS}$ -load inverters with different  $L_D$ 's at  $V_{DD}$  of 2 V. (d) NM of the In<sub>2</sub>O<sub>3</sub> zero- $V_{GS}$ -load inverter as in (a) at  $V_{DD}$  of 0.7 V.

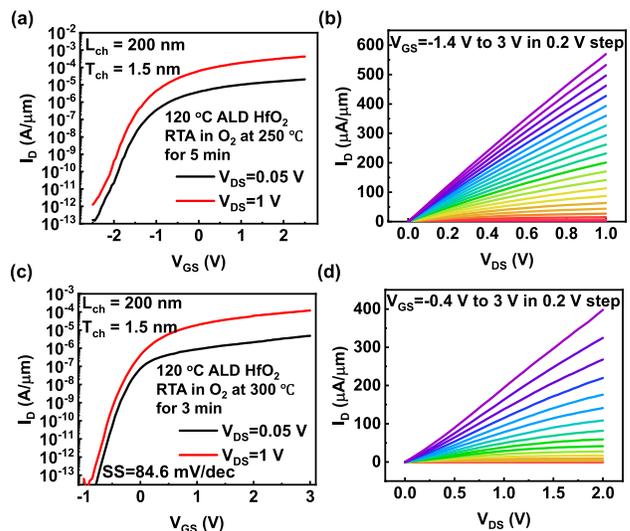


Fig. 6. (a)  $I_D$ - $V_{GS}$  and (b)  $I_D$ - $V_{DS}$  characteristics of a top-gate In<sub>2</sub>O<sub>3</sub> transistor with  $L_{ch}$  of 200 nm,  $T_{ch}$  of 1.5 nm, 7-nm HfO<sub>2</sub> by ALD at 120 °C, and with RTA in O<sub>2</sub> at 250 °C for 5 min. (c)  $I_D$ - $V_{GS}$  and (d)  $I_D$ - $V_{DS}$  characteristics of a top-gate In<sub>2</sub>O<sub>3</sub> transistor with  $L_{ch}$  of 200 nm,  $T_{ch}$  of 1.5 nm, 7-nm HfO<sub>2</sub> by ALD at 120 °C, and with RTA in O<sub>2</sub> at 300 °C for 3 min.

engineering accordingly. Therefore, a sufficiently large noise margin (NM) can be achieved at a low  $V_{DD}$  of 0.7 V, as shown in Fig. 5(d).

Fig. 6(a) and (b) shows the  $I_D$ - $V_{GS}$  and  $I_D$ - $V_{DS}$  characteristics of a top-gate In<sub>2</sub>O<sub>3</sub> transistor with  $L_{ch}$  of 200 nm and  $T_{ch}$  of 1.5 nm. The HfO<sub>2</sub> gate dielectric in this device was deposited at 120 °C, and the device was annealed by RTA in O<sub>2</sub> at 250 °C for 5 min. The device exhibits well-behaved switching on and off characteristics, with a maximum  $I_D$  of 570  $\mu$ A/ $\mu$ m. Fig. 6(c) and (d) shows the  $I_D$ - $V_{GS}$  and  $I_D$ - $V_{DS}$  characteristics of a top-gate In<sub>2</sub>O<sub>3</sub> transistor with  $L_{ch}$  of 200 nm,  $T_{ch}$  of 1.5 nm, and with HfO<sub>2</sub> gate dielectric deposited at 120 °C and annealed by RTA in O<sub>2</sub> at 300 °C

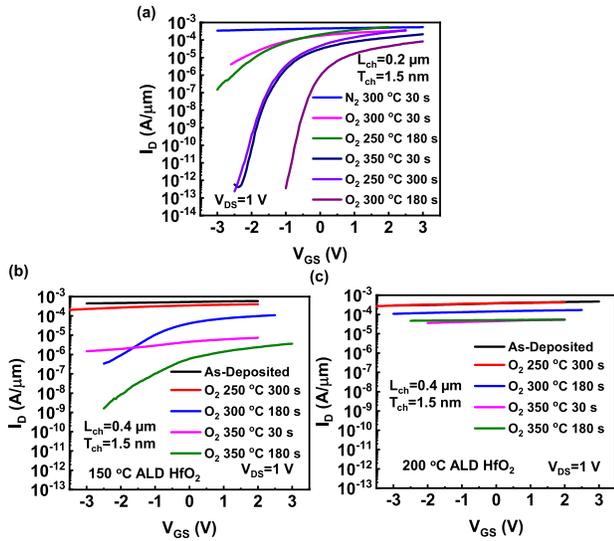


Fig. 7. (a)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS}$  of 1 V of top-gate  $\text{In}_2\text{O}_3$  transistors with different annealing conditions.  $I_D$ - $V_{GS}$  at  $V_{DS}$  of 1 V of top-gate  $\text{In}_2\text{O}_3$  transistors with different annealing conditions with  $\text{HfO}_2$  gate oxide deposited by ALD at 120 °C, (b) 150 °C, and (c) 200 °C.

for 3 min. This device has a maximum  $I_D$  of 397  $\mu\text{A}/\mu\text{m}$  and SS of 84.6 mV/decade. The small SS at the subthreshold region indicates a high-quality oxide/semiconductor interface. The interface trap density  $D_{it}$  at the sub-threshold region is estimated to be  $\sim 5\text{-}6 \times 10^{12}/\text{cm}^2$  eV.  $D_{it}$  at the  $\text{HfO}_2/\text{In}_2\text{O}_3$  interface in a top-gate device is much larger than that in a back-gate device. The main difficulty for the integration of top-gate on the ALD  $\text{In}_2\text{O}_3$  channel is from the ALD  $\text{HfO}_2$  process. Hf-O bond with dissociation energy of 801 kJ/mol is much more stable compared to the In-O bond of 346 kJ/mol. ALD of  $\text{HfO}_2$  on  $\text{In}_2\text{O}_3$  generates more O vacancies in  $\text{In}_2\text{O}_3$  and induces much more charge density. Meanwhile, it also degrades  $\text{In}_2\text{O}_3$  film and  $\text{HfO}_2/\text{In}_2\text{O}_3$  interface quality. Appropriate  $\text{O}_2$  annealing can fill these O vacancies and heal most of the defects from the process so that SS of top-gate devices can be improved. To further improve the oxide/semiconductor interface quality, a top gate oxide or interfacial layer with low bond dissociation energy is preferred, and a lower interface trap density may be achieved. For example, Al-O has dissociation energy of 512 kJ/mol, and Mg-O has dissociation energy of 394 kJ/mol.

Fig. 7(a) shows the transfer characteristics at  $V_{DS}$  of 1 V of top-gate  $\text{In}_2\text{O}_3$  transistors with different annealing conditions where the ALD  $\text{HfO}_2$  was grown at 120 °C. As-fabricated devices, without annealing or devices annealed in the  $\text{N}_2$  environment, cannot be turned off, the reason why these devices cannot be turned off is not just due to the high carrier density because the drain current density here is smaller than previous reported values in devices with similar dimensions [15]. Thus, the poor switching characteristics are also partly due to the high trap density at the  $\text{HfO}_2/\text{In}_2\text{O}_3$  interface, which is generated during the ALD  $\text{HfO}_2$  process. Devices annealed in  $\text{O}_2$  show well-behaved switching on/off characteristics, suggesting that  $\text{O}_2$  is necessary to heal these defects, also indicating that these defects are likely to be O deficiencies.

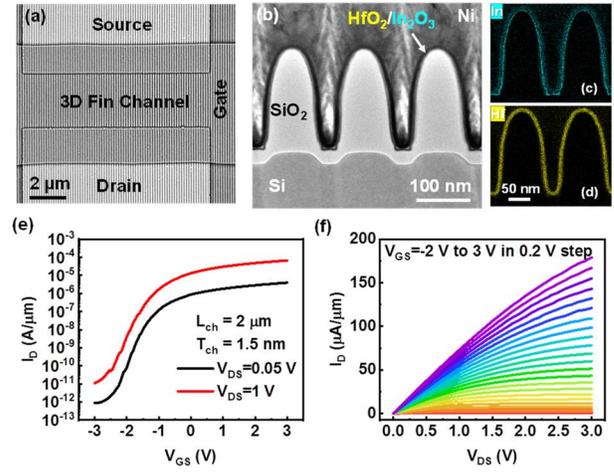


Fig. 8. (a) SEM image of an  $\text{In}_2\text{O}_3$  3-D Fin transistor with top-gate structure.  $\text{SiO}_2$  fin structures were fabricated by SEMATECH. (b) TEM image of a new type of 3-D Fin transistor with top-gate structure and  $\text{In}_2\text{O}_3$  channel. EDX mapping under HAADF STEM of (c) In and (d) Hf, showing the conformal coating around the fin structure by ALD. (e)  $I_D$ - $V_{GS}$  and (f)  $I_D$ - $V_{DS}$  characteristics of an  $\text{In}_2\text{O}_3$  3-D Fin transistor with  $L_{ch}$  of 2  $\mu\text{m}$  and  $T_{ch}$  of 1.5 nm.

Therefore, from the above experimental observation, it is speculated that the deposition of  $\text{HfO}_2$  by ALD generates defects at the  $\text{HfO}_2/\text{In}_2\text{O}_3$  interface, most likely because the pulse of Hf precursor (TDMAHf) takes oxygen atoms away from  $\text{In}_2\text{O}_3$ , leading to the formation of oxygen vacancies at  $\text{HfO}_2/\text{In}_2\text{O}_3$  interface. Such defects can only be healed in an  $\text{O}_2$  environment by  $\text{O}_2$  annealing. Such a process also depends on the annealing time, as shown in Fig. 7(a). It is also found that devices with  $\text{O}_2$  annealing at 250 °C have higher  $I_D$  than devices with  $\text{O}_2$  annealing at 300 °C with a similar threshold voltage ( $V_T$ ). Therefore, low-temperature  $\text{O}_2$  annealing is preferred to maintain high mobility.

Fig. 7 presents the  $I_D$ - $V_{GS}$  characteristics at  $V_{DS}$  of 1 V of top-gate  $\text{In}_2\text{O}_3$  transistors with  $\text{O}_2$  annealing and with  $\text{HfO}_2$  gate oxide deposited by ALD at (a) 120 °C, (b) 150 °C, and (c) 200 °C. As we can see, the on/off ratio of the devices degrades significantly with higher temperature  $\text{HfO}_2$  ALD process and indicates that much more defects are generated at higher ALD temperature most likely due to the stronger reaction between TDMAHf and  $\text{In}_2\text{O}_3$ . All these detailed experiments offer a consistent picture of the challenge of integration of ALD  $\text{HfO}_2$  on top of  $\text{In}_2\text{O}_3$ .

Fig. 8(a) shows the scanning electron microscopic (SEM) image of an  $\text{In}_2\text{O}_3$  3-D Fin transistor with top-gate structure, capturing the gate metal, source/drain contacts, and the fin structures. Fig. 8(b)-(d) presents the transmission electron microscope (TEM) image and energy-dispersive X-ray spectroscopic (EDX) mapping under high-angle annular dark-field imaging (HAADF) scanning transmission electron microscope (STEM) of an  $\text{In}_2\text{O}_3$  3-D fin transistor. ALD  $\text{In}_2\text{O}_3$  channel with  $T_{ch}$  of 1.5 nm is conformally coated on top of  $\text{SiO}_2$  fin structures with a fin height of 180 nm and a fin pitch of 130 nm, as shown in the EDX element mapping of Hf and In. Fig. 8(e) shows  $I_D$ - $V_{GS}$  characteristics of an  $\text{In}_2\text{O}_3$  3-D Fin transistor with  $L_{ch}$  of 2  $\mu\text{m}$  and  $T_{ch}$  of 1.5 nm, exhibiting well-behaved transfer characteristics. Fig. 8(f) shows the

corresponding  $I_D$ - $V_{DS}$  characteristics with a maximum  $I_D$  of  $180 \mu\text{A}/\mu\text{m}$ , normalized by device width, which is about two times larger than that from its top-gate planar counterpart. The 3-D fin structure provides an effective approach to increase the drive current without increasing the device area. The ultrathin channel thickness and the top-gate non-self-align structure with a large link resistance make  $I_D$  smaller than those from back-gate planar devices.

#### IV. CONCLUSION

In summary, high-performance 3-D Fin transistors and integrated circuits based on BEOL compatible oxide semiconductors by ALD are demonstrated. High mobility of  $113 \text{ cm}^2/\text{V}\cdot\text{s}$  and high maximum drain current of  $2.5 \text{ mA}/\mu\text{m}$  are achieved. The demonstration of 3-D devices and integrated circuits suggests that ALD oxide semiconductors and devices have their unique advantages over sputtering films and are promising toward BEOL-compatible monolithic 3-D integration for 3-D integrated circuits.

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