Total Ionizing Dose (TID) Effects in GaAs MOSFETs With La-Based Epitaxial Gate Dielectrics

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***Abstract*— Epitaxially grown La-based oxide has shown promise as a gate dielectric for GaAs substrate materials with a low interface trap density in the mid to low 10^{11} cm^{-2} eV^{-1} range. Total ionizing dose (TID) effects have been studied on GaAs MOSFETs with Al_2O_3/La_2O_3 and $Al_2O_3/La_{1.8}Y_{0.2}O_3$ gate oxides. Charge trapping mechanisms in GaAs MOSFETs are studied by the AC transconductance dispersion method. Al_2O_3/La_2O_3 gated devices show a combination of electron and hole trapping, whereas $Al_2O_3/La_{1.8}Y_{0.2}O_3$ gated devices show primarily hole trapping.**

***Index Terms*— AC transconductance dispersion method (ACGD), atomic layer epitaxy, border traps, GaAs, La_2O_3, oxide traps.**

I. Introduction

CMOS channels with higher carrier mobility than Si are being intensively studied. GaAs is considered to be one of the promising n-channel materials due to its high electron mobility [1]. Although promising as channel materials, growth of high quality gate oxide with low interface trap density D_{it} on these III-V substrates has always been a challenge [2]. To achieve superior interface and bulk quality, there have been efforts on the epitaxial growth of crystalline oxide on III-V materials, especially GaAs [3]–[4].

Methods previously used for such growth were not commercially viable until 2010, when the growth of epitaxial oxide ($LaLuO_3$) on GaAs by ALD was reported [5]. Compared to ALD-deposited amorphous Al_2O_3, a D_{it} reduction by one order of magnitude was found for $LaLuO_3$, thanks to its crystalline quality. Recently, crystalline $La_{1.8}Y_{0.2}O_3$ and La_2O_3 films have been successfully deposited on GaAs (111)A substrates as gate dielectrics by atomic layer epitaxy (ALE) with high manufacturability, achieving even lower interface-trap density and consequently high electron mobility [6]–[8]. La_2O_3 was found to be lattice-matched with GaAs, leading to excellent interface quality. Epitaxial La_2O_3 insulators provide a lower density of interfacial traps on GaAs (111) than amorphous dielectric materials [6]. $La_{1.8}Y_{0.2}O_3$ and La_2O_3 have k values of 22 and 16 [6]; the dielectric thicknesses in these devices are chosen such that their EOT values are 1nm.

In this paper we report a study of total ionizing dose (TID) effects in GaAs MOSFETs with epitaxially grown crystalline gate oxides incorporating $La_{1.8}Y_{0.2}O_3$ and La_2O_3. AC transconductance measurement on MOSFETs and measurements of TID effects for La_2O_3 based capacitors are also performed to understand charge trapping mechanisms. These results are important for potential space applications of these technologies. Moreover, as the adoption of EUV is being considered for the 7 nm node, radiation emitted by lithographic tools can cause damage to devices during their fabrication. Therefore, radiation hardness will be important for future generations of CMOS devices not only for applications in harsh environments, but also to withstand possible radiation damage from fabrication processes.

II. Devices and Experiments

Fabrication of the MOSFETs is done on GaAs (111) wafers. The (111) interface is chosen because the As-As bond, responsible for Fermi level pinning, is hard to form on this surface. After cleaning the wafers with organic solvents, HCl is used to etch away the native oxide. Before deposition of the oxide passivation, the wafers are treated with 10% ammonium

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sulfide solution. Two different high-k gate stacks have been deposited: $Al_2O_3/La_{1.8}Y_{0.2}O_3$ (Device A) and Al_2O_3/La_2O_3 (Device B). Both the $La_{1.8}Y_{0.2}O_3$ layer and the La_2O_3 layer are crystalline, and epitaxially grown with high interface quality. An Al_2O_3 film is in-situ deposited on top of epitaxial $La_{1.8}Y_2O_3$ and La_2O_3. Details of the deposition process are in [6]. For Device A, 7.5 nm of $La_{1.8}Y_{0.2}O_3$ is deposited by ALE, followed by 6.5 nm of Al_2O_3 serving as a capping layer to prevent La oxide reacting with water in air and/or during the process. For Device B, 4 nm of La_2O_3 is deposited by ALE, followed by 4 nm as a Al_2O_3 capping layer. After the oxide deposition process, two steps of ion implantation (with Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV) are performed for source/drain (S/D) formation. Annealing at 850 °C is done for ion activation. The S/D implanted area is then covered with a Ni/Au/Ge-based metal stack using photolithography, metal deposition, and a lift-off process. Ohmic contact formation is completed by annealing in N_2 ambient. After ohmic contact, gate electrodes are formed using Ni/Au metallization. Further details of the fabrication process can be found in [7]–[8]. Interfacial traps for La-based dielectric layers for MOS transistor applications are in the range of mid to low 10^{11} cm^{-2} eV^{-1} [7]–[8], which is among the lowest reported for III-V based gate dielectrics. Excellent device characteristics are observed on as-processed devices. Mobility and subthreshold swings for La_2O_3 based devices are 1150 cm^2/V.s and 74 mV/dec, respectively [8]. Drain currents up to 376 mA/mm are also obtained, indicating their promise for future high speed electronics [8]. Schematic diagrams and channel cross section TEMs of the MOSFETs under study are shown in Figs. 1(a) and 1(b). MOS capacitors are also fabricated with 8 nm of La_2O_3 deposited on GaAs by ALE, followed by 4 nm of Al_2O_3 as a capping layer.

Devices were irradiated with 10 keV X-rays at a dose rate of 31.5 krad(SiO_2)/min at room temperature with all device terminals grounded. For MOSFETs, radiation-induced threshold voltage shifts (ΔV_{th}) are measured, and for MOS capacitors, radiation-induced flatband shifts (ΔV_{fb}) are monitored from *C-V* curves measured at 10 kHz. The AC transconductance dispersion (ACGD) method is employed to characterize oxide-charge trapping in the two epitaxial gate dielectrics [9]–[11]. AC-G_m is a useful technique for probing traps, especially for scaled transistor structures without body contacts, which inhibits the use of charge pumping.

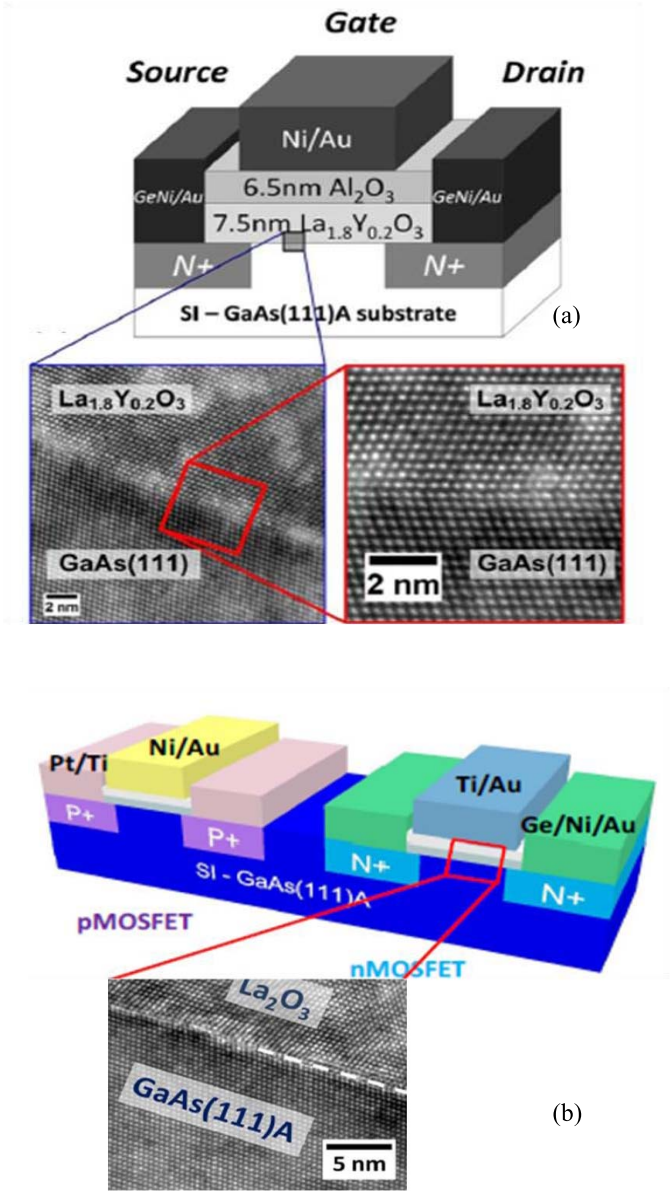

Fig. 1. Schematic representations of GaAs MOSFETs: (a) set-A with $Al_2O_3/La_{1.8}Y_{0.2}O_3$ as gate dielectrics; (b) set-B with Al_2O_3/La_2O_3 gate dielectrics. (After [7], [8])

III. Results and Discussion

A. Comparison between Al_2O_3 /$La_{1.8}Y_{0.2}O_3$ (Device A) and Al_2O_3 /La_2O_3 (Device B) GaAs MOSFETs

Figs. 2(a) and 3(a) show I_d-V_g characteristics for Devices from sets A and B for x-ray doses up to 1000 krad(SiO_2) with 0 V bias applied during irradiation. Figs. 2(b) and 3(b) show radiation-induced V_{th} shifts (ΔV_{th}) for these two types of devices, respectively. Negative ΔV_{th} is observed in Device A for all doses up to 1000 krad(SiO_2), indicating net hole trapping in the high-k gate oxide stack. In Device B, positive ΔV_{th} is observed at low radiation doses (up to $\sim$ 10 krad(SiO_2)), and then negative ΔV_{th} is observed up to 1000 krad(SiO_2), indicating two competing trapping mechanisms, with electron trapping dominating at low doses, and hole trapping becoming dominant at higher doses. This phenomenon was not observed in GaAs or InGaAs MOSFETs with amorphous high-k dielectrics, either in planar or 3D device structures [12].

The magnitude of the ΔV_{th} shift in Device B is discernibly smaller than that in Device A, most likely because: 1) the gate stack in Device B is thinner than that in Device A, and 2) the oxide and interface qualities in Device B are better than those in Device A, because La_2O_3 has a better matched lattice constant to GaAs compared to $La_{1.8}Y_{0.2}O_3$ [8]. Al_2O_3 traps predominantly holes during irradiation [12], which contributes to the negative V_{th} shift in each type of device. La_2O_3 traps electrons during irradiation, which partially offsets the negative V_{th} shift due to Al_2O_3. $La_{1.8}Y_2O_3$ traps holes, adding

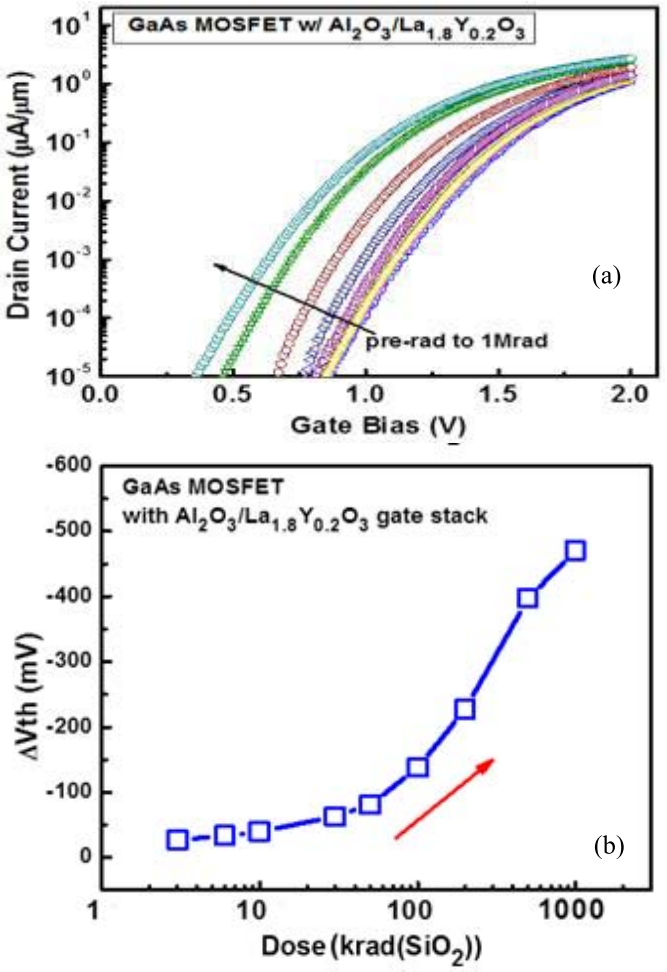

Fig. 2. (a) Shifts of I_d-V_g curves with increasing dose up to 1000 krad(SiO_2); (b) threshold voltage shift (ΔV_{th}) as a function of x-ray dose. Negative V_{th} shift indicates net hole trapping.

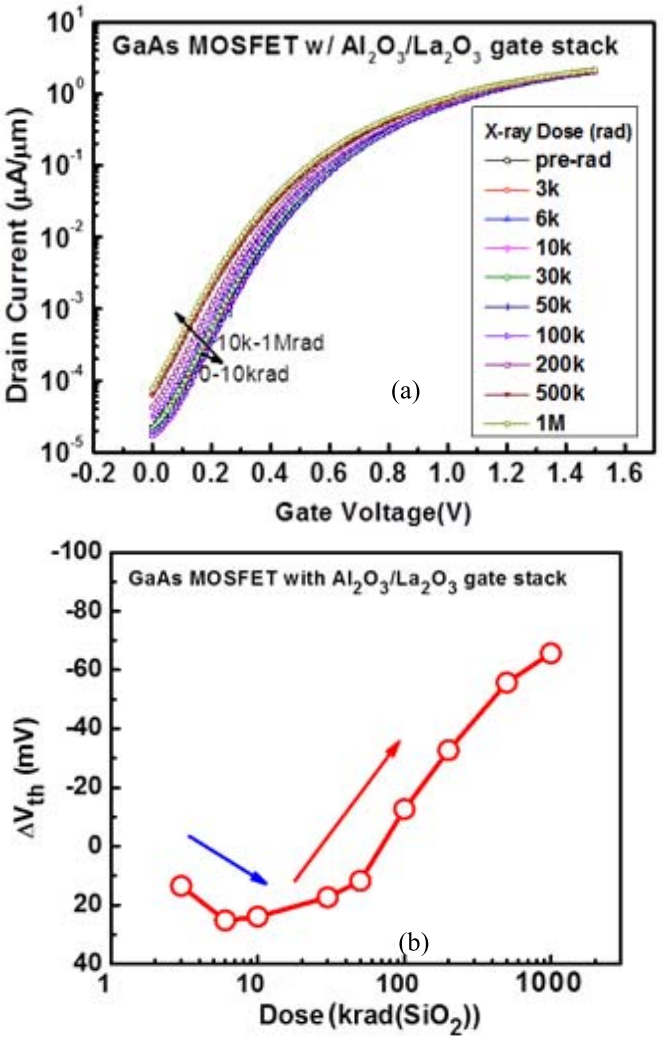

Fig. 3. (a) Shifts of I_d-V_g curves with increasing dose up to 1000 krad(SiO_2); (b) positive-then-negative V_{th} shifts are observed as the dose increases, indicating two trapping mechanisms, electron and hole trapping.

to the negative V_{th} shift caused by trapping in Al_2O_3. Hence, the $La_{1.8}Y_2O_3$ devices show a more negative V_{th} shift than the La_2O_3 devices.

Fig. 4 shows radiation effects on gate leakage for a device with an Al_2O_3/La_2O_3 stack (device B). The gate leakage remains unchanged with increasing dose, indicating the high quality of these gate dielectrics.

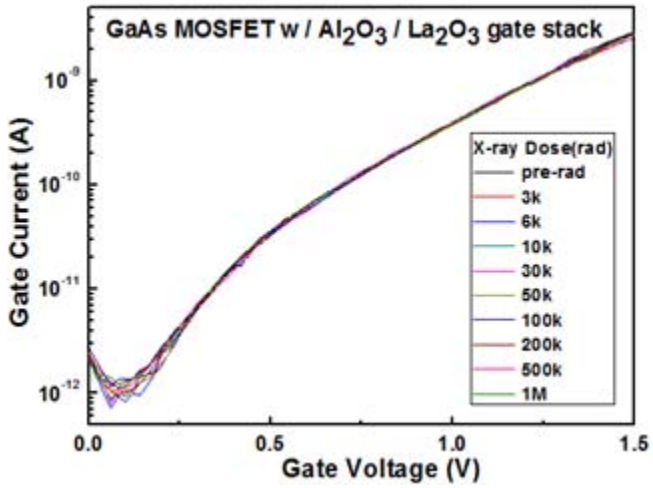

Fig. 4. Gate leakage current vs. gate voltage at $V_{ds} = 50$ mV for devices from set B irradiated to different radiation doses.

B. MOS Capacitors

GaAs MOS capacitors with 4 nm Al_2O_3/8 nm La_2O_3 gate stack are studied to further understand the TID response in Al_2O_3/La_2O_3-gated devices. Well-behaved pre-irradiation C-V curves have been obtained for MOS capacitors at frequencies ranging from 1 kHz to 1 MHz, as shown in Fig. 5. Frequency dispersion of 3% in the accumulation region has been observed over this frequency range. Hill's method [13] has been adopted in order to extract interface-trap density from single *C-V* and *G-V* characteristics at a frequency of 1 MHz. The following equation is used to estimate an initial, as-processed trap density of $\sim 7 \times 10^{11}$ $cm^{-2}eV^{-1}$, which is comparable to that of results in [6].

$$Dit = \frac{(2.Gmax)/(q.A.\omega)}{\left[\left(\frac{Gmax}{\omega.Cox}\right)^2 + \left(1 - \frac{Cm}{Cox}\right)^2\right]}.$$

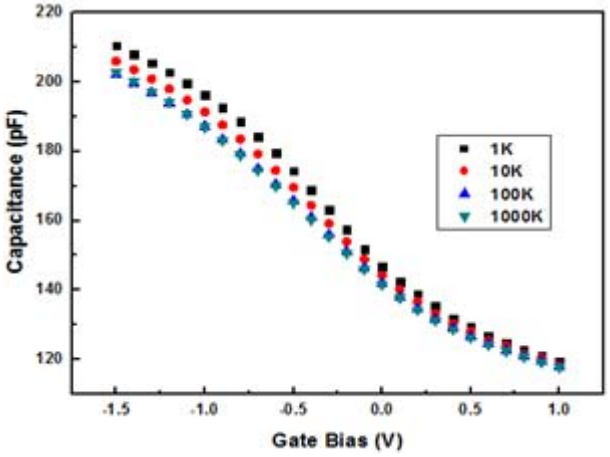

Fig. 5. Multi-frequency *C-V* curves for GaAs MOS capacitors with 4 nm Al2O3/ 8 nm La2O3.

More detailed information on as-processed device characteristics can be found in [6].

Fig. 6(a) shows the C-V characteristics measured at 10 kHz after each increment of x-ray irradiation dose. Fig. 6(b) summarizes ΔV_{fb} at incremental x-ray doses up to 1000 krad(SiO_2). Consistent with the observed values of ΔV_{th} for GaAs MOSFETs having a 4 nm Al_2O_3/4 nm La_2O_3 gate stack (set B), MOS capacitors with 4 nm Al_2O_3/8 nm La_2O_3 gate stacks show positive ΔV_{fb} up to 100 krad(SiO_2), and then shift negatively. Capacitors with thicker epitaxial La_2O_3 layers show larger positive V_{fb} shifts compared to devices with thinner La_2O_3 layers. Moreover, the turn-around dose for ΔV_{fb} is higher for devices with thicker La_2O_3 ($\sim$ 100 krad(SiO_2)) than with thinner La_2O_3 ($\sim$ 10 krad(SiO_2)). The aforementioned observations suggest that radiation induced electron trapping may primarily exist in the crystalline La_2O_3 layer, whereas hole trapping primarily exists in the Al_2O_3 layer. Effects of biased irradiation on Al_2O_3- and HfO_2-based devices were considered in [12] and [14], with qualitatively similar results. We focused on zero bias in this work because the built-in electric field is sufficient to observe radiation-induced charge trapping effects without the complicating effects of charge injection from the substrate during the irradiation. Finally, we note that the above results suggest that electron traps have lower densities but higher capture cross sections than hole traps in these materials.

C. ACGD Measurements

In order to better understand the charge trapping mechanisms in Devices A and B, the AC-G_m dispersion (ACGD) method is employed [9]–[11]. Fig. 7(a) shows the experimental set-up for the ACGD measurement. A lock-in amplifier is used to generate both DC and AC signals having an amplitude of 25 mV. An AC-DC mixer is used to superimpose the AC on top of DC, which is then applied to the device. Current flowing through the channel is passed through a current amplifier, and the output from the amplifier is fed back into the lock-in amplifier. From the first harmonic measurement, the lock-in amplifier can record the variation in drain current due to

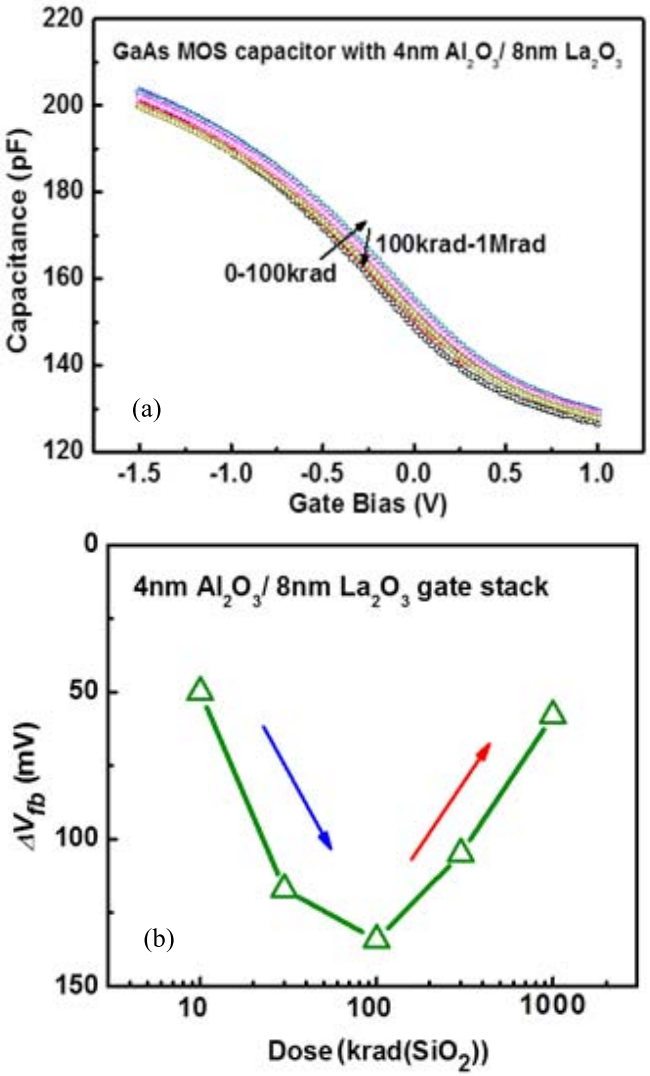

Fig. 6. (a) *C-V* curve (measured at 10 kHz) shifts with increasing radiation dose up to 1000 krad(SiO_2) for GaAs MOS capacitors with 4 nm Al_2O_3/ 8 nm La_2O_3 and (b) initial positive V_{fb} shifts turn negative as the radiation dose increases, indicating two trapping mechanisms, electron and hole trapping.

the application of the AC superimposed DC gate signal. The variation divided by the AC amplitude of the gate voltage gives the AC-G_m. Fig. 7(b) shows the AC-G_m (color) and the DC-G_m (black) characteristics as functions of gate bias for Device A.

Figs. 8(a) and (b) show AC-G_m measurements as functions of frequency at several different applied gate biases for as-processed Devices from groups A and B, respectively. The frequency range for both devices is between 0.5 Hz and 20 kHz.

It has been previously shown that the sign of the slope of the AC-G_m vs frequency curve can provide insight into the charge trapping mechanism in the gate stack [11]. In the AC-G_m dispersion method, the oxide (border) trap [15] density depends on G_m and frequency as $N_{ot} \propto \frac{dG_m}{dln\omega}$. The sign of $\frac{dG_m}{dln\omega}$ indicates the trapping mechanism between channel carriers and border traps, electron trapping or hole trapping. For Device A, only one slope is observed for all gate biases, indicating that there is only one dominant trapping

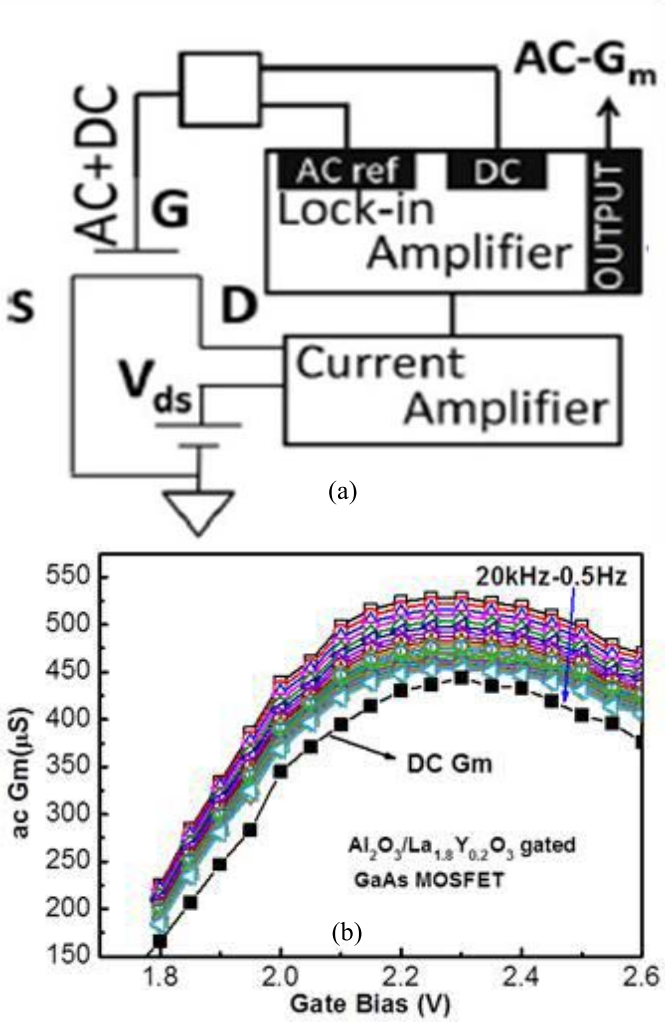

Fig. 7. (a) Schematic diagram of experimental set-up for AC-G_m dispersion measurement; (b) AC-G_m vs gate bias obtained from Device A with $Al_2O_3/La_{1.8}Y_{0.2}O_3$ gate.

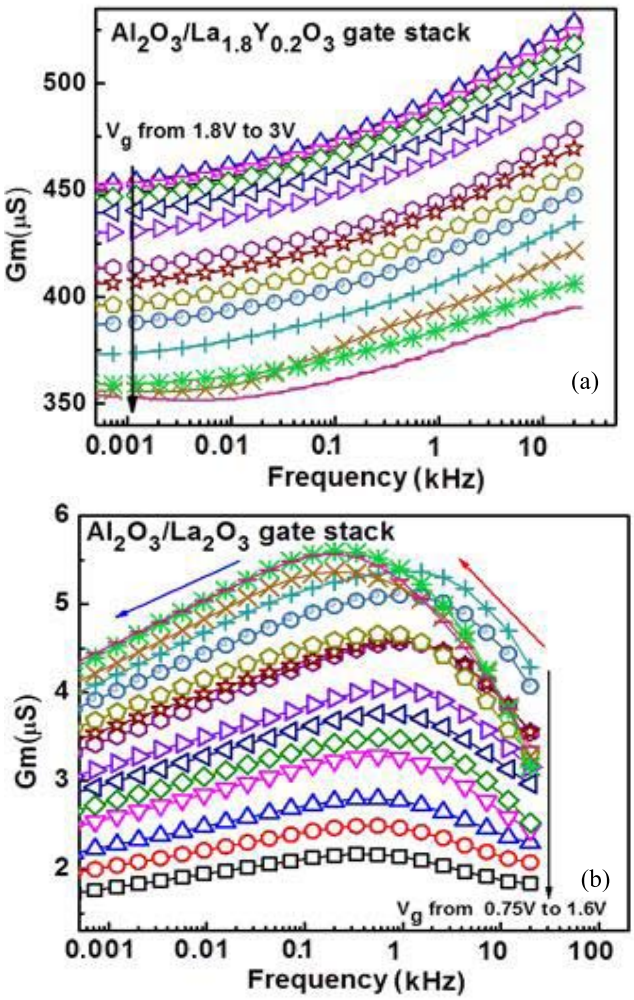

Fig. 8. (a) AC-G_m vs frequency at various gate biases for Device A with gate stack of $Al_2O_3/La_{1.8}Y_{0.2}O_3$, and (b) Al_2O_3/La_2O_3 (Device B), respectively.

mechanism in the $Al_2O_3/La_{1.8}Y_{0.2}O_3$ gate stack. However, for Device B, two opposite slopes are observed: the AC-G_m decreases with increasing frequency at high frequencies (above 1kHz), but increases with increasing frequency at lower frequencies, confirming that both electron and hole trapping are observed in these devices. These observations from AC-G_m data for Devices A and B are in good agreement with the corresponding MOSFET TID responses.

The strong AC-G_m signals and the observed frequency dispersion demonstrates that, for each device, it is likely that holes are exchanged with border traps; for Device B at higher frequencies, the exchange of electrons with fast border traps (or interface traps) also contributes to the measured AC-G_m signal.

Finally, we note that oxygen vacancies can act as trap centers in La_2O_3. Fourfold-coordinated oxygen vacancies with V^{-2}, V^{-1}, V^0, V^{+1}, V^{+2} charge states and sixfold oxygen vacancies with V^0, V^{+1}, V^{+2} charge states have been reported in [16], [17]. Hence, it is quite plausible to observe both radiation-induced hole and electron trapping in La_2O_3-based dielectric layers in MOS devices.

IV. Conclusion

In conclusion, we have observed primarily hole trapping in $La_{1.8}Y_{0.2}O_3$ gated devices, and both electron and hole trapping in the La_2O_3 gated devices. The thinner dielectric layers and compensating electron trapping in the La_2O_3-based devices lead to superior radiation resistance compared to the $La_{1.8}Y_{0.2}O_3$ gated devices. MOS capacitors show similar responses, although the dose for which the hole trapping becomes dominant is higher than has been found in MOSFETs. This is due to the use of thicker La_2O_3 layers in capacitor structures. *AC-G_m* measurements are consistent with the results of the *I-V* and *C-V* measurements. With future technology development, it should be expected that the radiation-induced voltage shifts in these dielectric layers should decrease with decreasing dielectric layer thickness. These results are useful to the further development of GaAs MOSFET technology, and show that devices are becoming more promising for potential future, radiation-tolerant technology.

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