Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods

Junkang Li, Yiming Qu, Mengwei Si, Xiao Lyu, and Peide D. Ye*
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA. Email: *yep@purdue.edu

Abstract

In this work, we report on the multi-probe characterization of interfacial charges at the ferroelectric/dielectric (FE/DE) interface in response to both large-signal measurement associated with polarization switching and small-signal measurement without polarization switching. Charge densities at the FE/DE interface are extracted from temperature dependent C-V, P-V, conductance methods. It is found that the charge injection and accumulation at the FE/DE interface play a key role in the operation of FE/DE stack. These enormous trapped charges of 10^{13}-10^{14}/cm^2 at the FE/DE interface are supplied from the leakage current through the ultrathin DE layer. The proposed multi-probe measurement techniques provide a comprehensive understanding of FE/DE stack. The demonstrated leakage-assist polarization switching provides the new insights on the understanding of negative - capacitance (NC) effect and ferroelectric device performance.

Introduction

Ferroelectric-gated field-effect transistor (FET) is widely studied as its application on non-volatile memory as ferroelectric FET (Fe-FET) and low power CMOS logic as negative capacitance FET (NC-FET) [1-4]. FE/DE stack is commonly applied in both Fe-FET and NC-FET. It is known that the FE/DE stack is fundamentally different from a FE capacitor and a DE capacitor in series due to the FE/DE interfacial coupling effect and charge accumulation at the FE/DE interface [5-13]. However, the physical mechanism of this coupling effect, especially the charge behaviors and interface trap properties, is still unclear.

In this work, interfacial charges in the FE/DE stack are characterized quantitatively. P-V and C-V techniques are firstly applied in the FE/DE stack to obtain the charge density during dynamic polarization switching. Furthermore, the conductance (G-V) method, which is widely used for the study of MOS interface [14], is for the first time formulated to measure the density of FE/DE interface traps. FE/DE interfacial charges considering both with and without polarization switching are clarified for FE devices towards logic and memory applications.

Device Fabrication

$Hf_{0.5}Zr_{0.5}O_2$ (HZO) is chosen as the FE layer and Al_2O_3 is chosen as the DE layer to study the FE/DE interface properties. TiN, HZO and Al_2O_3 were deposited by atomic layer deposition (ALD). TiN was deposited at 250 °C, using TDMAT and NH_3 as the Ti and N precursors. A 10 nm HZO (Hf:Zr=1:1) film was deposited at 200 °C, using TDMAHf, TDMAZr, and H_2O as the Hf, Zr, and O precursors. The stacked Al_2O_3 layer with four different thicknesses (1, 2, 3, 5 nm) was deposited at 200 °C, using TMA and H_2O as Al and O precursors. Another TiN was deposited on the top of HZO/Al_2O_3 stack. Finally, the samples were annealed at 500 °C in a N_2 ambient for 1 min by rapid thermal annealing. Fig. 1 shows the P-V properties of HZO/Al_2O_3 capacitors with different Al_2O_3 thicknesses. The significant decrease of remnant polarization (P_r) in P-V hysteresis loops is observed with thicker DE layer, which is consistent with previously reported leakage-assist-switching mechanism [11]. Figs. 2(a) and 2(b) show phase-voltage and amplitude-voltage hysteresis loops by piezoresponse force microscopy (PFM) measurement, which further confirm the ferroelectricity of HZO.

Results and Discussion

Figs. 3(a) and (b) show the temperature dependence of P-V properties for the 10 nm HZO/3 nm Al_2O_3 capacitor at high and low temperatures. Fig. 4 summaries the P_r values at different temperatures. It is found that P_r is smaller at lower temperatures because of the reduction of leakage current and less charges provided for polarization switching. It indicates that this leakage-assist charge injection is a thermionic process instead of direct tunneling. To clarify this phenomenon, C-V measurements were performed at the 10 nm HZO/3 nm Al_2O_3 capacitor with the frequencies ranging from 1 kHz up to 6 MHz (Fig. 5). Charge injection behaviors are confirmed by large frequency dispersion. Capacitance of a 20 nm Al_2O_3 capacitor was also measured as the control sample at different frequencies to exclude the influence of parasitic effect in the devices or the measurement setup (Fig. 6). Moreover, the C-V properties at low temperatures (Fig. 7) and at different frequencies (Fig. 8) were also measured. The smaller capacitance and larger frequency dispersion at lower temperatures further manifests the charge injection at the FE/DE interface.

To evaluate the density of injected charges, a simple approach with a combination of P-V and C-V measurements is proposed. As schematically shown in Fig. 9, the total polarization charge density (N_{tot}) is provided by P-V loops, and the charge density on the electrodes ($N_{electrode}$) is obtained by C-V curves. Then, injected charge density at the FE/DE interface (N_{in}) can be calculated by subtracting $N_{electrode}$ from N_{tot}. Fig. 10 exhibits surprisingly large N_{in} of ~10^{14} cm^{-2} for the 10 nm HZO/3 nm Al_2O_3 capacitor during dynamic polarization switching, which indicates that these injected charges are dominant for the polarization switching, similar to the phenomenon reported in the FE/DE stack [11] and also the Fe-FET [13]. It unveils that FE/DE interface is *not* fully investigated and understood. This *new* interface could play an important role in the device operations of Fe-FETs and NC-FETs.

In addition, G-V method is also for the first time applied in the metal/FE/DE/metal structure. As a small-signal measurement (30 mV), it is to characterize the interface traps at a steady polarization state. Fig. 11(a) shows the modified circuit model for this G-V method, which consists of the DE capacitance, C_{DE}, the FE capacitance, C_{FE}, the interface trap capacitance, C_{it}, and the loss of charge capture-emission by interface traps, R_{it}. Fig. 11(b) gives the mathematical expression of admittance for this circuit model, where the conductance, G_p, and capacitance, C_p, can be directly measured by LCR meter. It is found that, C_p is large at low frequency due to the immediate response of interface traps to the ac voltage, while C_p decreases at high frequency since the trap responses lag behind. This trend is consistent with the result observed in Fig. 6, suggesting the validation of the proposed model. By using this method, the G_p/ω-frequency relationships are characterized for the HZO/Al_2O_3 capacitors with different Al_2O_3 thicknesses (Fig. 12). It is observed that the G_p/ω peak value decreases and the peak frequency value increases with increasing the Al_2O_3 thickness (Figs. 13 and 14). Fig. 15(a) shows the density of interface traps (D_{it}) ~ 10^{13}/cm^{2}eV obtained from G_p/ω peaks experimentally. Note that this is the interface trap responses to the small-signal measurement. It is fundamentally different from the charge density induced by ferroelectric polarization switching. Fig. 15(b) shows the extracted frequencies at G_p/ω peak by the proposed model, with a time constant (τ_{it}) of ~1.6 μs. The result agrees well with the measured data (Fig. 14), indicating the validity of conductance method applied in the FE/DE structure to characterize the FE/DE interface properties.

Conclusion

The multi-probe C-V, P-V and G-V methods are applied to characterize the interfacial charge response at the FE/DE interface. The interfacial charge density is at ~10^{14}/cm^2 during dynamic polarization switching and D_{it} ~10^{13}/cm^{2}eV by small-signal response at a steady polarization state. The FE/DE interface is of importance to understand NC-FETs and Fe-FETs operations. The work is supported by SRC/DARPA JUMP ASCENT Center.

References: [1] J. Muller et al., *Appl. Phys. Lett.*, **99**, 112901, 2011. [2] K. Ni *et al.*, *IEEE TED*, **65**, 2461, 2018. [3] S. Salahuddin *et al.*, *Nano Lett.*, **8**, 405, 2008. [4] W. Chung *et al.*, *IEDM*, 365, 2017. [5] Y. J. Kim *et al.*, *J. Appl. Phys.*, **118**, 224105, 2015. [6] A. Khan *et al.*, *IEEE TED*, **63**, 4416, 2016. [7] F. C. Sun *et al.*, *J. Mater. Sci.*, **51**, 499−505, 2016. [8] Y. J. Kim *et al.*, *Nano Lett.*, **16**, 4375, 2016. [9] M. Hoffmann *et al.*, *IEDM*, 727, 2018. [10] M. A. Alam *et al.*, *Appl. Phys. Lett.*, **114**, 090401, 2019. [11] M. Si *et al.*, *ACS Appl. Elec. Mat.*, **1**, 745, 2019. [12] K. D. Kim *et al.*, *Adv. Funct. Mater.*, **29**, 1808228, 2019. [13] K. Toprasertpong *et al*, *IEDM*, 570, 2019. [14] E. H. Nicollian *et al.*, *Bell Syst. Tech. J.*, 1055, 1967.

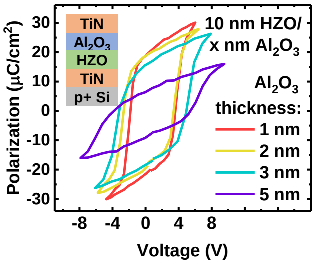


Fig. 1. P-V hysteresis loops of HZO/Al_2O_3 capacitors with different Al_2O_3 thicknesses. Thicker Al_2O_3 can prevent FE switch in FE/DE stack.

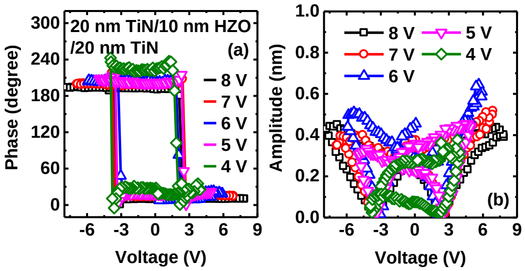


Fig. 2. (a) Phase-voltage and (b) amplitude-voltage hysteresis loops by PFM measurement at different voltage ranges, showing clear ferroelectricity of HZO.

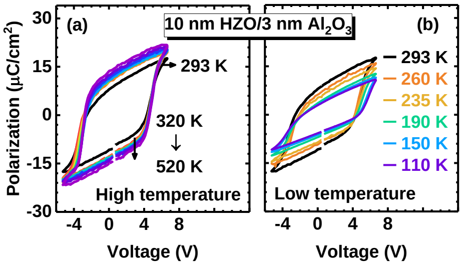


Fig. 3. P-V hysteresis loops for the 10 nm HZO/3 nm capacitor (a) at high temperatures above 293 K and (b) at low temperatures below 293 K.

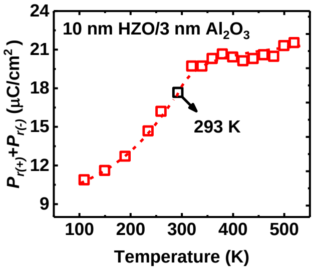


Fig. 4. Temperature dependence of P_r for a 10 nm HZO/3 nm Al_2O_3 capacitor.

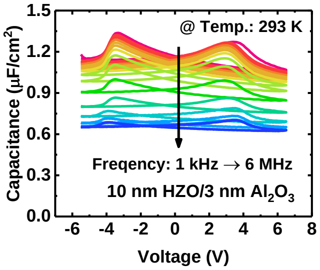


Fig. 5. C-V characteristics of the 10 nm HZO/3 nm capacitor measured from 1 kHz to 1MHz.

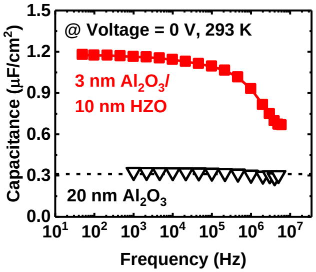


Fig. 6. Frequency dependence of capacitance at $V = 0$ V for the 10 nm HZO/3 nm Al_2O_3 and 20 nm Al_2O_3 capacitor.

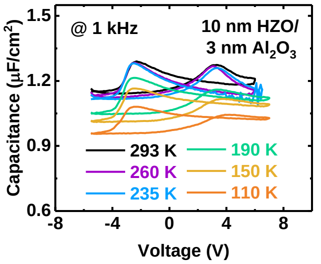


Fig. 7. C-V characteristics of the 10 nm HZO/3 nm Al_2O_3 capacitor measured at the frequency of 1 kHz measured from 110 to 293 K.

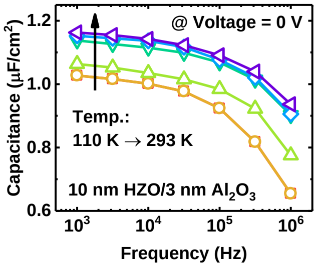


Fig. 8. Frequency dependence of capacitance at $V = 0$ V for the 10 nm HZO/3 nm Al_2O_3 capacitor measured from 110 to 293 K.

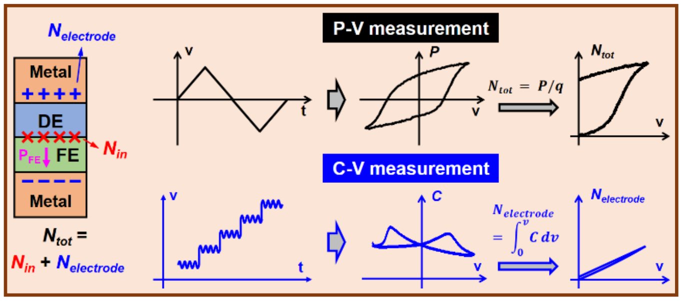


Fig. 9. Illustration of the characterization method to extract the injected charges at the FE/DE interface by C-V and P-V measurements.

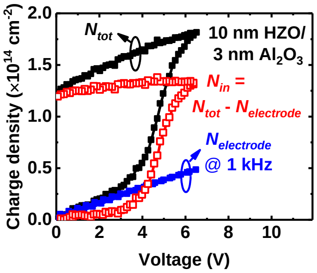
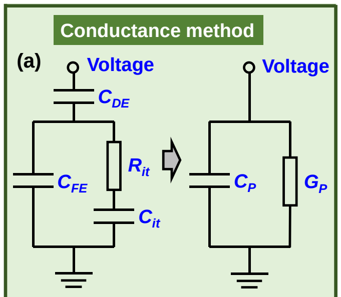


Fig. 10. Measured N_{tot}, $N_{electrode}$ and calculated N_{in} for the 10 nm HZO/3 nm Al_2O_3 capacitor.



$$Y_{it} = G_p + j\omega C_p \qquad \text{(b)}$$

$$\frac{G_p}{\omega} = \frac{(\omega\tau_{it})C_{DE}^2C_{it}}{(\omega\tau_{it})^2(C_{FE}+C_{DE})^2 + C_A^2}$$

$$\left.\frac{G_p}{\omega}\right|_{peak} = \frac{C_{DE}^2}{2(C_{FE}+C_{DE})C_A}C_{it};\ \omega_{peak} = \frac{C_{FE}+C_{DE}+C_{it}}{(C_{FE}+C_{DE})\tau_{it}}$$

$$C_p = \frac{C_AC_{FE}[C_{DE}+C_{it}] + (\omega\tau_{it})^2C_{FE}C_{DE}(C_{FE}+C_{DE})}{(\omega\tau_{it})^2(C_{FE}+C_{DE})^2 + C_A^2}$$

$$C_p = \frac{C_{DE}(C_{FE}+C_{it})}{C_{FE}+C_{DE}+C_{it}}(\omega \to 0);\ C_p = \frac{C_{FE}C_{DE}}{(C_{FE}+C_{DE})}(\omega \to \infty)$$

$$\text{Here,}\ \ C_A = C_{FE}+C_{DE}+C_{it},\ \ C_{it} = qD_{it}$$

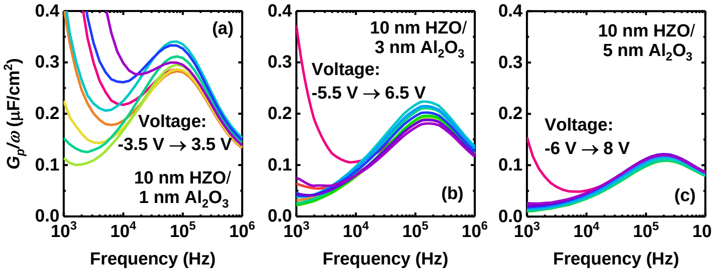


Fig. 12. Experimental results of the G_p/ω-frequency curves at different voltages for the HZO/Al_2O_3 capacitors with Al_2O_3 thickness of 1 nm (a), 3 nm (b), 5 nm (c). Clear G_p/ω peak can be observed for all the capacitors.

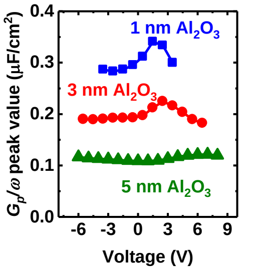


Fig. 13. Summarized G_p/ω peak for the HZO/Al_2O_3 capacitors with 1, 3, 5 nm Al_2O_3.

Fig. 11. (a) Modified circuit model for the conductance method applied in the FE/DE stack to extract the FE/DE interface trap; (b) mathematical expression of the admittance for this model.

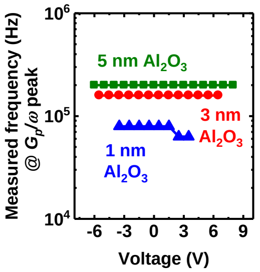


Fig. 14. Summarized peak frequency values for the HZO/Al_2O_3 capacitors with 1, 3, 5 nm Al_2O_3.

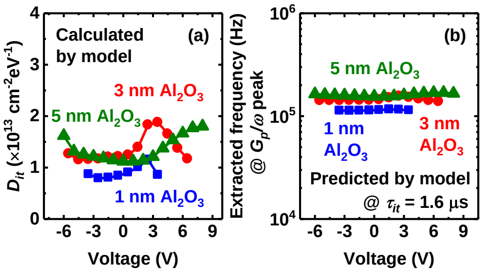


Fig. 15. (a) Calculated D_{it} of the HZO/Al_2O_3 capacitors with different Al_2O_3 thicknesses; (b) peak frequency values predicted by the model when τ_{it} is around 1.6 μs.