First Direct Experimental Studies of $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Polarization Switching Down to 100-picosecond in Sub-60mV/dec Germanium Ferroelectric Nanowire FETs

Wonil Chung[1], Mengwei Si[1], Pragya R. Shrestha[2,3], Jason P. Campbell[3], Kin P. Cheung[3] and Peide D. Ye[1]*
[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA
[2]Theiss Research, La Jolla, CA 92037, USA
[3]National Institute of Standards and Technology, Gaithersburg, MD 20899, USA
*Email: yep@purdue.edu

ABSTRACT

In this work, ultrafast pulses with pulse widths ranging from 100 ps to seconds were applied on the gate of Ge ferroelectric (FE) nanowire (NW) pFETs with FE $Hf_{0.5}Zr_{0.5}O_2$ (HZO) gate dielectric exhibiting steep subthreshold slope (SS) below 60 mV/dec bi-directionally. With applied gate bias pulses (V_G = -1 to -10 V), high-mobility Ge drain current was monitored as a test vehicle to capture the polarization switching of HZO. It was found that HZO could switch its polarization directly by a single pulse with the minimum pulse width of 3.6 ns. The polarization switching triggered by pulse train with pulse width as short as 100 ps was demonstrated for the first time.

INTRODUCTION

To further reduce device's SS for lower power operation, negative capacitance FETs (NC-FETs) and use of ferroelectric oxide have been recently studied intensively [1]–[4]. Embedded FE oxides such as HZO within the gate stack of a conventional structure has proven to be successful in SS reduction below the 60 mV/dec limit on various channel materials [5]–[10]. HZO specifically has been reported to be reliable in terms of its switching and polarization capability [8], [11]–[15]. The time response of ferroelectric polarization switching is crucial to evaluate the working speed of HZO based ferroelectric FETs (Fe-FETs) and NC-FETs. However, time response properties of the HZO in FE-FETs were rarely studied. Specifically, at ultrafast sub-10ns regime (towards GHz working frequency), time response of HZO has not been extensively studied yet. In this work, we report the *direct experimental observation* of HZO polarization switching under deep sub-10ns and extend the study using pulse train with 100 ps pulses.

EXPERIMENT

Process flow for the fabrication of Ge FE NW FET with FE HZO gate stack was elaborated in our previous report [6] except the NW release step after fin formation. GeOI wafer was implanted by BF_2^+ ions. Dimensions of fins were controlled by SF_6-based dry etching. HF solution was used to release the Ge NWs from SiO_2. 1 nm Al_2O_3 was deposited by atomic layer deposition (ALD), followed by post-oxidation (O_2, 500 °C) to form ultrathin GeO_x. Subsequent HZO (10 nm) and Al_2O_3 (1 nm) were deposited by ALD and post deposition annealed at 500 °C. Source and Drain areas were etched and deposited with Ni for optimum contacts. 3D structure and SEM images of the final devices are shown in Fig. 1 and 2 respectively.

RESULTS AND DISCUSSION

Firstly, the HZO film was analyzed with XRD as shown in Fig. 3 revealing its non-centrosymmetric, orthorhombic crystal structure which causes the FE property [10]. Ferro-electricity of HZO can be further confirmed with P-V measurement (Fig. 4) showing a clear ferroelectric loop [5]–[7].

Fig. 5 is a typical I_D-V_G curve of the fabricated Ge FE NW pFET. Steep sub-60mV/dec SS for five orders of I_D changes are observed bi-directionally. Fig. 6 (a) and (b) show I_D-V_D curves swept in forward and reverse direction, respectively. Negative differential resistance (NDR) is observed owing to negative drain-induced-barrier-lowering (DIBL) [5]. Fig 7 (a) and (b) depict the instrument set-up for generation and measurement of ultrafast pulses with logarithmically increasing widths from 100 ps to few seconds. Agilent 81110 Pulse Generator (PG) was used with current amplifier and a Lecroy oscilloscope (Fig. 7 (a)) for pulse width > 3.6 ns. For picosecond pulses, as shown in Fig. 7 (b), AVTECH PG was used triggered by the Agilent 81110 PG with a period of 2 µs. Lecroy oscilloscope operating at 80 GS/s sampling rate was used to monitor the sub-ns pulse precisely. V_G and V_D applied to the gate are shown in Fig. 8 (a) and (b). To switch the polarization to off-state, as shown in Fig. 8 (a), initialization pulse V_G = 5 V was applied (>100 ms). Different V_G levels (-1 ~ -10V) were pulsed to the gate with various pulse widths and change in I_D was monitored precisely with oscilloscope in real time through a current amplifier. V_G and V_D were 0 V and -50 mV respectively during the measurements carried out between two adjacent V_G pulses to minimize the effect on the polarization. For lower V_G range (-1 ~ -4 V), Keysight B1530A Waveform Generator/Fast Measurement Unit (WGFMU) was used and the measurement time was fixed at 100 µs. Fig. 9 shows that it takes much shorter time to switch the polarization when the V_G pulse approaches -4 V. As pulse width was decreased to sub-µs regime, transient current fluctuation was observed when the polarization switching occurred as seen in Fig. 10 (a) and (b). Therefore, the current was read after stabilization to ensure it was the current caused by changed polarization state only. At higher V_G (-5 ~ -10 V), sub-10ns switching was also observed directly by experiment and it switched fastest at V_G = - 10 V (Fig. 11). Off-state current was plotted at t = 1 ns to show clear I_D transition from off to on-state. The fastest switching by a single pulse observed in our Ge FeFETs with 10 nm HZO was 3.6 ns (Fig. 12). Considering the RC delay present in the measurement set-up and the large probing pads, the intrinsic time response of polarization is expected to be faster than 3.6 ns. To further investigate the effect of sub-ns pulses, Fig. 7 (b) set-up was configured and 100 ps pulses with period of 2 µs (Fig. 13 (a), V_G = -6 V) were generated in the form of pulse train (duty cycle = 0.005 %). Although a single 100 ps pulse (Fig. 14) did not trigger noticeable polarization switching, as the pulses accumulated, polarization switching could be detected (Fig. 15). Further studies on the effect of duty cycle with picosecond pulse widths could be valuable for deeper understanding of dynamics of polarization switching in HZO devices for various applications including FeRAM.

CONCLUSION

High mobility Ge FE NW pFETs were applied as test vehicles for the first time to study the time response of FE HZO gate stack down to 100 ps. It was found that a single deep sub-10ns pulse or even a pulse train with 100 ps pulses were enough to initiate polarization switching in HZO. This work opens the route to studying the dynamics of FE HZO through direct experiments down to 100 ps and even beyond. The work is supported by SRC and Lam Research. U.S. Government is not endorsing any of the equipment mentioned in the paper.

References: [1] S. Salahuddin et.al., *Nano Lett.,* 2008. [2] Z. Krivokapic et.al., *IEDM*, 2017. [3] H. Ota et. al., *IEDM*, 2016. [4] P. Sharma et.al., *VLSI*, 2017. [5] M. Si et. al., *Nat. Nanotechnol.*, vol. 13, p. 24–28, 2018. [6] W. Chung et. al., *IEDM*, 2017. [7] M. Si et. al., *IEDM*, 2017. [8] M. H. Lee et. al., *IEDM*, 2016. [9] C.-J. Su et. al., *VLSI*, 2017. [10] J. Muller et. al., *Nano Lett.*, 2012. [11] K.-Y. Chen et. al., *VLSI*, 2017. [12] H. J. Kim et. al., *Nanoscale*, vol. 8, p. 1383, 2016. [13] J. Muller et. al., *EDL*, vol. 33, no. 2, p. 185-187, 2012. [14] Y. Chiu et. al., *IRPS*, 2015. [15] S. Oh et. al., *EDL*, vol. 38, no. 6, p. 732-735, 2017.

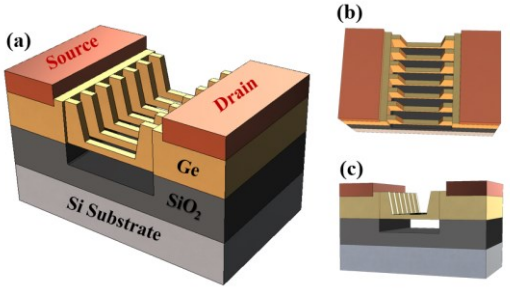

Fig. 1. 3D structure of a Ge NW FET viewed from **(a)** top-right, **(b)** top and **(c)** front. Under the nanowires, SiO_2 was etched and kept hollow.

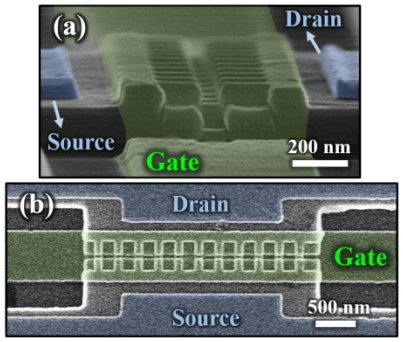

Fig. 2. SEM images of fabricated device viewed from **(a)** side and **(b)** top. 11 parallel NWs make one device.

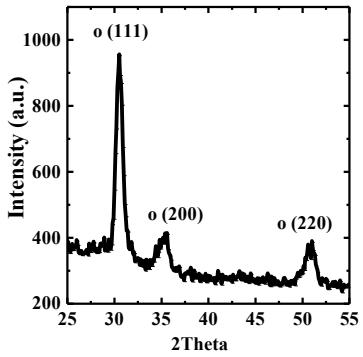

Fig. 3. XRD peaks of the $Hf_{0.5}Zr_{0.5}O_2$ film used in the device exhibits orthorhombic structure.

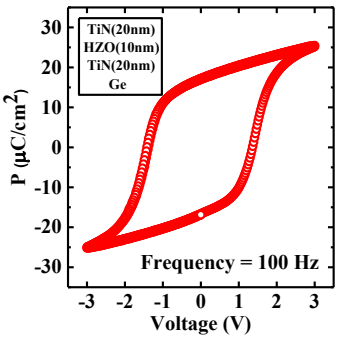

Fig. 4. Polarization-Voltage (P-V) graph of 10 nm HZO film measured at frequency of 100 Hz.

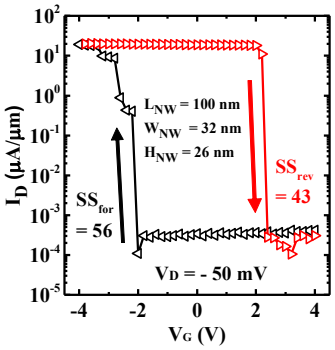

Fig. 5. I_D-V_G exhibits bi-directional SS < 60 mV/dec for 4~5 orders of I_D changes.

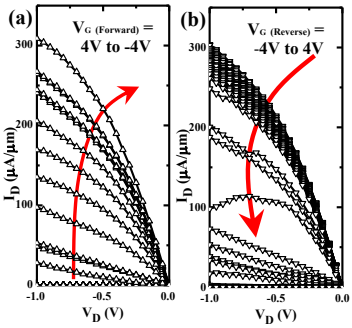

Fig. 6. I_D-V_G of **(a)** forward and **(b)** reverse sweeps. Negative Differential Resistance (NDR) can be observed in reverse sweep direction.

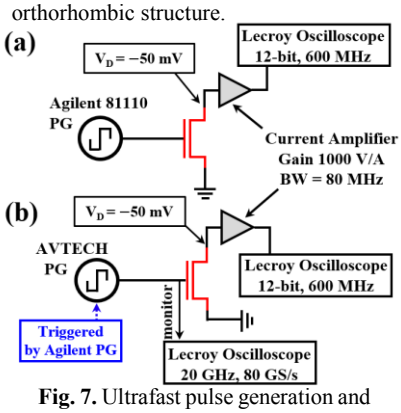

Fig. 7. Ultrafast pulse generation and measurement set-up for **(a)** pulse widths > 3.6 ns and **(b)** picosecond pulses.

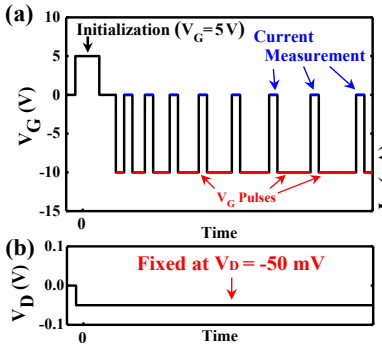

Fig. 8. Pulse time line of **(a)** V_G and **(b)** V_D. Currents were measured in between pulses with V_G = 0 V.

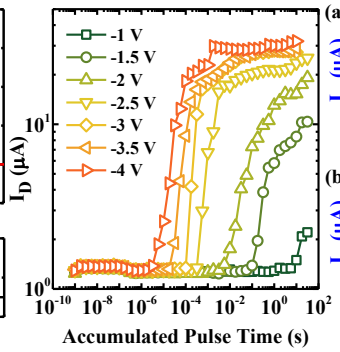

Fig. 9. Polarization current (I_D) over accumulated pulse time with different V_G pulses. Keysight B1530A was used for these pulses.

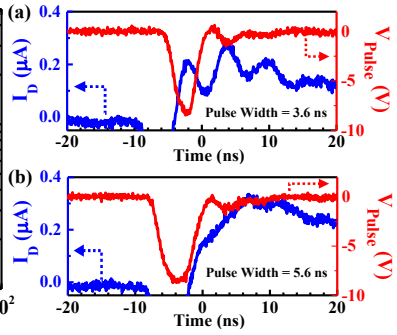

Fig. 10. Polarization switching can be monitored by I_D. Time responses with pulse widths of **(a)** 3.6 ns and **(b)** 5.6 ns are shown. I_D was taken after the fluctuation was stabilized.

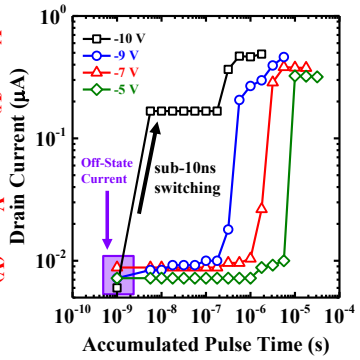

Fig. 11. V_G was pushed down to -10 V to probe the polarization switching limit which showed minimized time under 10 ns. Off-state current was plotted at 1 ns for reference.

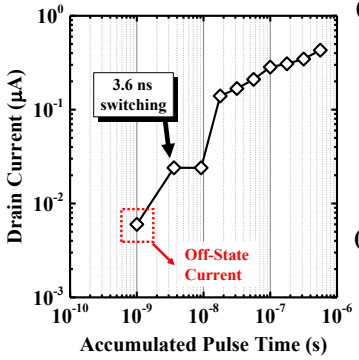

Fig. 12. The fastest switching was observed at accumulated V_G pulse time of 3.6 ns. Off-State current was plotted at 1 ns for reference.

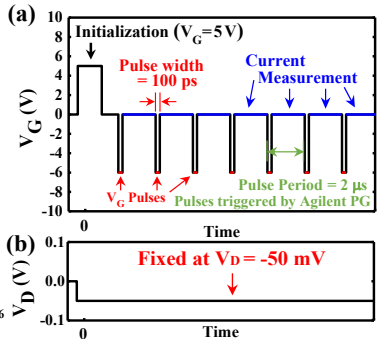

Fig. 13. (a) V_G and **(b)** V_D settings for sub-ns pulse measurements with Fig. 7 (b) configuration. I_D was kept constant at -50 mV and 100 ps pulses were triggered every 2 μs (duty cycle = 0.005 %).

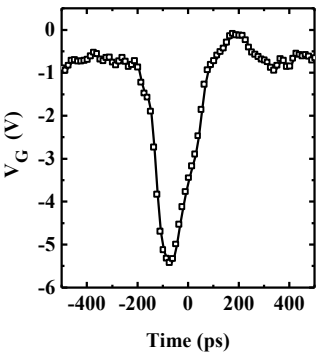

Fig. 14. 100 ps pulse generated with rise time of 60 ps was measured at the rate of 80 GS/s. Maximum voltage was -6 V. To avoid loss of voltage due to cables, the PG was placed very close to the device.

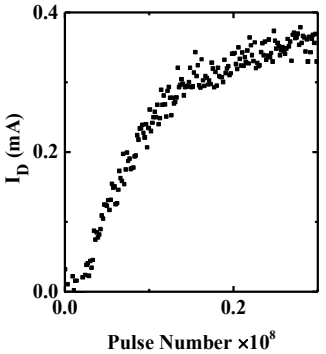

Fig. 15. Polarization switching was monitored by applying the 100 ps pulse shown in Fig. 14 in the form of a continuous pulse train.