First Experimental Demonstration of Ge 3D FinFET CMOS Circuits

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I. Abstract
We report the first experimental demonstration of Ge 3D CMOS circuits, based on the recessed fin structure. Both n-FinFETs and p-FinFETs with channel length (Lch) from 200 to 20 nm and fin width (WFin) from 60 to 10 nm are realized on a Ge-on-insulator (GeOI) substrate. The Ge FinFETs show superior gate electrostatic control over planar counterparts and sub-threshold swing (SS) as low as 93 and 73 mV/dec are obtained on n- and p-FETs, respectively. Combining the n- and p-type 3D devices together, the FinFET CMOS inverters have high voltage gain up to 34 V/V at Vds of 1 V, demonstrating more than 200% improvement over the planar ones at the same Lch of 200 nm. Scalability studies are also carried out for both types of FinFETs in terms of Lch and WFin.

II. Introduction
Recently, Ge CMOS circuits have been experimentally demonstrated on GeOI [1] or poly-Ge substrate [2], showing the promise of Ge CMOS beyond CMOS-Si technology node. However, the device characteristics such as SS, DIBL and Lch scaling metrics of the planar Ge recessed channel MOSFETs [3] are still greatly limited by the planar structure, suffering from relatively severe short channel effects (SCEs). Various 3D structures such as: tri-gate fin [4-5], omega-gate [6] and gate all around (GAA) nanowire [7] have been widely applied to Ge [8-14] or III-V compounds [15] to enhance the gate electrostatics, demonstrating the scaling of device down to sub-20 nm. However, to our best knowledge, there’s no CMOS circuit level work reported on Ge 3D transistors [13-17]. In this paper, we successfully integrate the 3D fin structure into the recessed channel, building up the first Ge 3D FinFET CMOS circuits. The introduction of 3D structure has allowed the demonstration of decent SSs of 93 and 73 mV/dec on 200 nm Lch for n- and p-type devices and high voltage gains up to 34 V/V for CMOS inverters, providing more than 200% improvement over the planar ones. Lch and WFin and doping concentration dependence of device characteristics are also studied in great details.

III. Experiment
Fig. 1(a) summarizes the fabrication processes of the Ge recessed FinFET CMOS and Fig. 1(b) gives the CMOS inverter schematic, with the recessed fin highlighted, which is further enlarged in Fig. 1(c) for a better illustration with the doping density plotted as the color map. For balanced device performance, 4 recessed fins are employed for nFETs and 5 for pFETs. The experiment started with the GeOI wafer grown by the SmartcutTM technology from SoitecTM. After a standard cleaning, the device isolation was carried out by dry etching. Next, the samples were selectively P and BF2 implanted consequently, which were activated by rapid thermal annealing (RTA), respectively. Note that a split anneal condition with low and shallow doping was used in the P implantation to study the doping density dependence. Then, an optimized common SF6 dry etching was used to form the recessed channel, followed by another common dry etching process to define the fins in the channel. The fin dry etching is carefully calibrated to get a near vertical side wall surface with high aspect ratio. After a surface wet clean, 1 nm Al2O3 capping layer was first deposited and then the post-oxidation was performed as the interface passivation, continued by a common 80 nm ALD Al2O3 gate dielectric deposition. After a post deposition annealing (PDA) in forming gas ambient, common recessed S/D etching was conducted, with Ni deposited as the common metal contact, followed by an ohmic annealing. Finally, the common gate metal was formed by Ni/Au for both nFETs and pFETs and devices were connected for the logic gates.

IV. Results and Discussion
The fabricated devices have Lch from 200 to 20 nm, WFin from 60 to 10 nm fin height (Hfin) from 30 nm and EOT of around 4.5 nm, considering both AlOx and GeOx. Fig. 2(a) shows a FinFET CMOS inverter under SEM, with n- and p-Fins etched after the fabrication process. Thanks to the better gate electrostatic from the 3D fin structure, both SS and DIBL are improved significantly and SS as low as 93 and 73 mV/dec are obtained for n-FinFETs and p-FinFETs, respectively. Ge CMOS inverters with high voltage gain up to 34 V/V also demonstrated.

VI. Reference
Fig. 1 (a) Key processes in the fabrication of the Ge FinFET CMOS. (b) Device schematic of a Ge FinFET CMOS inverter. Note that 4 recessed fins were employed in the n-FinFETs and 5 fins for the p-FinFETs for balanced performance. (c) Illustration of the recessed fin structure.

Fig. 2 (a) Top down SEM image of a fabricated Ge FinFET CMOS inverter. The fin structure in the channel could be clearly observed. (b) The channel area of a fabricated p-FinFET with 5 conducting fins. (c) Zoom-in view of the fin area in (b) with the gate metal removed. The recessed fin region is highlighted.

Fig. 3 One of the narrowest fin structures with \( W_{\text{Fin}} = 10 \) nm and aspect ratio of 18.

Fig. 4 (a) Transfer curves of a 200 nm \( L_{\text{ch}} \) Ge p-FinFET with \( V_{\text{gs}} \) from -0.6 to -2 V at various \( V_{\text{ds}} \) bias. (b) The \( g_m \) versus \( V_{\text{gs}} \) of the same device in (a). A decent \( g_{\text{max}} \) of 555 mS/mm is obtained.

Fig. 5 (a) Transfer curves of a 200 nm \( L_{\text{ch}} \) Ge n-FinFET with \( V_{\text{gs}} \) from -0.6 to 0.5 V at various \( V_{\text{ds}} \) bias. Low SS of 93 mV/dec is obtained. (b) The \( g_m \) versus \( V_{\text{gs}} \) of the same device in (a).

Fig. 6 Transfer curves of a Ge p-FinFET with the lowest SS of 73 mV/dec.

Fig. 7 Scaling metrics of Ge p-FinFETs with \( W_{\text{Fin}} \) of 10, 20, 30 and 40 nm. Scale bars give the standard deviations of data points of more than 5 devices measured. (a) \( L_{\text{ch}} \) dependence of the \( V_{\text{TH}} \). (b) DIBL versus \( L_{\text{ch}} \). Planar pFETs with \( T_{\text{ch}} \) of 25 nm are benchmarked. (c) \( L_{\text{ch}} \) dependence of SS at low \( V_{\text{ds}} \) of -0.05 V. SSs of the same set of planar pFETs in (b) are also compared. (d) \( L_{\text{ch}} \) dependence of \( g_{\text{max}} \) at \( V_{\text{ds}} \) of 1 V.

Fig. 8 \( L_{\text{ch}} \) dependence of 60 nm \( W_{\text{Fin}} \) Ge n-FinFETs with low and high doping. (a) \( V_{\text{IH}} \) metrics. (b) DIBL metrics, benchmarked with planar nFETs of 25 nm \( T_{\text{ch}} \).

Fig. 9 (a) SS scaling metrics of 60 and 20 nm \( W_{\text{Fin}} \) Ge nFinFETs with low and high doping. Planar nFETs are also compared. (b) Dependence of SS on \( W_{\text{Fin}} \).

Fig. 10 \( V_{\text{OUT}} \) versus \( V_{\text{IN}} \) of a 200 nm \( L_{\text{ch}} \) and 10 nm \( W_{\text{Fin}} \) FinFET CMOS inverter at various \( V_{\text{DD}} \).

Fig. 11 Voltage gain versus \( V_{\text{DD}} \) of the same FinFET CMOS inverter in Fig. 10.

Fig. 12 Benchmark of voltage gain of 3D and planar CMOS inverter with \( L_{\text{ch}} \) of 200 nm.