Ge CMOS: Breakthroughs of nFETs (I_{max}=714 mA/mm, g_{max}=590 mS/mm) by recessed channel and S/D

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I. Abstract

We report a new approach to realize the Ge CMOS technology based on the recessed channel and source/drain (S/D). Both junctionless (JL) nFETs and pFETs are integrated on a common GeOI substrate. The recessed S/D process greatly improves the Ge n-contacts. A record high maximum drain current (I_{max}) of 714 mA/mm and trans-conductance (g_{max}) of 590 mS/mm, high I_{on}/I_{off} ratio of 1×10^5 are archived at channel length (L_{ch}) of 60 nm on the nFETs. Scalability studies on Ge nFETs are conducted in sub-100 nm region down to 25 nm for the first time. Considering the Fermi level (E_F) pining near the valence band edge (E_V) of Ge, a novel hybrid CMOS structure with the inversion-mode (IM) Ge pFET and the JL accumulation-mode (JAM) Ge nFET is proposed.

II. Introduction

Ge is considered as a very promising channel material to replace Si, due to its high and balanced carrier mobilities. Benefiting from the E_F pining of Ge near the E_V, recently, high performance Ge pFETs have been demonstrated [1-3]. However, to realize well-behaved Ge nFETs faces more challenges [3-5]. High Schottky barrier in the n-Ge metal-semiconductor (MS) contact leads to large contact resistance. Large inversion electron density requires low D_{it} interface. Strong electron inversion is hard to realize at a non-ideal interface since the trap neutrality level (TNL) tends to align near the E_V of Ge.

In this abstract, a new approach to realize Ge CMOS is demonstrated. Both sub-100 nm L_{ch} nFETs and pFETs are integrated on a common GeOI substrate. Thanks to the low contact resistance on n-Ge enabled by the recessed S/D and the excellent gate control realized by the ultra-thin recessed channel, record high performance Ge nFETs are archived. With a well-engineered gate stack, enhancement-mode (E-mode) devices are obtained for both nFETs and pFETs.

III. Experiment

Fig. 1(a) summarizes the fabrication processes of the Ge recessed channel and S/D JL nFETs and Fig. 1(b) shows the device schematic. The recessed channel and S/D are highlighted. The experiment started with a GeOI wafer grown by the Smartcut™ technology from Soitec™. After a standard clean, the sample was globally implanted with P ions, which were activated later. Then, the device isolation was carried out. After that, an optimized SF_6 dry etching with high aspect ratio was used for the recessed channel formation, as shown in Fig. 2(a). After smoothing the interface using a surface wet clean, the sample was immediately transferred into an oxidation furnace for GeO_2 growth, followed by Al_2O_3 ALD growth, as shown in Fig. 2(b). After etching away the oxide in the S/D area, a well-calibrated BCl_3/Ar dry etching was used to remove the top Ge layer as the recessed S/D etching. Fig. 2(c-d) show the test recessed S/D structure. Ni was then deposited as the S/D metal contact, followed by an ohmic anneal. Finally, Cr/Au gate metal was deposited. A fabricated device is shown in Fig. 2(e-f). JAM pFETs were also integrated on the same wafer in parallel. The pFETs fabrication was described in our previous work [6]. A bird's eye view of a Ge CMOS inverter is given in Fig. 2(g) and the pFET and nFET components are highlighted.

IV. Results and Discussion

A. Ohmic contacts to n-Ge

High doping concentration (N_D) is normally used to realize a good MS contact. Fig. 3 shows the mechanism of the contact improvement in the recessed S/D structure. The implanted ions' profile in Ge can be approximated by a Gaussian distribution function, as shown in the N_D-depth relation. The peak of the ion distribution is located several nanometers underneath the surface. By etching away the top doped layer above the peak, the N_D in the new surface region can be pushed much higher than before. The Schottky barrier width (W_{SB}) is then significantly reduced, as shown in the band-diagram, thus contact resistance is dramatically decreased. For the ion implantation condition employed in this work, the peak is about 30 nm away from the surface [7]. The recessed S/D process removed about 12 nm Ge layer. Fig. 4(a) shows the I-V curves of two top TLM contacts using Ni and Al for both recessed and non-recessed structures. Great enhancement is observed by this simple recessed process for both Ni and Al. The same I-V curves are redrawn in Fig. 4(b) in linear scale and indicate that only the Ni recessed contact behaves in ohmic. Correspondingly, the contact resistance (R_c) is extracted to be 0.38 Ω·mm and sheet resistance (R_{sh}) to be 90 Ω/□ by the TLM structure shown in Fig. 4(c).

B. nFETs electrical characteristics

The fabricated nFETs have a W_{ch} of 0.8 μm, a T_{ch} of 20 nm, and L_{ch} from 25 to 100 nm. The gate dielectric is composed of 3nm GeO_2 and 8 nm Al_2O_3, corresponding to an EOT of 5.2 nm. Fig. 5 shows the transfer curves of two devices with L_{ch} of 60 and 100 nm. The 60 nm L_{ch} device has a large on-current (I_{on}) of 550 mA/mm ($V_{ds} = V_{gs}-V_{TH} = 1$ V), an I_{on}/I_{off} ratio of 1×10^5 at $V_{ds} = 0.05$ V and a V_{TH} of 0.2 V. The 100 nm L_{ch} device has a smaller I_{on} of 247 mA/mm but steeper SS of 185 mV/dec at $V_{ds} = 0.05$ V. The lowest SS obtained is 117 mV/dec (not shown), corresponding to a mid-gap D_{it} of 4×10^{12} $eV^{-1}cm^{-2}$, indicating a reasonable interface in the nFETs. Fig. 6(a) presents the output characteristics of the same two devices in Fig. 5. The I_{max} of the 60 nm L_{ch} device is 714 mA/mm at $V_{ds} = V_{gs} = 1.5$ V. Fig. 6(b) shows the g_m-V_{gs} for the same device. A record high g_{max} of 590 mS/mm for Ge nFETs is achieved at V_{ds} = 1 V. The peak field-effect mobility is estimated to be 180 cm^2/Vs. Fig. 6(c) shows the low gate leakage current density. Fig 7(a-d) gives the scaling metrics for the nFETs. V_{TH} roll-off and SS degradation are resulted from the short channel effects. g_m and I_{ds} remain constant at smaller L_{ch}, due to velocity saturation. Fig. 8 and Fig. 9 benchmark the I_{ds} and g_m in this work with other published results. We have realized the shortest channel length and a breakthrough in drain current and trans-conductance on Ge nFETs. The I_{max} and g_{max} start to be comparable to Ge pFETs [1-3] and are 5 times of the highest value ever reported on Ge nFETs.

C. CMOS for future

The Ge JL nFETs and pFETs with deeply recessed channels in this work operate in the accumulation mode. Fig. 10 gives the transfer curves of a pFET and an nFET with an L_{ch} of 50 nm at $V_{ds} = 0.5$ V. Both of the E-mode devices have good ON & OFF states and balanced $|V_{TH}| < 0.5$ V.

For a non-ideal oxide/semiconductor (OS) interface [8-10], the E_F at the interface tends to be aligned at the TNL. For the conventional Ge IM pFETs in Fig. 11(a), the channel is n-doped and the E_F tends to move down to the TNL near E_v at the interface. Thus, it's easy to switch from OFF to ON state and realize large drain current Ge IM pFETs. However, for the conventional Ge IM nFETs in Fig 11(b), the E_F in the p-doped channel tends to locate near E_v and thus it's hard to move E_F fully up to the conduction band edge (E_c) and realize a large drain current at a Ge IM nFET. On the contrary, for the JAM nFETs in Fig. 11(c), it's easy for electrons to accumulate in the n-doped channel (the bulk E_F is close to E_C, a small E_F increase would make the number of electrons exponentially increase) and the TNL near E_v also assists the device to be easily switched off. That's why high I_{on} and high I_{on}/I_{off} ratio are achieved in this work. The JAM pFETs in Fig. 11(d) is similar to the IM nFET's case and that's why the JAM pFET in Fig. 10(a) needs a larger gate bias to switch (much larger V_{gs} range than the JAM nFET with a same EOT). Due to the E_F pining in Ge near E_V, only IM pFETs and JAM nFETs could work well in all of the four types of devices (IM pFET & nFET, JAM nFET & pFET) considering both the MS interface for contacts and the OS interface for the channel. Based on this fundamental understanding, we propose a hybrid Ge CMOS structure with an IM pFET and a JAM nFET in Fig. 11(e) for the future Ge CMOS technology development.

V. Conclusion

We present a new recessed channel and S/D process for the Ge CMOS technology development. Breakthroughs in Ge nFETs in terms of the record high I_{max} and g_{max} are reported. Through a fundamental understanding on the Ge's interfaces, a new CMOS structure with an IM pFET and a JAM nFET is proposed, which can be easily demonstrated with a non-ideal OS interface.

VI. Reference

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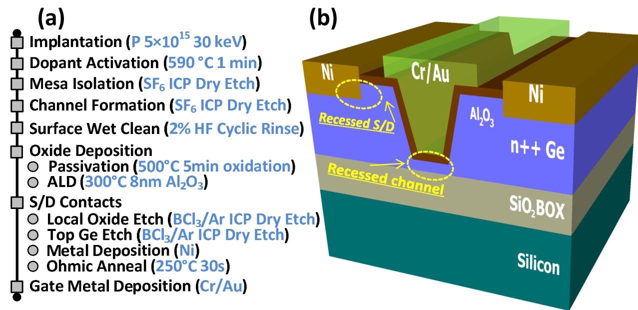

Fig. 1 (a) Key processes in the fabrication of the Ge recessed channel and S/D JL nFET. (b) Device schematic. A GeOI wafer with 180nm Ge, 400nm SiO_2 and Si handle substrate, grown by the Smartcut™ technology from Soitec™, was used. The recessed channel and S/D are highlighted for better illustration.

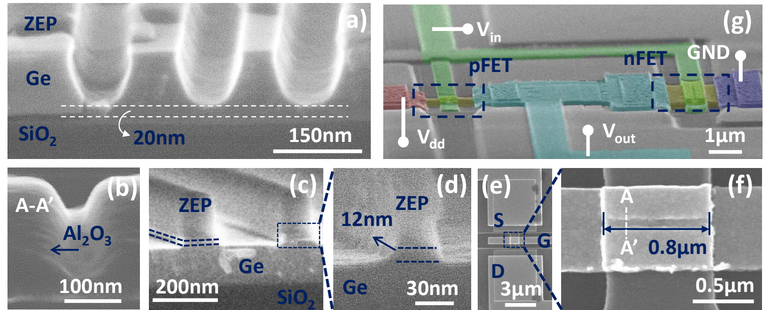

Fig. 2 (a) Test recessed channels, T_{ch} is 20 nm. (b) The shortest 25 nm L_{ch} recessed channel after ALD growth, the Al_2O_3 could be clear observed. (c) Test recessed S/D structure. (d) Zoom of the etched area, 12 nm Ge is removed. (e) Top down view of a fabricated device. (f) Zoom of the gate area in (e). The W_{ch} is 0.8 μm. (g) Bird's eye view of a CMOS inverter. The pFET and nFET are highlighted.

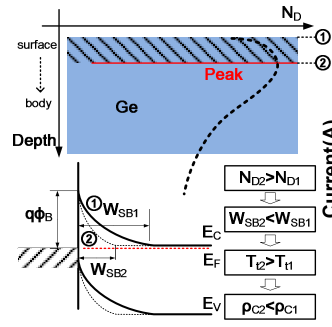

Fig. 3 The contact improvement mechanism in the recessed S/D structure: higher surface doping leads to higher tunneling efficiency, thus lows the resistivity.

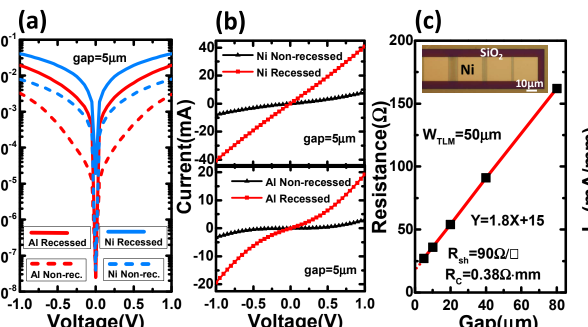

Fig. 4 (a) I-V curves of two top TLM contacts on n-Ge with and without the recessed S/D for Ni and Al. (b) Redrawing of (a) in linear scale, the recessed S/D samples improve a lot, the recessed Ni contact has ohmic behavior. (c) TLM results of the recessed Ni contact. Inserted figure: optical image of the TLM structure.

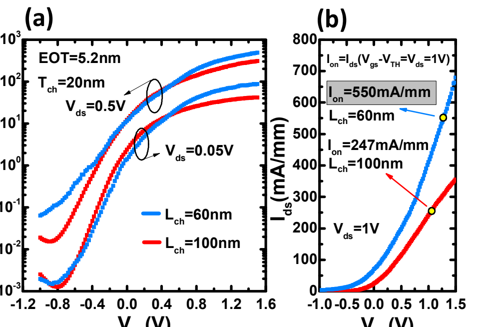

Fig. 5 (a) Transfer curves of two devices with L_{ch}=60 and 100 nm at V_{ds} = 0.05 and 0.5 V. (b) Transfer curves of the same two devices in (a) at V_{ds} = 1 V in linear scale. Highest I_{on} of 550 mA/mm is obtained in the 60 nm L_{ch} device at V_{gs}-V_{TH} = V_{ds} = 1 V.

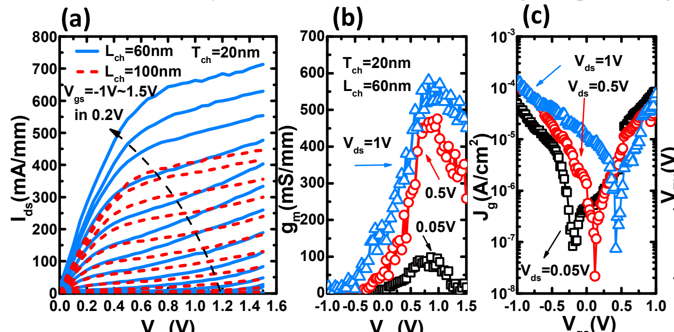

Fig. 6 (a) Output characteristics of the same two devices in Fig. 5(a). Record high I_{max} of 714 mA/mm is obtained. (b) g_m vs V_{gs} relationship of the 60 nm L_{ch} device. Highest g_{max} of 590 mS/mm is archived. (c) Gate leakage current density of the nFETs.

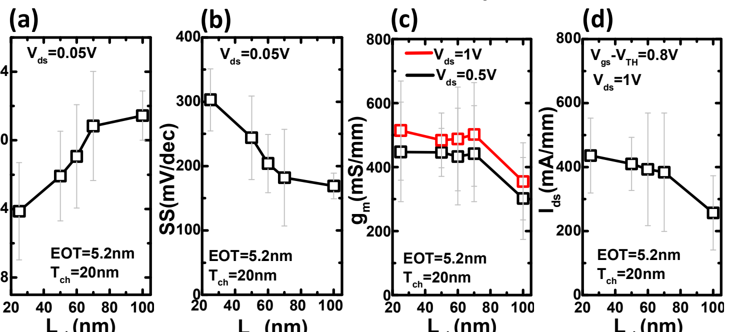

Fig. 7 (a) V_{TH} scaling trend, the V_{TH} is linearly extrapolated at a low V_{ds} of 0.05 V. (b) SS (V_{ds} = 0.05 V) scaling metrics. (c) g_m scaling trend with V_{ds} = 0.5 and 1 V (d) Drain current scaling metrics with V_{gs}-V_{TH} = 0.8 V and V_{ds} = 0.5 V. Error bars show the standard deviation of the measurement over 10 devices at each data point.

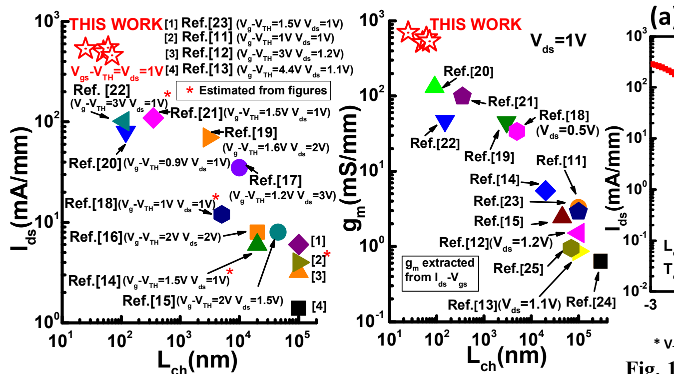

Fig. 8 Drain current benchmarking of the Ge nFETs.

Fig. 9 g_{max} benchmarking of the Ge nFETs.

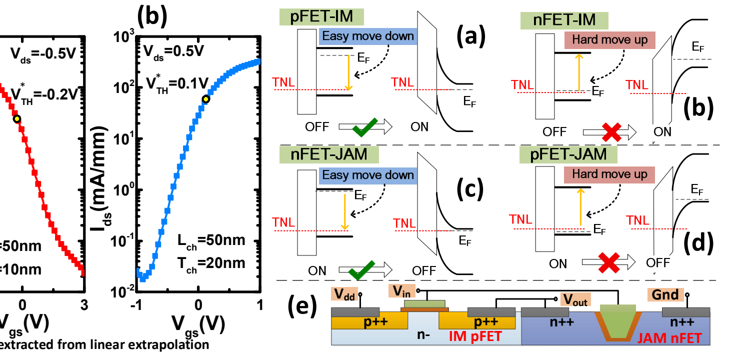

Fig. 10 Transfer curves of Ge CMOS E-mode devices at V_{ds} = 0.5 V. (a) Ge pFET curve. (b) Ge nFET curve.

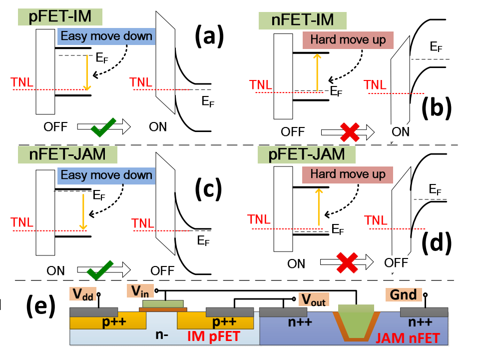

Fig. 11 (a-d) Band-diagrams of Ge IM pFET & nFET, JAM nFET & pFET in device ON and OFF states. (e) A new Ge hybrid CMOS structure.