First Demonstration of Atomic-Layer-Deposited BEOL-Compatible In$_2$O$_3$ 3D Fin Transistors and Integrated Circuits: High Mobility of 113 cm$^2$/V·s, Maximum Drain Current of 2.5 mA/μm and Maximum Voltage Gain of 38 V/V in In$_2$O$_3$ Inverter

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Abstract

In this work, we report the first demonstration of In$_2$O$_3$ 3D transistors coated on fin-structures and integrated circuits by a back-end-of-line (BEOL) compatible atomic layer deposition (ALD) process. High performance planar In$_2$O$_3$ transistors with high mobility of 113 cm$^2$/V·s and record high maximum drain current of 2.5 mA/μm are achieved by channel thickness engineering and post-deposition annealing. High-performance ALD In$_2$O$_3$ based zero-V$_{GS}$-load inverter is demonstrated with maximum voltage gain of 38 V/V and minimum supply voltage (V$_{DD}$) down to 0.5 V. ALD In$_2$O$_3$ 3D Fin transistors are also demonstrated, benefiting from the conformal deposition capability of ALD. These results suggest ALD oxide semiconductors and devices have unique advantages and are promising toward BEOL-compatible monolithic 3D integration for 3D integrated circuits.

Introduction

Indium oxide (In$_2$O$_3$) or doped-In$_2$O$_3$ are being investigated as promising channel materials for back-end-of-line (BEOL) compatible transistors for monolithic 3D integration [1], by both sputtering [2-8] and atomic layer deposition (ALD) [9-12], due to their high mobility, wide bandgap, low variability and high stability. ALD based oxide semiconductors are of special interest due to the atomically smooth surface, ultrathin thickness and the capability of conformal deposition on 3D structures. Recently, high-performance ALD In$_2$O$_3$ transistors have been demonstrated with high drain current over 2 mA/μm in both depletion-mode (D-mode) and enhancement-mode (E-mode) operations. The devices have ultra-scaled channel thickness down to 0.7 nm, high mobility of 91 cm$^2$/V·s, low thermal budget below 400 °C and scalability in P$_{DD}$ environment, which are highly compatible with BEOL process [10].

In this work, the performance of ALD In$_2$O$_3$ transistors are further enhanced by channel thickness ($T_{ch}$) engineering and post-deposition annealing. An optimized $T_{ch}$ is determined to be 2.2-2.5 nm, achieving high mobility of 113 cm$^2$/V·s and record high maximum drain current of 2.5 mA/μm at channel length ($L_{ch}$) of 40 nm and $V_{DS}$=0.7V. A new type of 3D Fin transistors and integrated circuits based on ALD In$_2$O$_3$ are demonstrated for the first time. High-performance ALD In$_2$O$_3$ based zero-V$_{GS}$-load inverter presents maximum voltage gain of 38 V/V and minimum supply voltage (V$_{DD}$) down to 0.5 V. ALD In$_2$O$_3$ 3D Fin transistors coated on SOI fin-structures are also demonstrated, taking advantage of conformal deposition of ALD on 3D structures.

Experiments

Fig. 1 presents the schematic diagram of a planar back-gate In$_2$O$_3$ transistor, using the same structure as previously reported in [9, 10], which is used for circuit demonstration. The gate stack consists of 40 nm Ni as gate metal, 5 nm HfO$_2$ as gate dielectric, 0.5-3.5 nm In$_2$O$_3$ as semiconducting channels and 80 nm Ni as source/drain electrodes. The device fabrication process is similar to [9, 10]. The fabricated devices were annealed in O$_3$, N$_2$ or forming gas (FG, 96% N$_2$/4% H$_2$) for 30 s at different temperatures from 250 °C to 350 °C according to the optimized annealing conditions achieved in [10]. Fig. 2(a) shows the photo image of a fabricated In$_2$O$_3$ zero-V$_{GS}$-load inverter with LD$_{ch}$=3 μm stage ring oscillator. The circuit diagram of the In$_2$O$_3$ zero-V$_{GS}$-load inverter is shown in Fig. 2(b). D-mode and E-mode transistors could be achieved by threshold voltage ($V_t$) engineering such as plasma annealing, as shown in Fig. 7. Average $μ_{FE}$ > 100 cm$^2$/V·s is achieved compared to other ALD based oxide semiconductors [9-16]. Such high mobility is achieved by $T_{ch}$ engineering and post-deposition annealing, as shown in Fig. 7. Average $μ_{FE}$ > 100 cm$^2$/V·s is achieved with $T_{ch}$ of 2.2-2.5 nm at optimized annealing conditions. $μ_{FE}$ decreases rapidly with $T_{ch}$ below 1 nm, mostly likely due to the enhanced surface scattering and quantum confinement effect on band structure [11]. $μ_{FE}$ decreases at $T_{ch}$ above 3 nm due to the higher carrier concentration and weaker gate electrostatic control, as also shown in $V_t$ versus $T_{ch}$ in Fig. 8. Post-deposition annealing for the reduction of oxygen vacancies in as-deposited films is needed to tune the $V_t$ of devices with $T_{ch}$ above 2 nm to obtain sufficiently high on/off ratio. Fig. 9 shows $T_{ch}$-dependent SS extracted from as-deposited devices and optimized annealing conditions, exhibiting SS close to the thermal limit of 60 mV/dec at room temperature at $T_{ch}$=1 nm. Fig 10 and Fig. 11 present the Id-Vgs and Id-Vds characteristics of an In$_2$O$_3$ Inverter with $T_{ch}$ of 1 nm and $V_{DD}$=2.2 V, exhibiting record high maximum Io of 2.5 mA/μm under V$_{DD}$=0.7V and V$_{DS}$=4 V with optimized $T_{ch}$ and annealing conditions.

Fig. 12 presents $V_{out}$ versus $V_{in}$ curve of an In$_2$O$_3$ zero-V$_{GS}$-load inverter with LD$_{ch}$ of 0.3 μm at different V$_{DD}$ from 2 V down to 0.5 V, showing well-behaved voltage transfer characteristics. The voltage gains are given in Fig. 13, achieving maximum voltage gain of 38 V/V at V$_{DD}$ of 2 V. The midpoint voltage of the In$_2$O$_3$ zero-V$_{GS}$-load inverter can be engineered by tuning the load resistance and varying the channel length of the D-mode transistor, as illustrated in Fig. 14, providing the essential approach for V$_{DD}$ and midpoint voltage engineering accordingly. Therefore, sufficiently large noise margin (NM) can be achieved, as shown in Fig. 15.

Fig. 16 shows the SEM image of an In$_2$O$_3$ 3D Fin transistor with top-gate structure, capturing the gate metal, source/drain contacts and the fin-structures. Fig. 17 presents the TEM image and EDX mapping of an In$_2$O$_3$ 3D Fin transistor. ALD In$_2$O$_3$ channel with $T_{ch}$ of 1.5 nm is conformally coated on top of SOI fin-structures with fin height of 180 nm and fin pitch of 130 nm. Fig. 18 shows Id-V$_{DS}$ characteristics of an In$_2$O$_3$ 3D Fin transistor with LD$_{ch}$ of 2 μm and $T_{ch}$ of 1.5 nm, exhibiting well-behaved transfer characteristics. Fig. 19 shows the corresponding Id-V$_{DS}$ characteristics with maximum Io of 180 μA/μm, normalized by device width, which is about 2 times larger that from top-gate planar In$_2$O$_3$ counterpart. The 3D Fin structure provides an effective approach to increase the drive current without increasing the device area. The ultra-thin channel thickness and top-gate non-self-align structure with a large link resistance make Io smaller than those from back-gate planar devices.

Conclusion

In summary, high-performance 3D Fin transistors and integrated circuits based on BEOL compatible oxide semiconductors by ALD are demonstrated for the first time. High mobility of 113 cm$^2$/V·s and record high maximum drain current of 2.5 mA/μm are achieved. The demonstration of 3D devices and integrated circuits suggest ALD oxide semiconductors and devices have their unique advantages over sputtering films and are promising toward BEOL-compatible monolithic 3D integration for 3D integrated circuits.

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Reference


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Fig. 1. Schematic diagram of a planar In$_2$O$_3$ transistor with 5 nm HfO$_2$ as gate dielectric and T$_{ch}$ from 0.5 nm to 3.5 nm.

Fig. 2. (a) Photo image of an In$_2$O$_3$ zero-V$_{GS}$-load inverter in a 5-stage ring oscillator. (b) Circuit diagram of the In$_2$O$_3$ zero-V$_{GS}$-load inverter.

Fig. 3. I$_D$-V$_{GS}$ characteristics of a planar In$_2$O$_3$ transistor with L$_{ch}$ of 1 µm and T$_{ch}$ of 2.2 nm with O$_2$ annealing.

Fig. 4. I$_D$-V$_{DS}$ characteristics of a planar In$_2$O$_3$ transistor with L$_{ch}$ of 1 µm and T$_{ch}$ of 2.2 nm with O$_2$ annealing.

Fig. 5. $\mu_{FE}$ versus V$_{GS}$ extracted from the maximum g$_m$ at V$_{DS}$ of 0.05 V from transfer curve.

Fig. 6. $\mu_{FE}$ versus V$_{GS}$ extracted from the g$_m$ from output curve. The consistency of $\mu_{FE}$ and $\mu_{eff}$ is further confirmed by $\mu_{Haille}$.\[8\]

Fig. 7. $\mu_{FE}$ versus T$_{ch}$ extracted from as-deposited devices and devices with optimized annealing conditions.

Fig. 8. V$_{T}$ versus T$_{ch}$ extracted from as-deposited devices and devices with different annealing conditions.

Fig. 9. SS versus T$_{ch}$ extracted from as-deposited devices and devices with optimized annealing conditions.

Fig. 10. I$_D$-V$_{GS}$ characteristics of an In$_2$O$_3$ transistor with L$_{ch}$ of 40 nm and T$_{ch}$ of 2.2 nm with O$_2$ annealing at 350 °C.

Fig. 11. I$_D$-V$_{DS}$ characteristics of an In$_2$O$_3$ transistor with L$_{ch}$ of 40 nm and T$_{ch}$ of 2.2 nm with O$_2$ annealing at 350 °C.

Fig. 12. V$_{out}$ versus V$_{in}$ of an In$_2$O$_3$ zero-V$_{GS}$-load inverter with L$_{ch}$ of 0.3 µm at different V$_{DD}$.

Fig. 13. Voltage gain of the In$_2$O$_3$ zero-V$_{GS}$-load inverter in Fig. 12 at different V$_{DD}$.

Fig. 14. V$_{out}$ versus V$_{in}$ of In$_2$O$_3$ zero-V$_{GS}$-load inverters with different L$_D$ at V$_{DD}$ of 2 V.

Fig. 15. Noise margin of the In$_2$O$_3$ zero-V$_{GS}$-load inverter as in Fig. 12 at V$_{DD}$ of 0.7 V.

Fig. 16. SEM image of an In$_2$O$_3$ 3D Fin transistor with top-gate structure.

Fig. 17. (a) TEM image of a new type of 3D In$_2$O$_3$ 3D Fin transistor with top-gate structure.

Fig. 18. I$_D$-V$_{GS}$ characteristics of an In$_2$O$_3$ 3D Fin transistor with L$_{ch}$ of 2 µm and T$_{ch}$ of 1.5 nm.

Fig. 19. I$_D$-V$_{GS}$ characteristics of an In$_2$O$_3$ 3D Fin transistor with L$_{ch}$ of 2 µm and T$_{ch}$ of 1.5 nm.

Fig. 19. SEM image of a new type of 3D In$_2$O$_3$ 3D Fin transistor with top-gate structure and In$_2$O$_3$ top-gate structure. SiO$_2$ fin structures were fabricated by SEMATECH.