Ultra-Fast Operation of BEOL-Compatible Atomic-Layer-Deposited In_2O_3 Fe-FETs: Achieving Memory Performance Enhancement with Memory Window of 2.5 V and High Endurance > 10^9 Cycles without V_T Drift Penalty

Zehao Lin, Mengwei Si, and Peide D. Ye
Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, U.S.A. *Email: yep@purdue.edu

Abstract

In this work, we report the ultra-fast operation of back-end-of-line (BEOL) compatible Fe-FETs with atomic layer deposition (ALD) In_2O_3 and $HfZrO_2$ (HZO) as channel semiconductor and ferroelectric gate insulator with channel length (L_{ch}) scaled down to 7 nm, enabled by ultra-fast I-V (UFIV) and pulse I-V measurements. It is found that device memory characteristics benefit from fast operation down to 10 ns level, by a suppression of trapping effect while maintaining fast FE switching speed. High memory performance is achieved, exhibiting a wide memory window of 2.5 V and a high endurance exceeding 10^9 cycles without V_T drift penalty. These results suggest that oxide semiconductor Fe-FETs are promising toward monolithic 3D integration for in-memory computing at ultra-fast operation speed.

Introduction

Ferroelectric field-effect transistor (Fe-FET) based on ALD-grown ferroelectric hafnium oxide (HfO_2) [1] is a promising non-volatile memory device candidate due to the superior performance including scalability, fast operation speed [2-5], as well as CMOS and back-end-of-line (BEOL) compatibility [6,7]. Recently, oxide semiconductor Fe-FETs with BEOL compatible oxide semiconductor channels such as In_2O_3 [8], W-doped In_2O_3 [9], and Indium-Gallium-Zinc-Oxide (IGZO) [10] have attracted great attention for their promising applications in monolithic 3D integration toward in-memory computing. However, despite of the decent reliability of FE-HfO_2 film, Si Fe-FET suffers from relatively poor endurance on the level of 10^4-10^6 cycles [11,12] and V_T drift [13,14], which is proved to be rooted in charge trapping effects on multiple interfaces in a FE/dielectric (DE)/semiconductor system [15-18], as shown in Fig. 1. The utility of oxide semiconductor channel without an interfacial layer is contributed to the enhanced endurance to 10^8-10^{10} [19-21], but these devices still suffer from strong V_T drift due to the charge trapping. How to suppress the trapping effect turns out to be essential for high-performance and reliable embedded non-volatile memories (eNVMs).

In this work, we report ultra-fast operation of BEOL-compatible Fe-FETs with ALD In_2O_3 and HZO as channel semiconductor and ferroelectric gate insulator with L_{ch} from 800nm down to 7 nm, utilizing ultra-fast I-V (UFIV) and pulse I-V measurements. It is found that UFIV scheme enables an enhancement of memory performance, resulted from a suppression of FE-unrelated trapping/de-trapping process, achieving a memory window boost to 2.5 V. Co-optimized with other operation conditions by V_{DS} reduction and utilizing trapezoidal pulses, a high endurance exceeding 10^9 cycles without V_T drift penalty is achieved.

Experiments

Fig. 2 and 3 show the device schematic diagram and fabrication process flow of BEOL compatible ALD In_2O_3 Fe-FETs. The details of fabrication process can be referred to our previous work [8]. A control group of devices w/o Al_2O_3 interfacial layer (IL) is also included. Demonstration of ultra-short 7nm L_{ch} devices can be found at TEM images reported previously [8]. Fig. 4 presents P-V loop of FE-HZO film w/ and w/o Al_2O_3 IL. A degradation of ferroelectricity is observed in stack w/o Al_2O_3 IL, because less FE-phase (O-phase) portion is formed in FE HZO without induced strain from top Al_2O_3 capping during annealing for FE formation.

Results and Discussion

Fig. 5 illustrates the waveforms applied using two different fast measurement schemes: UFIV and pulse I-V. An B1530A WGFMU is exploited to generate waveform and perform ultra-fast measurements with averaging time down to 10 ns. The shortest measurement delay (MD) for UFIV is 20 ns with rise time (RT) of 10 ns to achieve decent resolution. The average time (AT) is fixed at 10 ns for UFIV and 100 ns for pulse I-V unless elsewhere stated, which are minimum times to achieve a sufficient signal resolution. Fig. 6 rules out the appearance of ΔV_T from fast test conditions by measuring a MOSFET with negligible hysteresis. Fig. 7 displays the corresponding I_D-V_{GS} characteristics of an ultra-scaled ALD In_2O_3 Fe-FET with L_{ch} of 7 nm and Al_2O_3 of 1 nm at V_{DS} of 0.1 V, utilizing UFIV scheme with MD of 20 ns and V_{GS} step of 0.2V. A wide memory window (MW) of 2.5 V is achieved, greater than that of 2.2 V at conventional DC test with MD and AT of about ms level [8]. Fig. 8 shows an evolution of I_D-V_{GS} characteristics with MD from 20 ns to 200 µs of an In_2O_3 Fe-FET with L_{ch} of 200 nm at V_{DS} of 0.1 V, demonstrating a clear MW reduction with longer MD. Fig. 9(a) and 9(b) plot the dependence of MW on MD under UFIV tests for Fe-FETs w/ and w/o Al_2O_3 IL, respectively, illustrating that the reduction of MW with increasing MD is universal. This phenomenon can be interpreted as a suppression of FE/DE interface and bulk defects trapping/de-trapping process by shortening MD. The FE switching assisted by leakage current through DE or IL to satisfy charge balance condition at FE/DE interface, is relatively slow as shown in Fig. 9(a). For devices w/o DE IL, charge primarily gets trapped at FE/In_2O_3 interface, while the charge balance condition can be quickly satisfied, and thereby showing reduced L_{ch} dependence in Fig. 9(b). Longer channel devices show more MD dependence since the traps in the middle of the devices take longer time to respond. The reduction of MW of Fe-FETs w/o IL compared with that with IL is mainly because of reduction of ferroelectricity of HZO film, as illustrated in Fig. 4. It is also observed that the short-channel devices have enhanced MW than long-channel ones [8], indicating that trapping is less effective in short Fe-FETs.

Fig. 10 presents a comparison of MW for UFIV and pulse scheme of a Fe-FET with L_{ch} of 7 nm and Al_2O_3 of 1 nm at V_{DS} of 0.1 V. Pulse scheme shows a smaller MW in comparison to UFIV and similar weak dependence on MD from 500 ns to 50 µs, because pulse scheme has de-trapping during pulse base time (BT) and relaxation of FE during pulse falling time. Fig. 11 shows that such phenomenon is observed at a wide range of L_{ch} at V_{DS} of 0.1 V with MD of 500 ns. Less MW difference at long-channel devices is observed, which is likely a result of MW reduction itself at long-channel devices in general. Fig. 12 demonstrates the negligible dependence of MW on V_{DS} for both long-channel and short-channel devices under UFIV tests. This suggests that a reduced V_{DS} would be preferred with the same MW and better reliability characteristics by suppressing drain-induced degradation.

Fig. 13 illustrates the waveform sequence utilized for endurance test. UFIV scheme with MD of 300 ns is used to minimize measurement-induced degradation. Trapezoidal pulse instead of square pulse is utilized to suppressing trapping and defects generation under high bias while maintaining sufficient FE switching. V_{DS} is set to 0.03 V to minimize potential drain-induced degradation, and pulse BT is set to 500 ns for de-trapping unless stated elsewhere. Fig. 14 shows endurance performance of ALD In_2O_3 Fe-FETs with L_{ch} of 50 and 7 nm at erase/program voltage of ±2.4 V. A high endurance > 10^9 cycles for both devices is achieved without penalty of V_T drift, demonstrating the suppression of trapping and other degradation factors by co-optimization of operation conditions beneficial for device reliability. The high endurance with flat V_T drift provides an important promise for the BEOL Fe-FET development.

Conclusion

In conclusion, ultra-fast operation of BEOL-compatible ALD In_2O_3 Fe-FETs with L_{ch} down to 7 nm, enabled by ultra-fast I-V and pulse I-V measurement schemes, is systematically investigated. We achieved an enhancement of MW to 2.5 V by reducing staying time in UFIV down to 20 ns, and boosted endurance performance to 10^9 cycles without V_T drift penalty. Ultra-fast operation to ~ few 10 ns is found to be beneficial to Fe-FET's memory performance by suppressing charge trapping while with sufficient FE switching at a fast speed.

Acknowledgement

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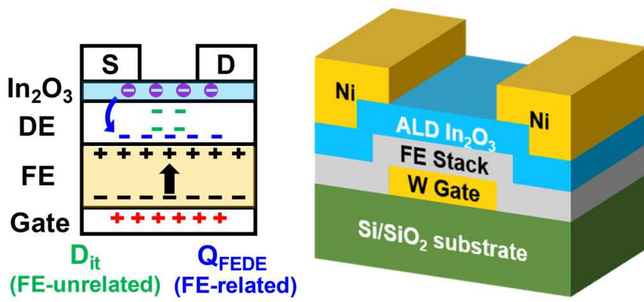
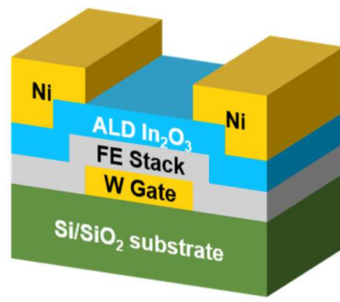
Reference: [1] J. Muller et al., Nano Lett., vol. 12, p. 4318, 2012. [2] S.S. Cheema et al., Nature p. 478, 2020. [3] X. Lyu et al., in VLSIT, p. T4.4, 2019. [4] M. Si et al., Appl. Phys. Lett., vol. 115, p. 072107, 2019. [5] X. Lyu et al., IEDM, p. 342, 2019. [6] J. Hur et al., IEEE TED, vol. 68, p. 3176, 2021. [7] K. Tahara et al., VLSI, p. T7.3, 2021. [8] Z. Lin et al., IEDM, p. 386, 2021. [9] S. Dutta et al., IEDM, p. 801, 2020. [10] C. Sun et al., VLSI, p. T7.4, 2021. [11] J. Muller et al., VLSIT, p. 25, 2012. [12] K.T. Chen et al., EDL, vol. 40p. 399, 2019. [13] T. Ali et al., IEDM, pp. 28.7.1, 2019. [14] A. Sharma et al., IEDM, p. 391, 2020. [15] K. Ni et al., IEEE TED, vol. 65, p. 2461, 2018. [16] K. Toprasertpong et al., IEDM, p. 570, 2019. [17] M. Si et al., IEEE TED, vol. 68, p. 5108, 2021. [18] N. Tasneem et al., IEDM, p. 122, 2021. [19] A.J. Tan et al., EDL, 2021. [20] S. Dutta et al., IEDM, p.374, 2021. [21] Z. Liang et al., IEDM, p.382, 2021.





- ❑ Solvent clean of SiO_2/Si substrate
- ❑ 40 nm W gate sputtering
- ❑ ALD FE gate stack at 200 °C
  - ❖ 8 nm HZO (w/ & w/o Al_2O_3 IL)
- ❑ RTA in N_2 at 350 °C for 10 mins
- ❑ ALD 1.5 nm In_2O_3 at 225 °C
- ❑ 40 nm Ni S/D contact evaporation
  - ❖ Two-step e-beam lithography
- ❑ Channel isolation and defining
- ❑ RTA 300 °C in O_2 for 1 min

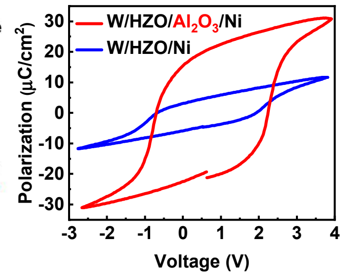


Fig. 1. Schematic diagram of charge distribution in a typical Fe-FET with DE IL.

Fig. 2. Schematic diagram of a BEOL-compatible In_2O_3 Fe-FET.

Fig. 3. Fabrication process flow of the In_2O_3 Fe-FETs. Control group w/o Al_2O_3 IL is utilized.

Fig. 4. P-V loops of representative capacitors w/ and w/o Al_2O_3 IL. HZO w/o IL capping representing degraded ferroelectricity.

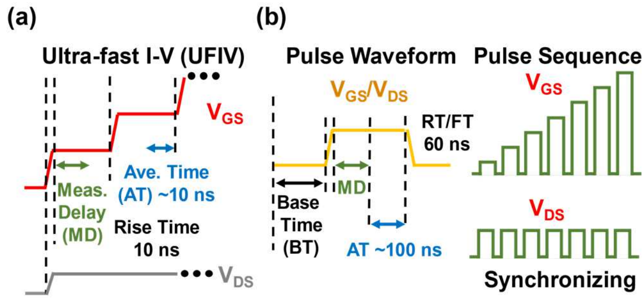


Fig. 5. Waveform of two ultra-fast test schemes: (a) ultra-fast I-V and (b) pulse I-V. The minimum measurement delay is 20 ns for UFIV and ~200 ns for pulse I-V. The average time is fixed at 10 ns for UFIV and 100 ns for pulse I-V unless elsewhere stated. UFIV is measured by V_{GS} fast sweep with each step of 0.1 V or 0.2 V. The total sweep time for 2V as Fig.8 below is about 500 ns.

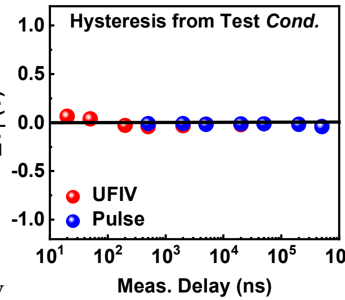


Fig. 6. Characterization of hysteresis in the transfer curve of In_2O_3 MOSFETs, where ΔV_T is negligible.

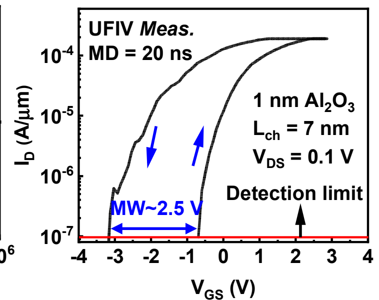
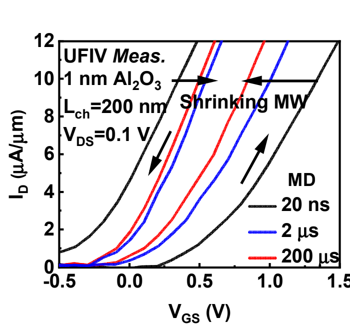
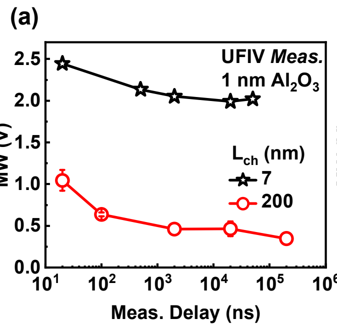


Fig. 7. I_D-V_{GS} characteristics of an ALD In_2O_3 Fe-FET with L_{ch} of 7 nm, Al_2O_3 of 1 nm at V_{DS} of 0.1 V under UFIV with MD=20 ns and total sweep time 800 ns, highlighting a memory window of 2.5 V.





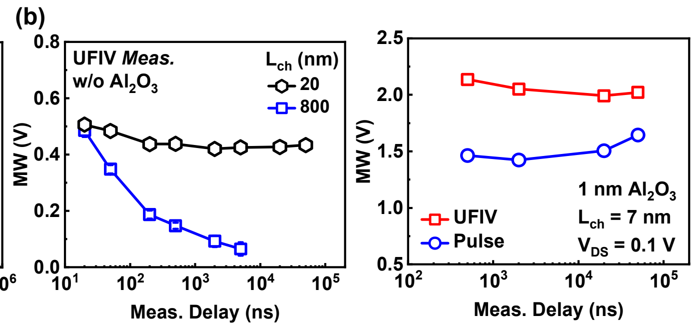


Fig. 8. I_D-V_{GS} characteristics of a Fe-FET with L_{ch} of 200 nm at V_{DS} of 0.1 V with various MD, showing a clear MW shrinking. The total sweep time is ~500 ns.

Fig. 9. Dependence of MW on MD under UFIV scheme for Fe-FETs (a) w/ and (b) w/o Al_2O_3 IL, respectively, demonstrating MW reduction with increasing MD.

Fig. 10. MW dependence on MD for UFIV and pulse I-V scheme of a Fe-FET with L_{ch} of 7 nm and Al_2O_3 of 1 nm at V_{DS} of 0.1 V.

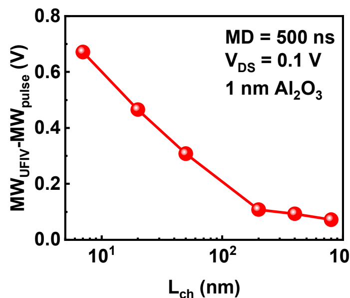


Fig. 11. Dependence of MW using UFIV and pulse schemes on L_{ch} with Al_2O_3 of 1 nm at V_{DS} of 0.1 V. MD is fixed at 500 ns for both schemes.

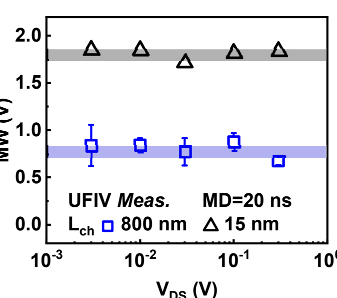


Fig. 12. MW dependence on V_{DS} of Fe-FETs with L_{ch} of 800 nm and 15 nm at V_{DS} of 0.1 V.

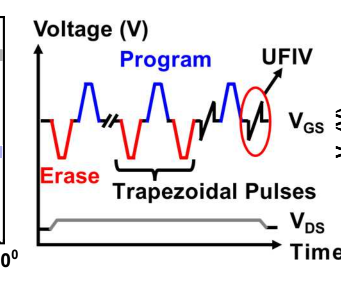


Fig. 13. Pulse sequence in endurance test. UFIV scheme with MD of 300 ns is utilized. Trapezoidal pulse is exploited with pulse interval of 500 ns at V_{DS} of 0.03 V.

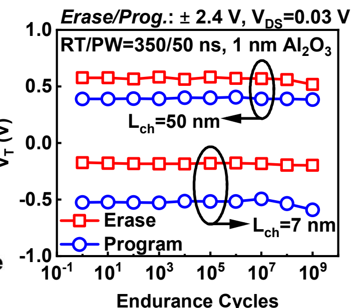


Fig. 14. Endurance performance of short-channel In_2O_3 Fe-FETs with L_{ch} of 50 nm and 7 nm at V_{DS} of 0.1 V, highlighting > 10^9 cycles endurance without V_T drift. V_T of 7 nm device shifts to negative due to short-channel effects.