Thermal Studies of BEOL-compatible Top-Gated Atomically Thin ALD In$_2$O$_3$ FETs
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Abstract
In this work, we investigate the thermal issues of top-gated (TG), ultrathin, atomic layer deposition (ALD) grown, back-end-of-line (BEOL) compatible indium oxide (In$_2$O$_3$) transistors with different substrates under different power conditions. The device is illuminated by high-speed LED pulses, and a synchronized charge coupled device (CCD) camera is employed to capture the surface reflectance. Fig. 5 reveals the working mechanism in time domain. As a V$_{DS}$ pulse starts, the device is turned OFF and therefore heated up/ cooled down. After the steady-state is reached, TR signals are captured as active/passive images. This process is repeated numerous times, and the difference between the active and passive images is averaged repeatedly to maximize the signal-to-noise (SNR) ratio as presented in Fig. 6. The resultant image of reflectance change is transformed into a temperature scale through dividing by the TR coefficient of the surface material (C$_{TH}$ = $-5 \times 10^5$ K$^{-1}$) and calibration to obtain the final thermal image [11].

Figs. 7–9 manifest the channel region of steady-state $\Delta T$ of TG In$_2$O$_3$ transistors with $L_{ch}$ of 400 nm, $W_A$ of 2 $\mu$m, and SiO$_2$/Si substrate at power density of 2.44 kW/mm$^2$, sapphire substrate at 2.65 kW/mm$^2$, and HR Si substrate at 3.00 kW/mm$^2$, respectively. The $\Delta T$ values are in excellent agreement to $\Delta T$ distribution with experimental results. By thermal engineering, TG In$_2$O$_3$ transistors with channel thickness of 1.8 nm and high drain current ($I_D$) up to 2.65 mA/µm are achieved.

Introduction
Oxide semiconductors have been explored as promising channel materials for BEOL logic and memory applications recently [1–9], where indium oxide (In$_2$O$_3$) [1–4] and doped indium oxide [5–9] are of special interest due to their outstanding properties including homogeneous wafer-scale growth, ambient stability, high mobility, atomically smooth surface roughness, and low thermal budget BEOL compatibility for monolithic 3-D integration. On the other hand, most demonstrated In$_2$O$_3$ transistors use a back-gated (BG) design [1–3] due to the difficulty of forming a high-quality interface between the high-k dielectric layer and In$_2$O$_3$ channel, as well as SHE related thermal issues. However, for practical applications, TG devices are especially desired.

To understand and resolve the self-heating issue, in this work, an ultrathin high-resolution thermo-reflectance imaging technique is introduced to observe and visualize the SHE and temperature increase of TG In$_2$O$_3$ transistors with different substrates under different power density conditions. Moreover, thermal simulations are performed and match well with the experimental measurements. The $\Delta T$ of In$_2$O$_3$ devices with highly resistive Si (resistivity ~ $10^5 \Omega \cdot $ cm) and $\kappa$ = 142 W·m$^{-1}$·K$^{-1}$ [10] substrates is reduced by a factor of 6 compared to SiO$_2$/Si substrates. Therefore, an exceptionally high $I_D$ of 2.65 mA/µm is achieved with 1.8-nm-thick TG In$_2$O$_3$ devices by employing HR Si as the substrate to substantially alleviate the SHE.

Device Fabrication and Performance
Fig. 1 presents the schematic diagram of TG In$_2$O$_3$ transistors. After substrate solvent cleaning, 45 nm of Ni was deposited by e-beam evaporation to form the source/drain (S/D). The 1.5–1.8 nm In$_2$O$_3$ channel was grown by ALD at 225 °C and isolated by an Ar/BCl$_3$ dry etch process, and the 6.4 nm HfO$_2$ dielectric stack was formed by ALD at 120 °C. The top gate metal of 50 nm Ni was deposited finally followed by a rapid-thermal-annealing (RTA) treatment at 200–235 °C in O$_2$ ambient.

Fig. 2 exhibits the transfer characteristics of a long-channel TG In$_2$O$_3$ device with channel length ($L_{ch}$) of 400 nm on SiO$_2$/Si substrate after annealing at 200 °C, showing an $I_D$/$L_{ch}$ ratio of more than 7 orders and subthreshold slope (SS) of 163 mV/dec. Fig. 3(a) shows the output characteristics of a short-channel transistor with $L_{ch}$ of 50 nm on SiO$_2$/Si substrate after oxygen annealing at 230 °C. A maximum $I_D$ of 875 $\mu$A/µm at $V_{DS}$ of 1 V is demonstrated, exceeding the previous report of 570 $\mu$A/µm [2]. However, it is unfeasible to achieve $I_D$ values as high as 2.2 $\mu$A/µm that have been shown with BG transistors [1] using traditional SiO$_2$/Si substrates, since SHE starts to degrade the device performance when larger $L_{ch}$ is applied. As shown in Fig. 3(b), higher $I_D$ conducts when larger $V_{DS}$ is applied. However, it is unfeasible to achieve $I_D$ values as high as 2.2 $\mu$A/µm that have been shown with BG transistors [1] using traditional SiO$_2$/Si substrates, since SHE starts to degrade the device performance when larger $L_{ch}$ is applied.

Thermo-Reflectance Measurement and Thermal Engineering
To quantitatively investigate and address the SHE, an ultrathin high-resolution TR measurement system is introduced with the setup illustrated in Fig. 4. Periodic $V_{DS}$ pulses are applied to the device under test, and a direct-current (DC) supply provides a constant gate-to-source (V$_{GS}$) bias. The device is also illuminated by high-speed LED pulses, and a synchronized charge coupled device (CCD) camera is employed to capture the surface reflectance. Fig. 5 reveals the working mechanism in time domain. As a $V_{DS}$ pulse starts, the device is turned ON/OFF and therefore heated up/ cooled down. After the steady-state is reached, TR signals are captured as active/passive images. This process is repeated numerous times, and the difference between the active and passive images is averaged repeatedly to maximize the signal-to-noise (SNR) ratio as presented in Fig. 6. The resultant image of reflectance change is transformed into a temperature scale through dividing by the TR coefficient of the surface material (C$_{TH}$ = $-5 \times 10^5$ K$^{-1}$) and calibration to obtain the final thermal image [11].

Figs. 7–9 manifest the channel region of steady-state $\Delta T$ of TG In$_2$O$_3$ transistors with $L_{ch}$ of 400 nm, $W_A$ of 2 $\mu$m, and SiO$_2$/Si substrate at power density of 2.44 kW/mm$^2$, sapphire substrate at 2.65 kW/mm$^2$, and HR Si substrate at 3.00 kW/mm$^2$, respectively. The $\Delta T$ values for sapphire and HR Si substrates are roughly 2.7 and 6 times smaller than that for SiO$_2$/Si, indicating that the SHE can be mostly eliminated by utilizing HR Si as the substrate.

To verify the TR measurement results, thermal simulation with a finite-element method is carried out through COMSOL. The model design, which is similar to the discussed In$_2$O$_3$ TG transistors, and its mesh build-up are illustrated in Fig. 11. The red square in Fig. 11 denotes the area of interest, and a false-color image of the corresponding area is plotted in Fig. 12. Fig. 13 reveals the simulated result with SiO$_2$/Si substrate and power density of 2.44 kW/mm$^2$ (same conditions as Fig. 7). To compare the simulation results with the TR measurements, the area of interest in Fig. 7 is shown in Fig. 14 in a similar fashion to Fig. 13, and their cross-sections are plotted in Fig. 15. It can be seen from Figs. 13–15 that the simulation and experimental results are in excellent agreement. The $\Delta T$ values of TG In$_2$O$_3$ transistors with the three different substrates at various power conditions are plotted in Fig. 6. The results show a clear correlation between increasing thermal conductivity of the substrate material and decreasing $\Delta T$ (SiO$_2$/Si < HR Si < sapphire).

Conclusion
In summary, the serious SHE limitation in TG In$_2$O$_3$ transistors is greatly mitigated by thermal management with the understanding of self-heating issue through TR measurement. By thermal engineering and RC modulation, ultrahigh $I_D$ of 2.65 mA/µm is achieved in a TG In$_2$O$_3$ transistor with atomically thin channel of 1.8 nm. The work points out a clear route to develop BEOL-compatible high-k materials such as ALD AIN to replace SiO$_2$ for 3D monolithic integration.

The work is supported by ONR N00014-11-1038, DARPA ASCENT and AFOSR. C. Wilk is with BASIS Scottsdale. C. Wilk is with BASIS Scottsdale.

References:
Fig. 1. Schematic diagram of TG In$_2$O$_3$ transistors with different substrates. The unit of thermal conductivity ($\kappa$) is W m$^{-1}$ K$^{-1}$.

Fig. 2. Transfer characteristics of a TG In$_2$O$_3$ transistor after O$_2$ annealing at 200 $^\circ$C with L$_{ch}$ of 400 nm, SiO$_2$/Si substrate.

Fig. 3. Output characteristics of a TG In$_2$O$_3$ transistor after O$_2$ annealing at 230 $^\circ$C with L$_{ch}$ of 80 nm, SiO$_2$/Si substrate, and V$_{0S}$ of (a) 1.0 V and (b) 1.6 V. The curves in (b) shows severe SHE at large V$_{0S}$ with high I$_D$.

Fig. 4. Schematic illustration of the high-resolution thermo-reflectance (TR) imaging equipment in time domain.

Fig. 5. Working mechanism of the high-resolution TR imaging equipment in time domain.

Fig. 6. Transformation from TR signal to a temperature scale.

Fig. 7. Temperature increase of a TG In$_2$O$_3$ transistor with SiO$_2$/Si substrate and power density of 2.44 kW/mm$^2$.

Fig. 8. Temperature increase of a TG In$_2$O$_3$ transistor with sapphire substrate and power density of 2.65 kW/mm$^2$.

Fig. 9. Temperature increase of a TG In$_2$O$_3$ transistor with HR Si substrate and power density of 3.00 kW/mm$^2$.

Fig. 10. Cross-sections of temperature increase of TG In$_2$O$_3$ transistors with different substrates normalized by power density.

Fig. 11. Model design and mesh build-up of a TG In$_2$O$_3$ device for thermal simulation with a finite-element method.

Fig. 12. A false-color image of a fabricated TG In$_2$O$_3$ device with L$_{ch}$/W$_{ch}$ of 0.4 / 2 $\mu$m.

Fig. 13. Simulation result of a TG In$_2$O$_3$ device with L$_{ch}$ of 400 nm and W$_{ch}$ of 2 $\mu$m.

Fig. 14. TR measurement of a TG In$_2$O$_3$ device with L$_{ch}$ of 400 nm and W$_{ch}$ of 2 $\mu$m.

Fig. 15. Cross-sections of the simulated and experimental results of temperature increase.

Fig. 16. $\Delta T$ extraction of TG In$_2$O$_3$ devices with different substrates and power density.

Fig. 17. $R_C$ decreases with increasing $V_{GS}$–$V_T$ due to carrier concentration modulation.

Fig. 18. (a) Transfer and (b) output characteristics of a TG In$_2$O$_3$ transistor with T$_{ch}$ of 1.8 nm, L$_{ch}$ of 80 nm, and HR Si substrate after O$_2$ annealing at 235 $^\circ$C achieving maximum I$_D$ of 2.65 mA/µm.