Ultrahigh Bias Stability of ALD In_2O_3 FETs Enabled by High Temperature O_2 Annealing

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Abstract

In this work, we systematically studied the temperature dependent electrical performance of atomic-layer-deposited (ALD) indium oxide (In_2O_3) transistors. Both enhancement-mode (E-mode) and depletion-mode (D-mode) In_2O_3 FETs are demonstrated by high temperature O_2 annealing at 400 °C with maximum drain current over 2 mA/μm, on/off ratio up to 10^9, highest mobility beyond 100 $cm^2/V{\cdot}s$ and lowest subthreshold swing (SS) of 70 mV/dec. High threshold voltage (V_T) stability is achieved in both negative and positive bias stress conditions with minimum threshold voltage shift (ΔV_T) of -18 mV under gate bias stress of -2 V for 5000 s. Such ultrahigh bias stability can be attributed to the passivation of oxygen vacancies by O_2 annealing. Temperature dependent I-V characteristics as well as bias instability are also comprehensively investigated. The optimized reliability indicates the back-end-of-line (BEOL) compatible ALD In_2O_3 does offer the great potential as the novel competitive channel in monolithic 3D integration.

Introduction

ALD amorphous oxide semiconductors are expected as promising BEOL compatible transistor channels due to reproducible wafer-scale synthesis, accurate film thickness control in atomic level, high uniformity on 3D structures and low thermal budget during fabrication process [1-3]. Recently, ALD In_2O_3 has been demonstrated as functional channels in top-gated or bottom-gated, vertically stacked and even gate-all-around (GAA) transistors with remarkable on-state current (I_{ON}) up to 20 mA/μm [1-6]. However, one remaining issue of ALD In_2O_3 is the trap induced large threshold voltage V_T shift under long time gate bias stress [7-9]. Therefore, an effective method is demanded to improve the reliability sufficiently enough towards practical application in BEOL integration.

In this work, bottom-gated ALD In_2O_3 FETs in both enhancement-mode (E-mode) and depletion-mode (D-mode) are fabricated and exhibit well-behaved switching characteristics after 400 °C O_2 annealing for 10 min. Oxygen vacancies are passivated during annealing and lead to excellent bias stability under both negative bias stress (NBS) and positive bias stress (PBS) conditions. A surprisingly small threshold voltage shift ΔV_T of -18 mV in D-mode FETs and 29 mV in E-mode FETs is achieved under 2 V gate bias stress for 5000 s. Temperature dependent I-V characteristics and bias instability are also systematically measured, illustrating a huge progress on lowering parameter shift via O_2 annealing towards practical applications.

Experiments

Fig. 1 shows the device schematic of an In_2O_3 FET. 40 nm W was deposited by sputtering as the bottom gate. 5 nm HfO_2 bottom dielectric and 1.6/3 nm In_2O_3 were grown by ALD at 200/225 °C. The film thickness was controlled by ALD cycles and examined by ellipsometer and TEM [3]. Next, the whole sample went through a high temperature O_2 annealing at 400 °C for 10 min to reduce oxygen vacancies. Finally, the In_2O_3 channel isolation was done by dry etching and 40 nm Ni was deposited by e-beam evaporation as the source/drain electrodes. All electrical characterization was conducted on a cascade probe station with Keysight B1500/1530 system.

Results and Discussion

To ensure the stability of ALD In_2O_3 for BEOL integration, a high temperature O_2 annealing up to 400 °C was applied. It turns out that the In_2O_3 channel still survives with outstanding electrical performance as shown in Figs. 2-9. Fig. 2 shows the typical transfer characteristics of a 1 μm long channel ALD In_2O_3 FET with T_{IO} of 1.6 nm and channel width (W_{ch}) of 1 μm. High on/off ratio over 10^8 and field-effect mobility (μ_{FE}) of 72 $cm^2/V{\cdot}s$ are achieved. The linear extrapolated V_T is larger than zero, indicating an E-mode operation. Fig. 3 presents the corresponding output characteristics, showing perfect current saturation at large V_{DS}. Figs. 4-5 show the transfer and output characteristics of a short channel E-mode device with L_{ch} of 60 nm. Open circles are measured by DC setup and solid ones are obtained by pulsed I-V setup with pulse width/period of 1 μs/100 ms to reduce self-heating effect in high bias region. High on/off ratio exceeding 10^9, lowest subthreshold swing of 70 mV/dec and maximum I_{ON} of 2.1 mA/μm are demonstrated. Figs. 6-7 present the transfer and output characteristics of a long channel In_2O_3 FET with T_{IO} of 3 nm and μ_{FE} of 115 $cm^2/V{\cdot}s$. Thicker In_2O_3 film results in a smaller bandgap and a deeper Fermi level in conduction band [1], so 3 nm In_2O_3 FETs operate in D-mode. Figs. 8-9 show the combined DC and pulsed measured transfer and output characteristics of a 40 nm short channel device in D-mode with maximum I_{ON} of 2.7 mA/μm. To investigate the temperature dependent electrical properties, I-V characteristics are measured up to 100 °C for both D-mode and E-mode devices as shown in Figs. 10-11. The transfer curves shift negatively at elevated temperatures with an average rate of shift $\partial V_T/\partial T$ of -6.1 mV/K and -7.3 mV/K for D-mode/E-mode, which are relatively smaller compared to -53.9 mV/K in previous In_2O_3 FETs without O_2 annealing [10]. Such shifting trend can be reversible during cooling. This is because the temperature dependent shift originates from the temporary creation of donor-like oxygen vacancies, which increase carrier density upon heating and cause a negative V_T shift [10, 11].

Reliability is of great significance in determining the feasibility of a material in real applications. Hence, we applied both NBS and PBS on 400 °C O_2 annealed ALD In_2O_3 FETs to examine the stability. Figs. 12-13 show the evolution of transfer curves of D-mode short channel In_2O_3 FETs under NBS/PBS of -2/2 V for 10000 s at room temperature. The shift is negligible under both bias conditions, confirming high robustness of In_2O_3 transistors enabled by high temperature O_2 annealing. Figs. 14-15 present the time evolution of ΔV_T extracted from transfer curves under NBS and PBS for both D-mode and E-mode devices. A relatively small ΔV_T of -18/21 mV under NBS/PBS for 5000 s is achieved in D-mode In_2O_3 FETs and a minimum ΔV_T of -113/29 mV under NBS/PBS for 5000 s is obtained in E-mode devices. Such little V_T shifts have been considerably reduced compared to previous bias stress studies on In_2O_3 transistors without high temperature O_2 annealing, where ΔV_T usually exceeds 100 mV under stress less than 1000 s [7-9]. As mentioned above, oxygen vacancies play an important role in In_2O_3 electrical characteristics and donor-like traps can be generated during the stress, inducing serious V_T shift [7-9]. Therefore, O_2 annealing is a simple but cruscial process to fill these vacancies and reinforce the device long term reliability. Figs. 16-19 plot the time evolution of ΔV_T of D-mode and E-mode In_2O_3 FETs under NBS and PBS at different temperatures. The larger negative V_T shift at higher temperatures can be ascribed to a faster generation of oxygen vacancies as well as H_2O adsorption from air, donating excessive electrons in the channel [12, 13]. To further minimize V_T shift, a proper encapsulation of In_2O_3 channel to avoid ambient reactions is indispensable in practical applications. Fig. 20 shows a benchmark of stability and mobility of oxide semiconductor thin film transistors (TFTs) [9, 14-24]. The stability is estimated from ΔV_T after 5000 s stress. Generally, the high temperature O_2 annealed ALD In_2O_3 exhibits outstanding electrical performance with preferred high mobility and V_T stability, which is critical for its paractical applications in monolithic 3D integration.

Conclusion

In conclusion, a record high stability is demonstrated in both E-mode and D-mode ALD In_2O_3 FETs through high temperature O_2 annealing. The passivation of oxygen vacancies leads to a significant reduction of V_T shift in temperature dependent I-V characteristics as well as negative and positive bias stability. This work proves the feasibility of ALD In_2O_3 as a practical channel material in BEOL compatible monolithic 3D integration and other related applications.

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Reference: [1] M. Si et al., Nano Lett., p. 500, 2021. [2] M. Si et al. VLSI, p. TF2.4, 2021. [3] M. Si et al., Nat. Electron., p. 164, 2022. [4] P.-Y. Liao et al., VLSI, 2022. [5] Z. Zhang et al., Appl. Phys. Lett., p. 202104, 2022. [6] Z. Zhang et al., IEEE EDL, p. 1905, 2022. [7] Y. P. Chen et al., IEEE EDL, p. 232, 2021. [8] A. Charnas et al., IEEE TED, p. 5549, 2022. [9] Z. Zhang et al., IEDM, 2022. [10] A. Charnas et al., Appl. Phys. Lett., p. 263503, 2021. [11] K. Hoshino et al., IEEE EDL, p. 818, 2010. [12] J. K. Jeong et al., Appl. Phys. Lett., p. 123508, 2008. [13] J. Zhang et al., IEEE EDL, 2022. [14] T. Kizu et al., Appl. Phys. Lett., p. 152103, 2014. [15] E. Chong et al., Semicond. Sci. Technol., p. 012001, 2011. [16] H. C. Wu et al., ECS J. Solid State Sci. Technol., p. Q24, 2013. [17] D. S. Han et al., J. Electron. Mater., p. 2470, 2013. [18] E. Chong et al., Appl. Phys. Lett., p. 252112, 2010. [19] B. S. Yang et al., Appl. Phys. Lett., p. 122110, 2011. [20] X. Li et al., Mater. Sci. Semicond. Process., p. 1292, 2013. [21] W. Chakraborty et al., IEEE TED, p. 5336, 2020. [22] D. Ki, Ngwashi et al., Mater. Res. Express, p. 026302, 2020. [23] B. Du Ahn et al., IEEE TED, p. 4132, 2014.

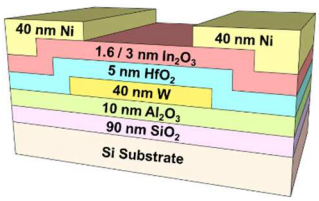

Fig. 1. Device schematic of an ALD In_2O_3 FET with 40 nm W bottom gate.

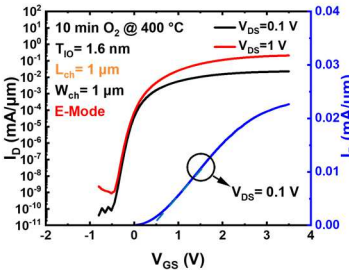

Fig. 2. Transfer characteristics of a 1 μm long channel In_2O_3 FET in E-mode. μ_{FE}=72 $cm^2/V{\cdot}s$.

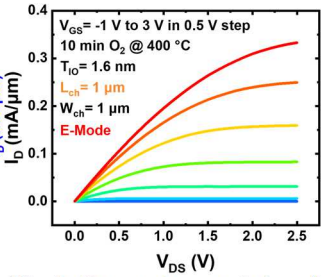

Fig. 3. Output characteristics of a 1 μm long channel In_2O_3 FET in E-mode.

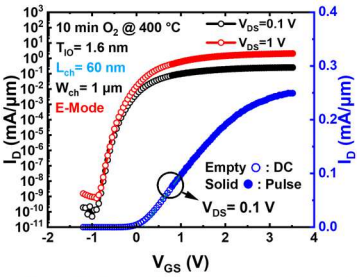

Fig. 4. Transfer characteristics of a 60 nm short channel In_2O_3 FET in E-mode.

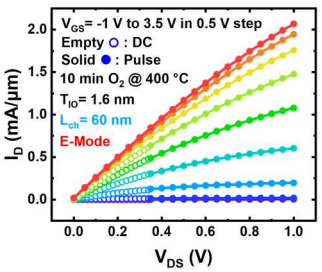

Fig. 5. Output characteristics of a 60 nm short channel In_2O_3 FET in E-mode. I_{ON}=2.1 mA/μm.

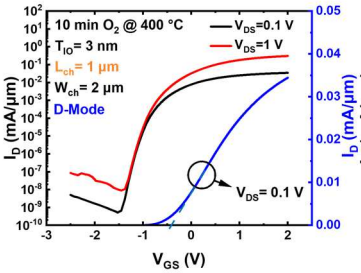

Fig. 6. Transfer characteristics of a 1 μm long channel In_2O_3 FET in D-mode. μ_{FE}=115 $cm^2/V{\cdot}s$.

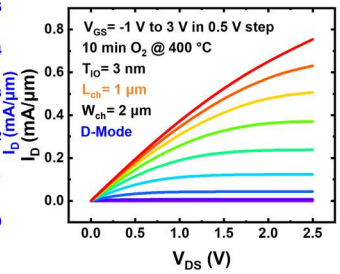

Fig. 7. Output characteristics of a 1 μm long channel In_2O_3 FET in D-mode.

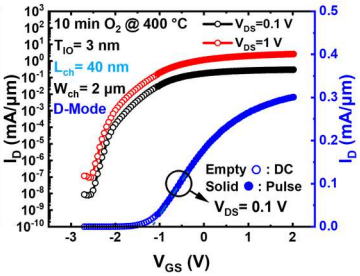

Fig. 8. Transfer characteristics of a 60 nm short channel In_2O_3 FET in D-mode.

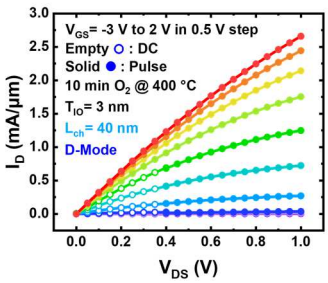

Fig. 9. Output characteristics of a 60 nm short channel In_2O_3 FET in D-mode. I_{ON}=2.7 mA/μm.

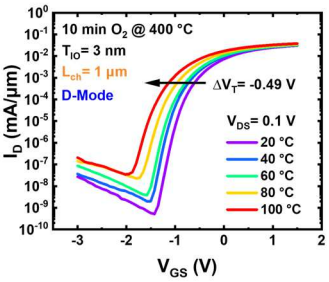

Fig. 10. Temperature dependent transfer curves of a D-mode In_2O_3 FET.

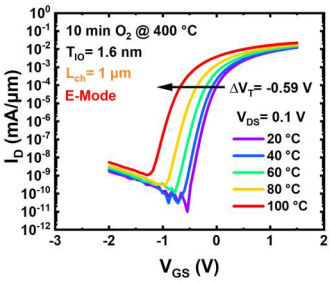

Fig. 11. Temperature dependent transfer curves of an E-mode In_2O_3 FET.

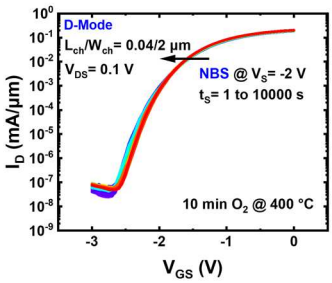

Fig. 12. Evolution of transfer curves of a D-mode In_2O_3 FET under NBS of -2 V for 10^4 s.

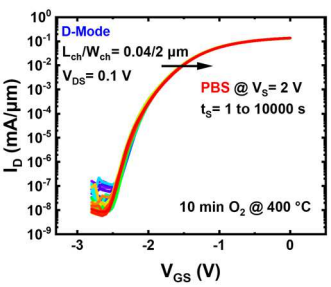

Fig. 13. Evolution of transfer curves of a D-mode In_2O_3 FET under PBS of 2 V for 10^4 s.

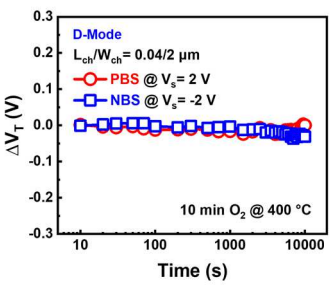

Fig. 14. Time evolution of ΔV_T of a D-mode In_2O_3 FET. ΔV_T of -18 mV after NBS for 5000 s.

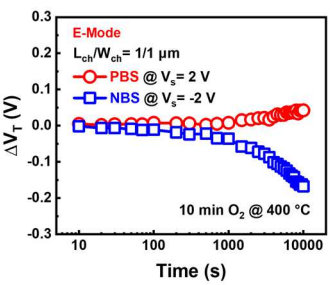

Fig. 15. Time evolution of ΔV_T of an E-mode In_2O_3 FET. ΔV_T of 29 mV after PBS for 5000 s.

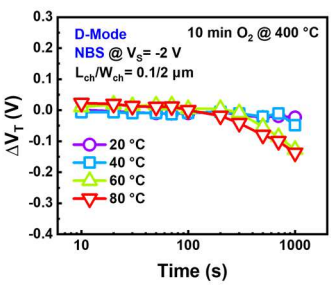

Fig. 16. Time evolution of ΔV_T of D-mode In_2O_3 FETs under NBS of -2 V at different temperatures.

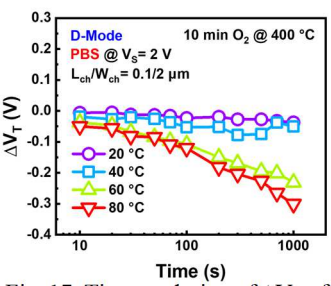

Fig. 17. Time evolution of ΔV_T of D-mode In_2O_3 FETs under PBS of 2 V at different temperatures.

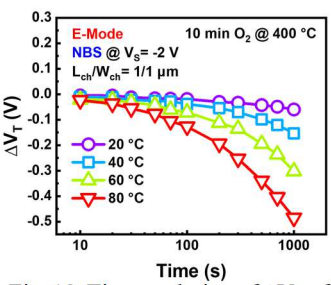

Fig. 18. Time evolution of ΔV_T of E-mode In_2O_3 FETs under NBS of -2 V at different temperatures.

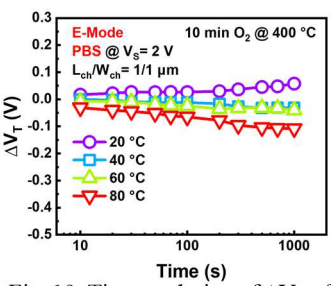

Fig. 19. Time evolution of ΔV_T of E-mode In_2O_3 FETs under PBS of 2 V at different temperatures.

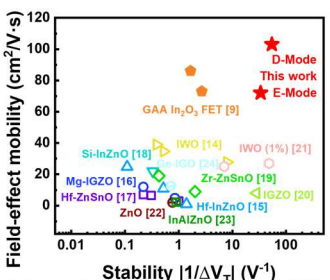

Fig. 20. Benchmark of stability and mobility of oxide TFTs. ΔV_T is estimated after 5000 s stress.